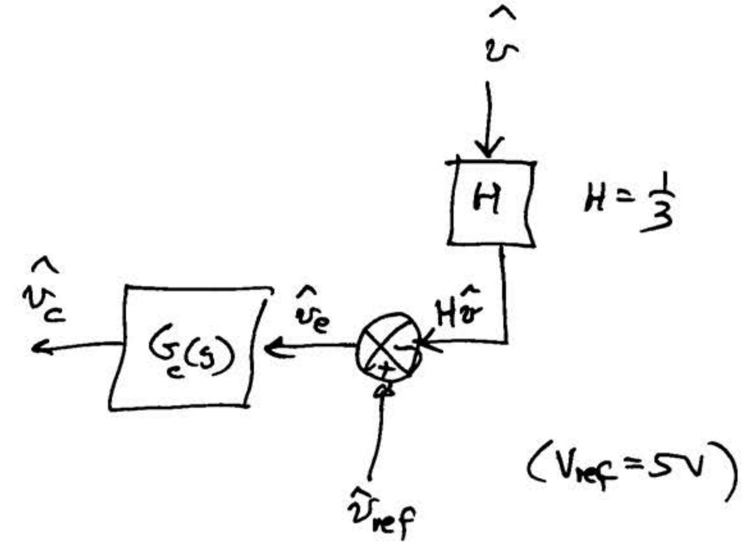
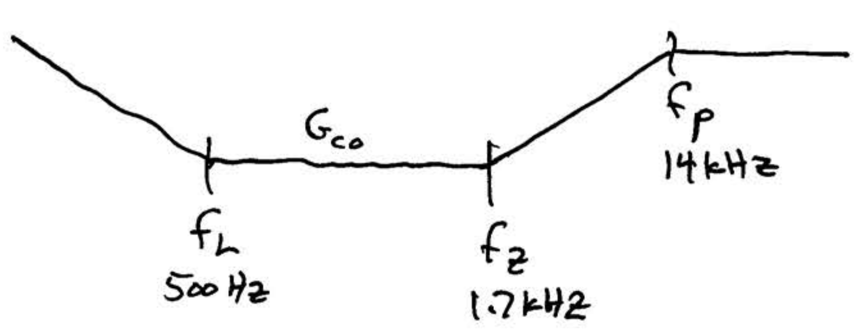
Design of op amp PID compensator circuit for the example of Section 9.5.4

We want to synthesize an op amp circuit that realizes the feedback block diagram below (excerpted from Fig. 9.22):



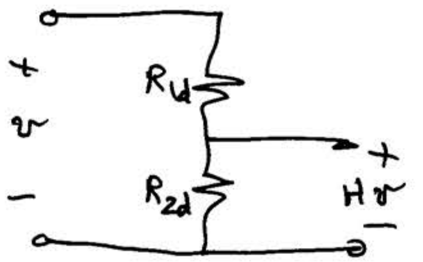
with $$G_c(s) = G_{co} \frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{\omega_L}{s}\right)}{\left(1+\frac{s}{\omega_p}\right)}$$ from Eq. (9.60)



$G_{co} = 3.7 \Rightarrow 11.3\ dB$ is the midband gain shown above (why?)

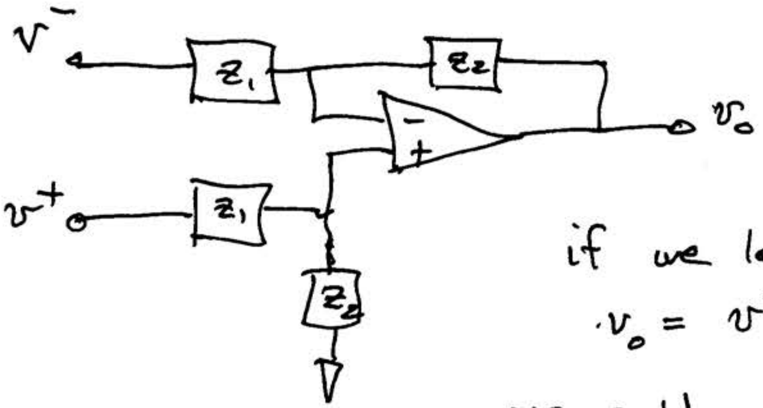
We need a candidate op amp circuit that can realize all of the functions of block diagram. Here are some basic circuits from the beginning circuits class

Voltage divider - suitable for H



$$H = \frac{R_{2d}}{R_{1d}+R_{2d}}$$

Subtractor - suitable for summing node



if we let $Z_1 = Z_2$ then

$$v_o = v^+ - v^-$$

we could use this circuit with

$v^- \rightarrow H\hat{v}$

$v^+ \rightarrow \hat{v}_{ref}$

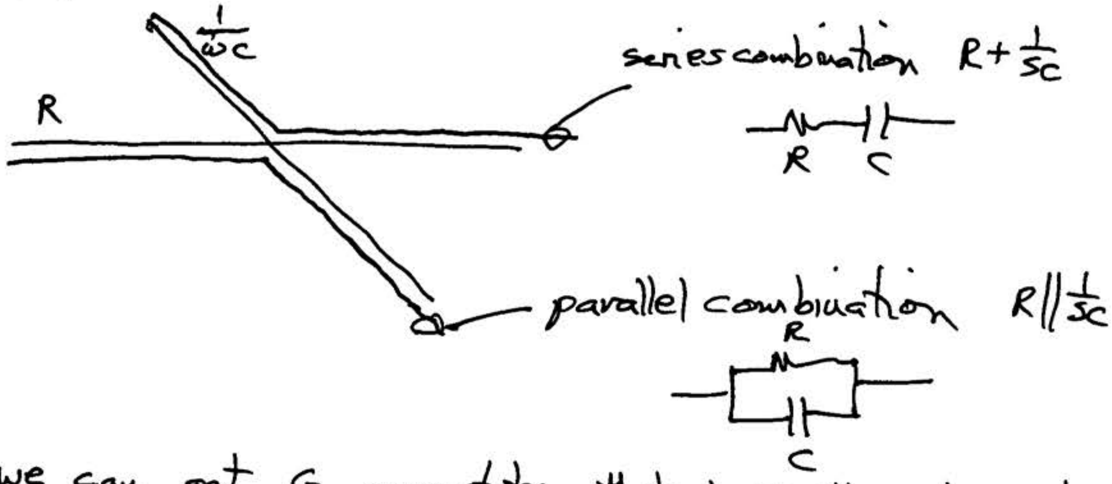
$v_o \rightarrow \hat{v}_e$

More generally, with $Z_1 \neq Z_2$, we get

$$v_o = \frac{Z_2}{Z_1}\left(v^+ - v^-\right)$$

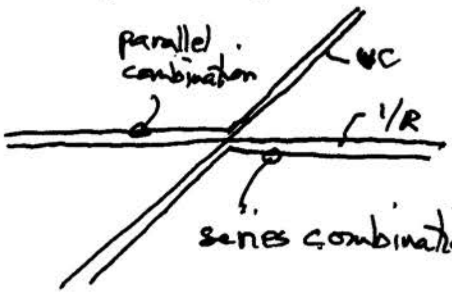
By proper choice of $\frac{Z_2}{Z_1} = G_c(s)$, we could use $v^- \rightarrow H\hat{v}$, $v^+ \rightarrow \hat{v}_{ref}$, and $v_o \rightarrow \hat{v}_c$

We need to synthesize series-parallel combinations of R's and C's so that $\frac{Z_2}{Z_1}$ has the $G_c(s)$ asymptotes of page 1.

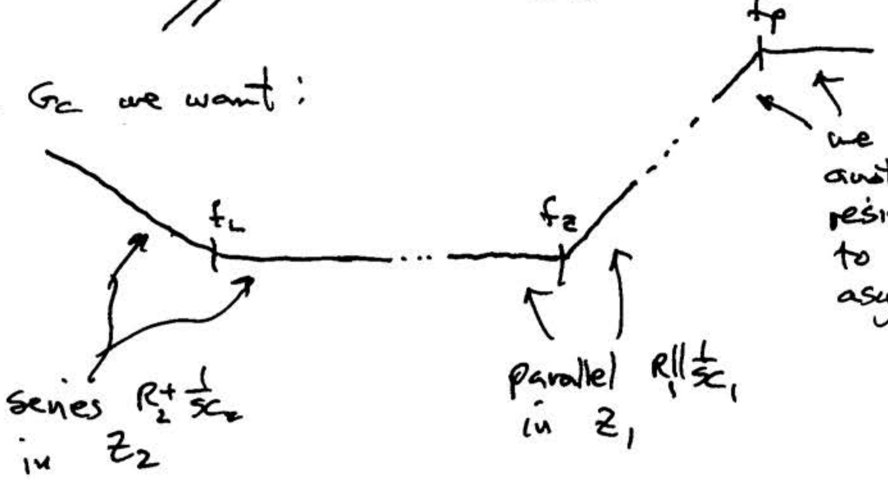


we can get G_c asymptotes that have the above shapes by placing the above impedances in Z_2.

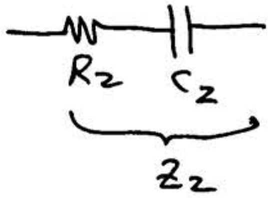
If we put the above impedance combinations in Z_1, then G_c will have asymptotes proportional to $\frac{1}{Z_1}$ that look like

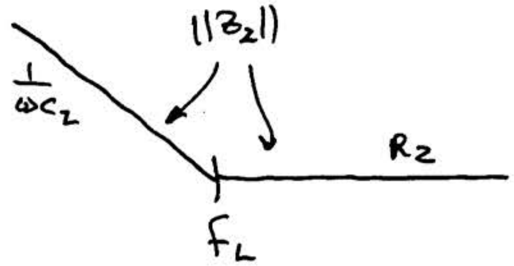


the G_c we want:



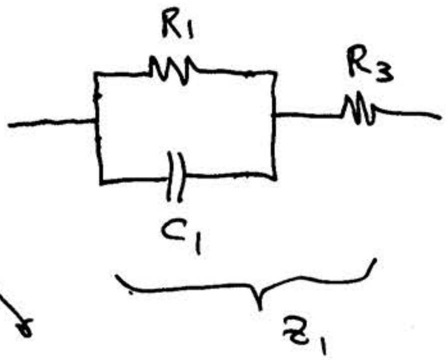
So $Z_2 = R_2 + \frac{1}{sC_2}$

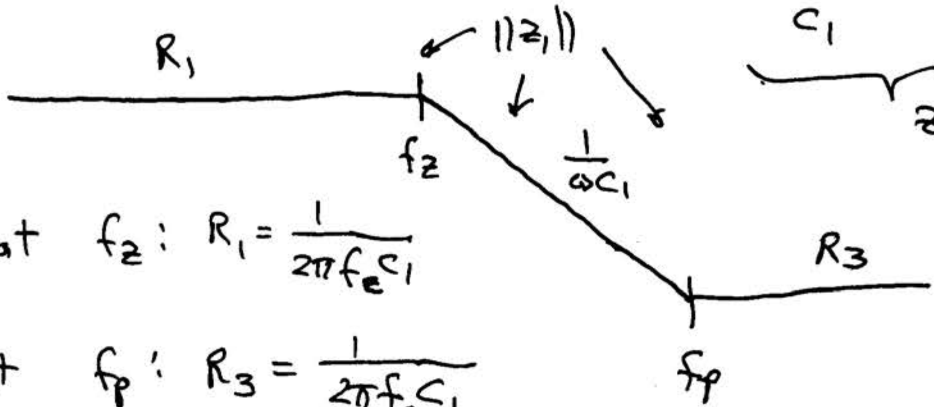




at f_L: $R_2 = \frac{1}{2\pi f_L C_2}$

$Z_1 = \left(R_1 \| \frac{1}{sC_1}\right) + R_3$

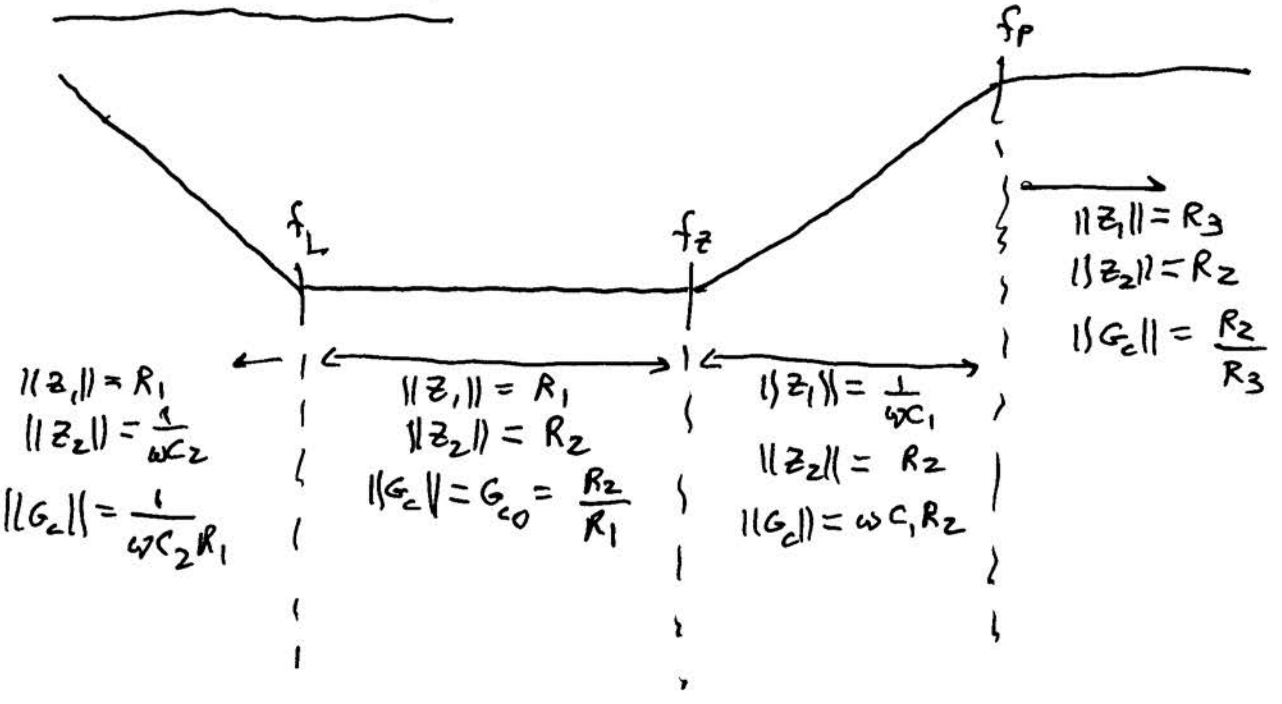




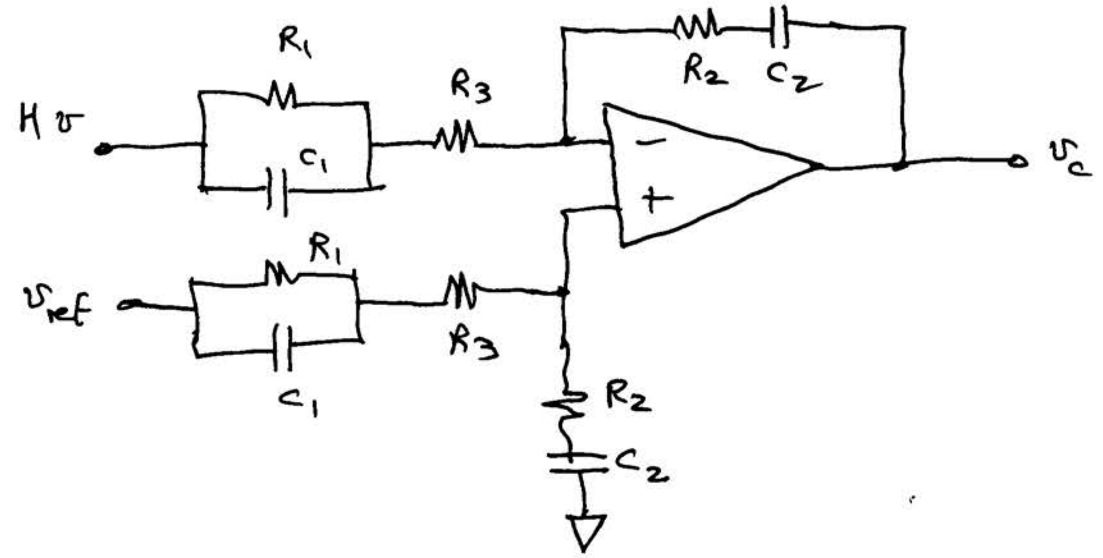
at f_z: $R_1 = \frac{1}{2\pi f_z C_1}$

at f_p: $R_3 = \frac{1}{2\pi f_p C_1}$

Construct $G_c = \frac{Z_2}{Z_1}$ Divide asymptotes



So the op amp circuit is



Choose element values

from above;

$$G_{co} = \frac{R_2}{R_1}, \quad R_2 = \frac{1}{2\pi f_L C_2},$$

$$R_1 = \frac{1}{2\pi f_z C_1}, \quad R_3 = \frac{1}{2\pi f_p C_1}$$

We have 4 equations and 5 unknowns.
One element value can be chosen arbitrarily, and this choice determines the impedance and current levels in the circuit.

Choose $R_2 = 100k\Omega$ to get currents of 10's of μA

then $C_2 = \frac{1}{2\pi f_L R_2} = 3.2\ nF$ (with $f_L = 500\ Hz$)

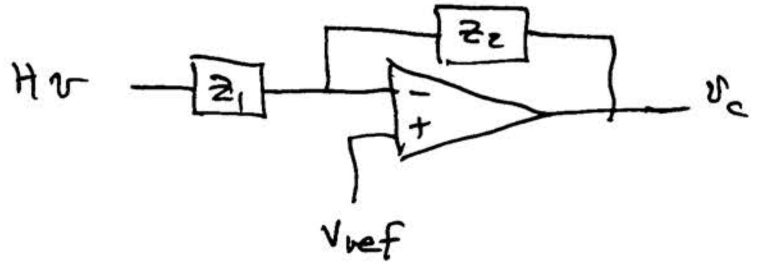
and $R_1 = \frac{R_2}{G_{co}} = \frac{100k}{3.7} = 27\ k$

$C_1 = \frac{1}{2\pi f_z R_1} = 3.5\ nF$ with $f_z = 1.7\ kHz$

$R_3 = 1/2\pi f_p C_1 = 3.3k$ with $f_p = 14\ kHz$

Some additional considerations:

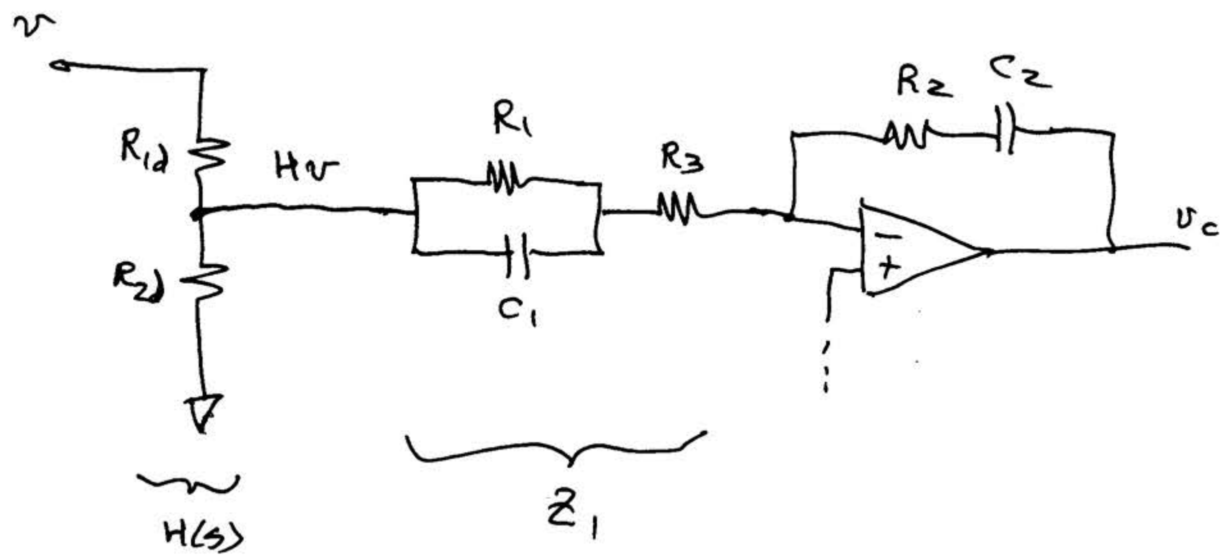
1. In this dc regulator application, if $v_{ref}(t) = V_{ref}$ is fixed (so $\hat{v}_{ref} = 0$ always) then $V^+ = V_{ref}$ never changes, and we could simply connect Vref directly to V^+:



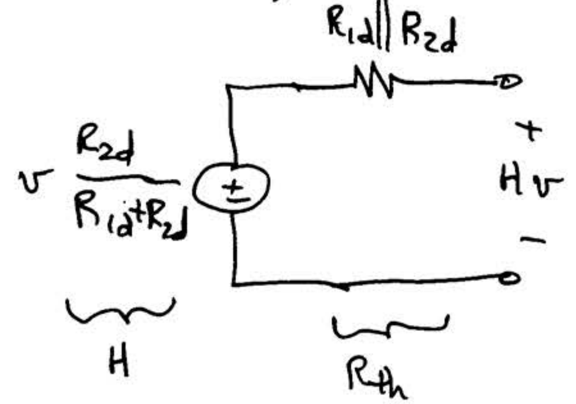
This will, however, add poles and zeroes to the transfer function from $\hat{v}_{ref}$ to $\hat{v}_c$. So if $v_{ref}(t)$ can have a significant ac component then it would be desirable to include Z_1 and Z_2 in the v_{ref} circuit.

In the above circuit: if the op amp has a significant input bias current, then it may be desirable to insert a resistor of value $R_1 + R_3$ between V_{ref} and the noninverting input so that the bias current does not affect the regulated dc output voltage.

2. When we connect this op amp circuit to the $H(s)$ voltage divider, Z_1 loads the divider:

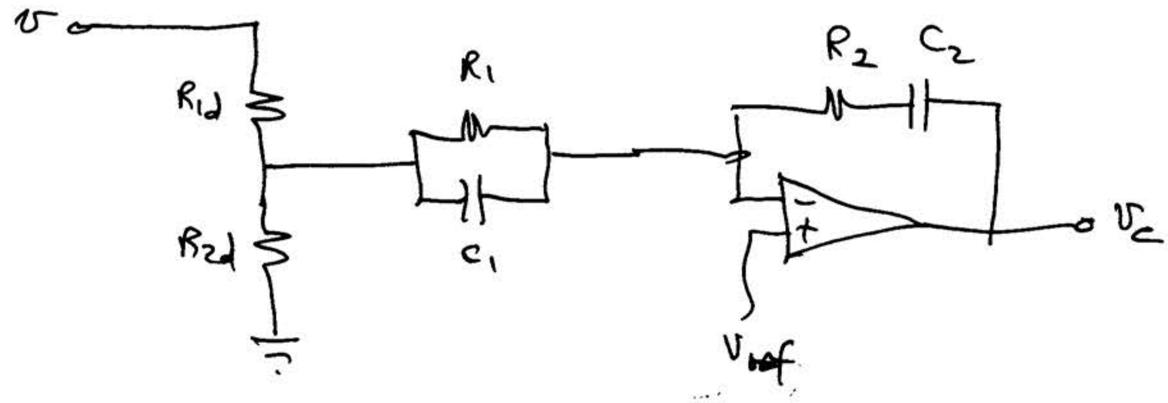


We can account for this in our design: Thevenin equivalent of the voltage divider:



$R_{th} = R_{1d} \| R_{2d}$ is effectively in series with Z_1

If we choose $R_{1d} \| R_{2d} = R_{th}$ to be equal to R_3, then we could eliminate R_3 and use R_{th} instead:



to get this to work, we must choose

$$R_{1d} \| R_{2d} = R_3 = 3.3k$$

with $\dfrac{R_{2d}}{R_{1d}+R_{2d}} = H = \dfrac{1}{3}$

note that $R_{1d} \| R_{2d} = H\, R_{1d}$

so we need $R_{1d} = \dfrac{R_3}{H} = 10k$

and $R_{2d} = R_{1d} \dfrac{H}{1-H} = 5k$

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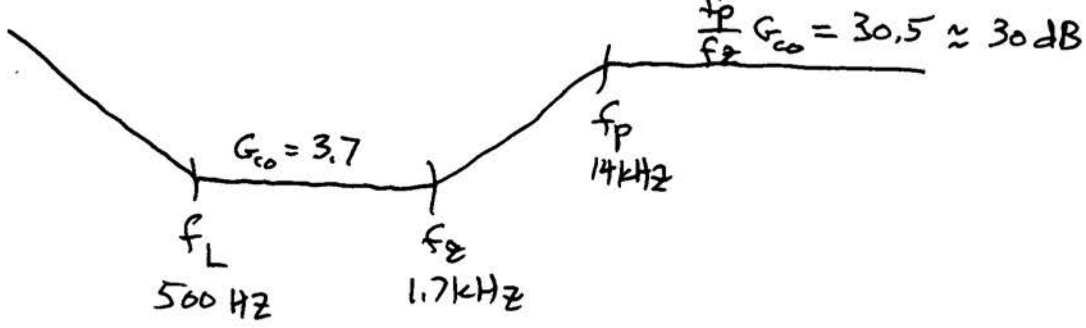
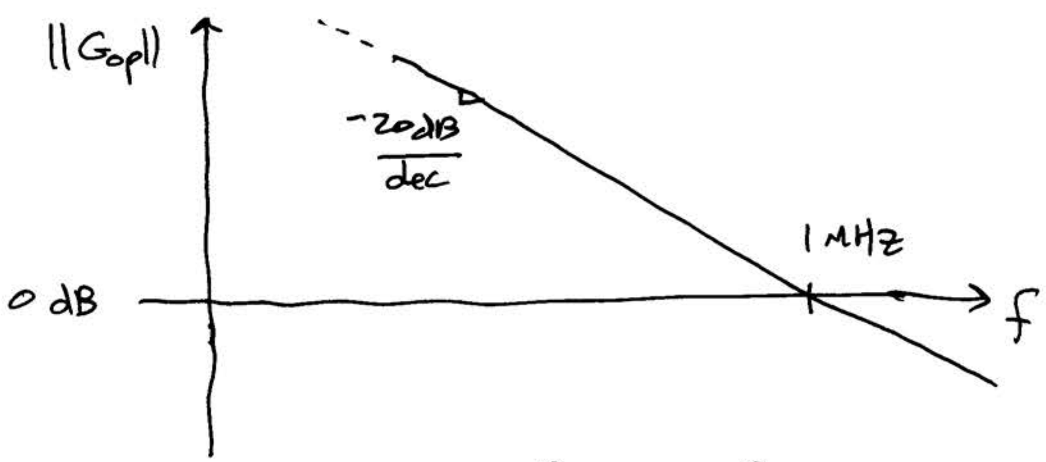
3. This design asks the op amp to have gain out to infinite frequency. This won't happen with a practical, physical op amp. Our G_c is



Suppose our op amp has a gain-bandwidth product of 1 MHz, so that its internal gain is



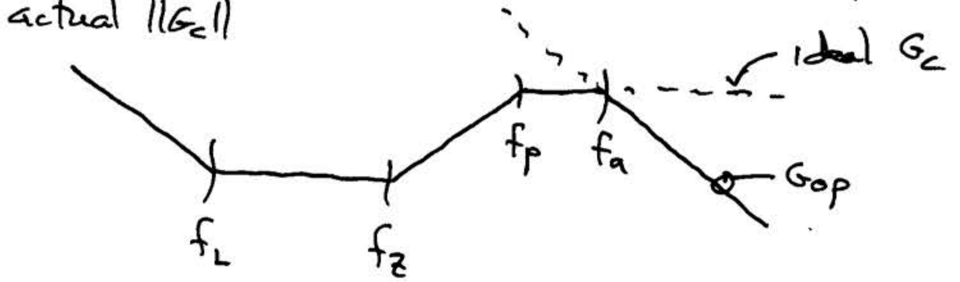
This asymptote is of the form

$$\|G_{op}\| = \frac{1}{\left(\frac{f}{f_{gbp}}\right)} \qquad \text{with } f_{gbp} = 1\text{ MHz}$$

It has the value 30.5 at frequency f_a:

$$30.5 = \frac{1}{\left(\frac{f_a}{f_{gbp}}\right)} \qquad = \frac{f_{gbp}}{30.5} = 32.8\text{ kHz}$$

Above f_a, the op amp is not capable of producing the desired gain, so the G_c transfer function will roll off:



The added pole at f_a will degrade the phase margin, so we will need to account for it in our design.