Foundations of Analog and Digital Electronic Circuits

Solutions to Exercises and Problems

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July 3, 2005

Chapter 1

The Circuit Abstraction

Exercises

Exercise 1.1 Quartz heaters are rated according to the average power drawn from a 120 volt AC 60 Hz voltage source. Estimate the resistance (when operating) a 1200 watt quartz heater.

NOTE: The voltage waveform for a 120 volt AC 60 Hz waveform is

$$v(t) = \sqrt{2}\ \ 120\ cos(2\pi 60t)$$

The factor of $\sqrt{2}$ in the peak amplitude cancels when the average power is computed. One result is that the peak amplitude of the voltage from a 120 volt wall outlet is about 170 volts.

Solution:

Power $= 1200$ watts $= i \cdot v = i^2 \cdot R = \frac{v^2}{R}$

$1200 = \frac{v^2}{R}$; where v is average value of sinusoidal voltage,

$$v(t) = \sqrt{2} \cdot 120\ cos(120\pi t)$$

Average value of a sinusoidally oscillating signal is the peak value divided by $\sqrt{2}$.

Therefore $v = 120$

$$R = \frac{120^2}{1200}$$

Therefore

$$R = 12\Omega$$

ANS:: $R = 12\Omega$

Exercise 1.2

a) The battery on your car has a rating stated in ampere-hours which permits you to estimate the length of time a fully charged battery could deliver any particular current before discharge. Approximately how much energy is stored by a 50 ampere-hour 12 volt battery?

b) Assuming 100% efficient energy conversion, how much water stored behind a 30 meter high hydroelectric dam would be required to charge the battery?

Solution:

a) $Power = i \cdot v = \frac{Energy}{time}$

$Energy = i \cdot v \cdot (time) = (50\ ampere - hours)(12\ volts) = 600\ ampere - hour - volts$

$600 ampere - hour - volts \cdot 3600\ seconds/hour = 2.16 \times 10^6\ Joules$

b) Potential Energy $\longrightarrow$ Electrical Energy; assume 100% efficiency

$m \cdot g \cdot h = 2.16 \times 10^6 Joules$

$m = 2.16 \times \frac{10^6}{g \cdot h}$

$g \approx \frac{10m}{s^2}$

$h = 30m$, height of water, assuming that there is enough water in the dam such that the height does not change as some of the water is taken out

$$mass = 14,400\ kg\ of\ water$$

ANS:: (a) 2.2×10^6 Joules, (b) 7200 kg, or about 8 tons.

Exercise 1.3 In the circuit in Figure 1.1, R is a linear resistor and $v = V_{DC}$ a constant (DC) voltage. What is the power dissipated in the resistor, in terms of R and V_{DC}?

Solution:

$Power = i \cdot v$

But $i = v/R$ (Ohm's Law), so

$$Power = \frac{v}{R} \cdot v = \frac{{V_{DC}}^2}{R}$$

ANS:: $\frac{V_{DC}^2}{R}$

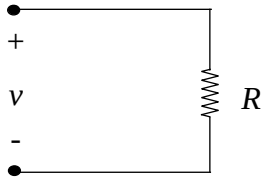


Figure 1.1:

Exercise 1.4 In the circuit of the previous exercise (Figure 1.1), $v = V_{AC}\ cos\omega t$, a sinusoidal (AC) voltage with peak amplitude V_{AC} and frequency ω, in radians/sec.

a) What is the average power dissipated in R?

b) What is the relationship between V_{DC} and V_{AC} in Figure 1.1 when the average power in R is the same for both waveforms?

Solution:

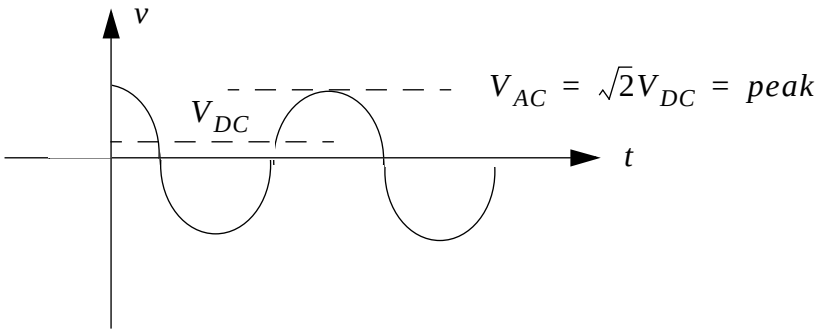


Figure 1.2:

a) If peak voltage is V_{AC}, then

$$V_{AC} = \sqrt{2}\, V_{DC}$$

where V_{DC} is the average amplitude of the voltage signal.

$$Average\ Power = \frac{(V_{average})^2}{R} = \frac{{V_{DC}}^2}{R} = \frac{(V_{AC}/\sqrt{2})^2}{R} = \frac{{V_{AC}}^2}{2R}$$

b) If peak voltage is V_{AC}, then

$$V_{AC} = \sqrt{2}\, V_{DC}$$

where V_{DC} is the average amplitude of the voltage signal.

ANS:: (a) $V_{AC}^2/2R$ (b) $V_{AC} = \sqrt{2}\ V_{DC}$

Problems

Problem 1.1 Determine the resistance of a cube with sides of length l cms and resistivity 10 Ohm-cms, when a pair of opposite surfaces are chosen as the terminals.

Problem 1.2 Sketch the $v - i$ characteristic of a battery rated at 10V with an internal resistance of 10 Ohms.

Problem 1.3 A battery rated at 7.2V and 10000 joules is connected across a lightbulb. Assume that the internal resistance of the battery is zero. Further assume that the resistance of the lightbulb is 100Ω.

1. Draw the circuit containing the battery and the lightbulb and label the terminal variables for the battery and the lightbulb according to the associated variables discipline.
2. What is the power into the lightbulb?
3. Determine the power into the battery.
4. Show that the sum of the power into the battery and the power into the bulb is zero.
5. How long will the battery last in the circuit?

Problem 1.4 A sinusoidal voltage source

$$v = 10sin\omega t$$

is connected across a 1k resistor.

1. Make a sketch of $p(t)$, the instantaneous power supplied by the source.
2. Determine the average power supplied by the source.
3. Now, suppose that a square wave generator is used as the source. If the square wave signal has a peak-to-peak of 20V and a zero average value, determine the average power supplied by the source.
4. Next, if the square wave signal has a peak-to-peak of 20V and a 10V average value, determine the average power supplied by the source.

Chapter 2

Resistive Networks

Exercises

Exercise 2.1 Find the equivalent resistance from the indicated terminal pair of the networks in Figure 2.1.

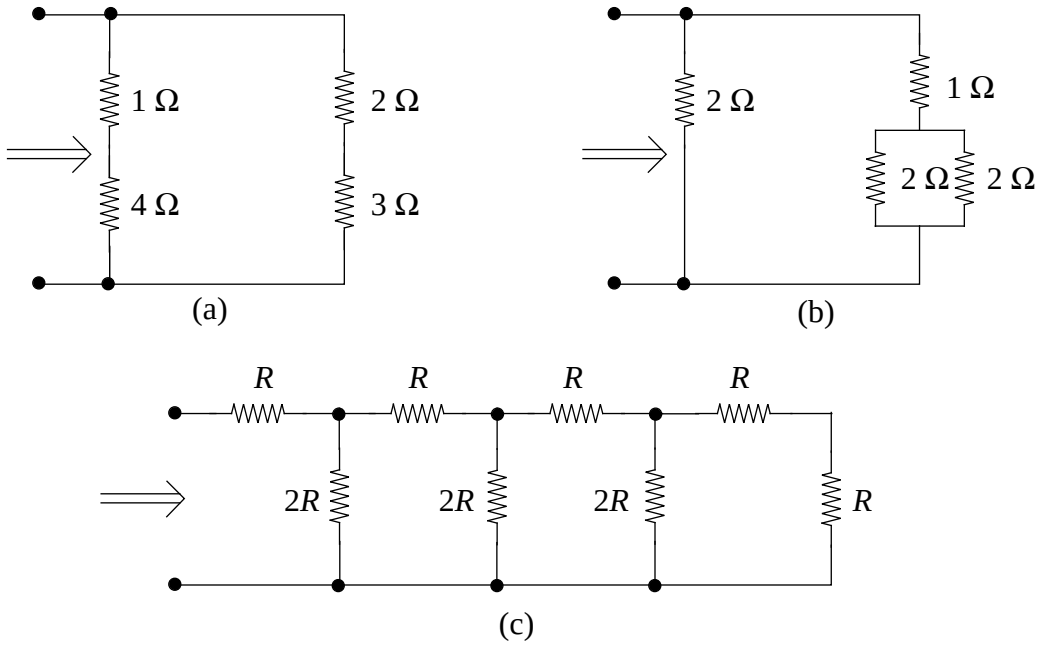


Figure 2.1:

Solution:

a)

$$R_{EQ} = 5 \,||\, 5 = \frac{5 \cdot 5}{5+5} = 2.5\Omega$$

b)

$$R_{EQ} = 2 \,||\, (1 + 2 \,||\, 2) = 2 \,||\, 2 = 1\Omega$$

c)

$$2R \,||\, 2R = \frac{4R^2}{4R} = R$$

Therefore

$$R_{EQ} = R + R = 2R$$

ANS:: (a) 2.5Ω (b) 1Ω (c) $2R$

Exercise 2.2 Determine the voltages v_A and v_B (in terms of v_S) for the network shown in Figure 2.2.

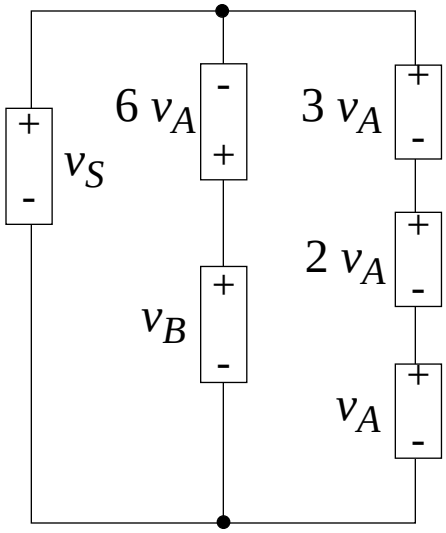


Figure 2.2:

Solution:

KVL:

(1)

$$v_S + 6v_A - v_B = 0$$

$$v_B = v_S + 6v_A$$

(2)

$$v_B - 6v_A - 3v_A - 2v_A - v_A = 0$$
$$v_B = 12v_A$$

$$12v_A = v_S + 6v_A$$

$$6v_A = v_S$$
$$v_A = \frac{v_S}{6}$$
$$v_B = 2v_S$$

ANS:: $v_A = v_S/6$, $v_B = 2v_S$

Exercise 2.3 Find the equivalent resistance between the indicated terminals (all resistances in ohms) in Figure 2.3.

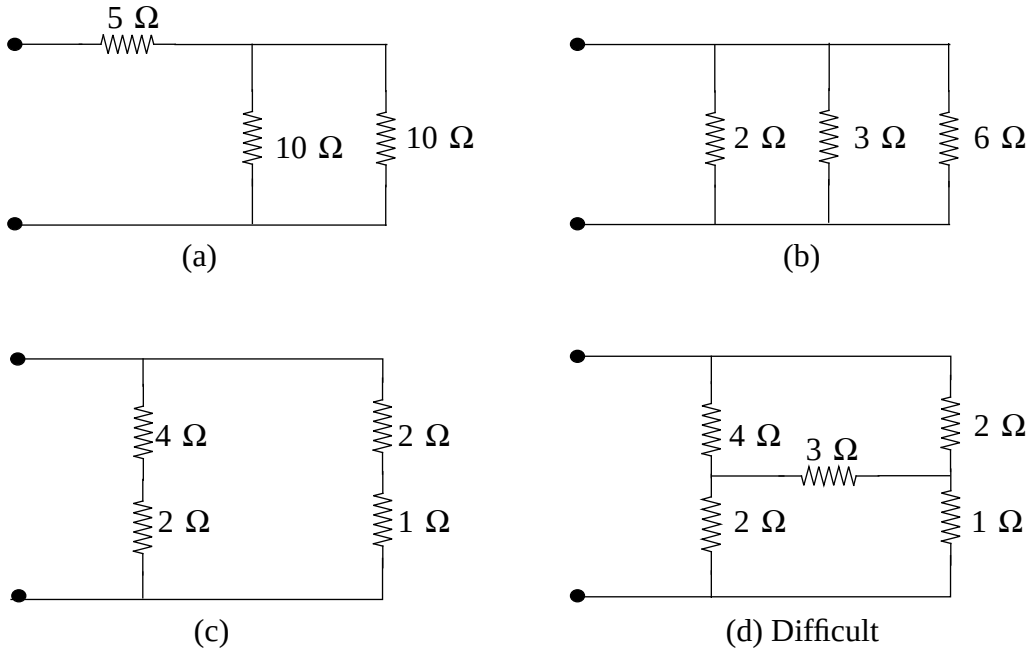


Figure 2.3:

Solution:

a) $R_{EQ} = 5 + 10||10 = 10\Omega$

b) $R_{EQ} = [2||3]||6 = 1\Omega$

c) $R_{EQ} = (4+2)||(2+1) = 2\Omega$

d) Apply test voltage: $R_{EQ} = \frac{v_{test}}{i_{test}}$

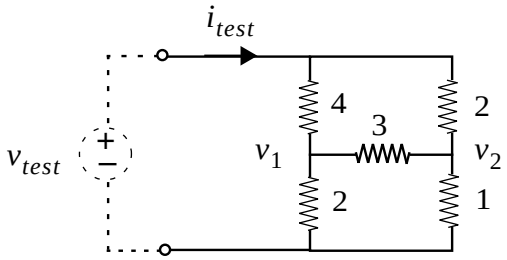


Figure 2.4:

$$\frac{(v_{test} - v_1)}{4} + \frac{(0 - v_1)}{2} + \frac{(v_2 - v_1)}{3} = 0$$

$$\frac{(v_{test} - v_2)}{2} + \frac{(v_1 - v_2)}{3} + \frac{(0 - v_2)}{1} = 0$$

$$v_1 = \frac{v_{test}}{3}, \qquad v_2 = \frac{v_{test}}{3}$$

Substitute these expressions into the equation below:

$$i_{test} + \frac{(v_1 - v_{test})}{4} + \frac{(v_2 - v_{test})}{2} = 0$$

$$\frac{v_{test}}{i_{test}} = R_{EQ} = 2\Omega$$

ANS:: (a) 10Ω (b) 1Ω (c) 2Ω (d) 2Ω

Exercise 2.4 Determine the indicated branch voltage or branch current in each network in Figure 2.5.

Solution:

a) $v = i \cdot R = 3 \cdot 2 = 6\ volts$

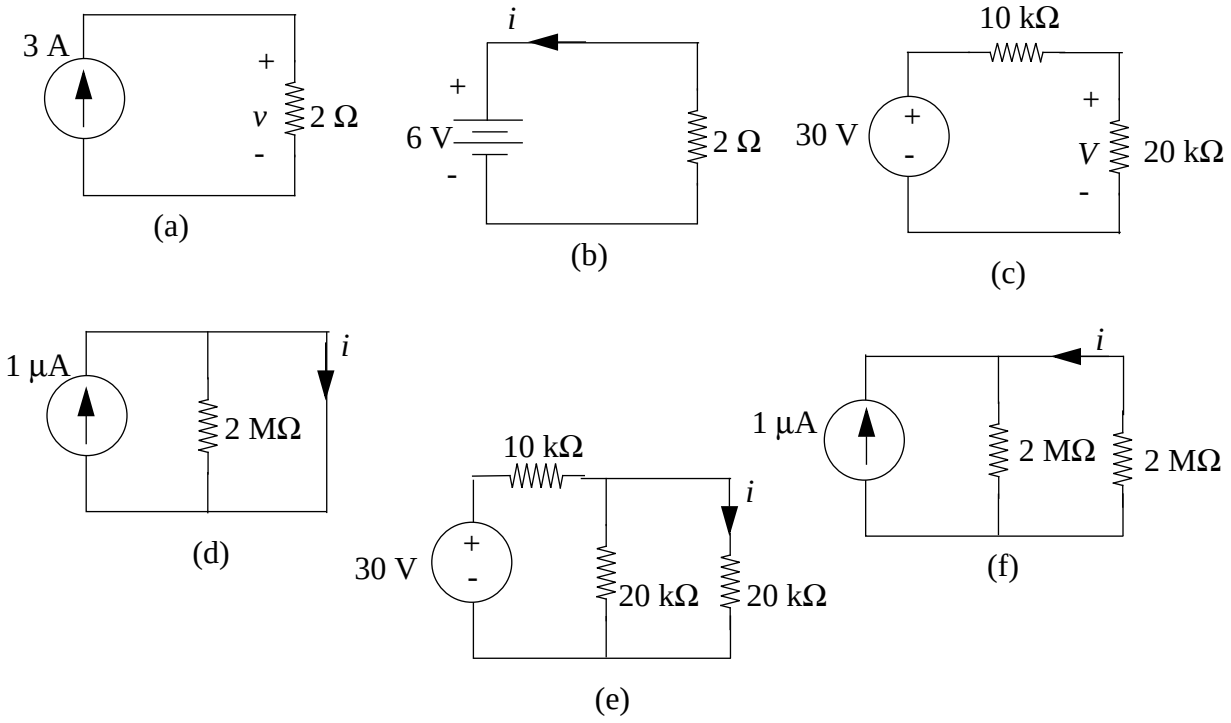


Figure 2.5:

b) $i = \frac{-6V}{2\Omega} = -3\ amps$

c) KVL: $30 - i(10,000 + 20,000) = 0$

$i = 1\ milliamp = 1mA$

$V = 20,000 \cdot i = 20\ volts$

d) $i = 1\mu A$; current follows path of “short circuit”

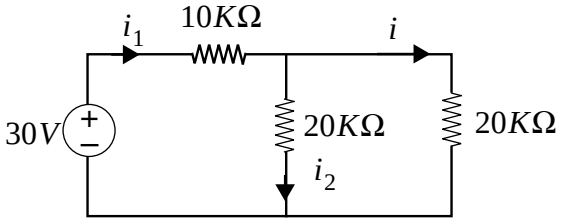


Figure 2.6:

e) $i_1 = \frac{30V}{R_{EQ}}$

$R_{EQ} = 10k + 20k||20k$

$R_{eq} = 20k\Omega$

$i_1 = 1.5mA$

KVL: (right loop)

$i_2(20,000) - i(20,000) = 0$

$i = i_2$

KCL:

$i_1 - i - i_2 = 0$

This implies $i_1 = 2i$

$2i = 1.5mA$

$i = 0.75mA$

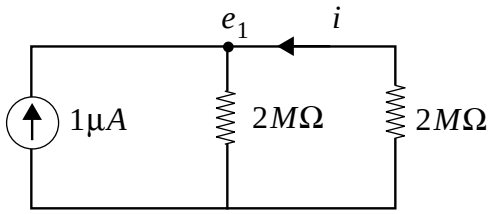


Figure 2.7:

f) KCL: $1\mu A + \frac{0-e_1}{2M\Omega} + \frac{0-e_1}{2M\Omega} = 0$

$e_1 = 1volt$

$i = \frac{0-e_1}{2M\Omega} = -0.5\mu A$

ANS:: (a) 6V (b) -3A (c) 20V (d) $1\mu A$ (e) .75mA (f) -.5 μA

Exercise 2.5 Find the equivalent resistance at the indicated terminal pair for each of the networks shown in Figure 2.8.

Solution:

a)

$$R_{EQ} = R_1 + R_2 + R_3$$

b)

$$R_{EQ} = R_1||R_2 + R_3 = \frac{R_1R_2 + R_3(R_1 + R_2)}{R_1 + R_2}$$

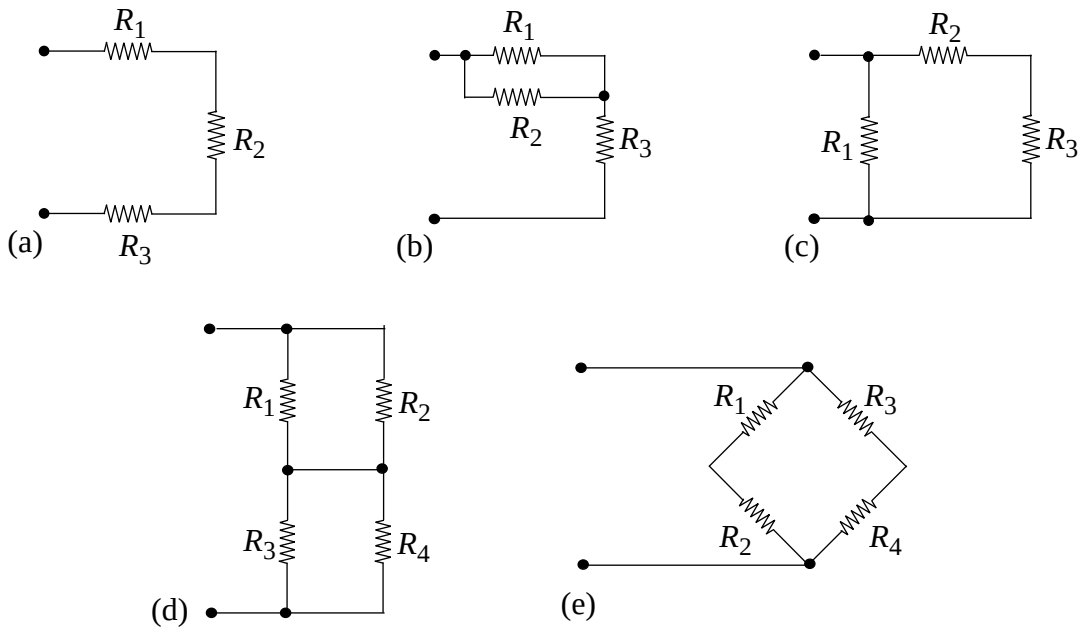


Figure 2.8:

c)

$$R_{EQ} = R_1||R_2 + R_3 = \frac{R_1(R_2 + R_3)}{R_1 + R_2 + R_3}$$

d)

$$R_{EQ} = R_1||R_2 + R_3||R_4 = \frac{R_1 R_2}{R_1 + R_2} + \frac{R_3 R_4}{R_3 + R_4}$$

e)

$$R_{EQ} = (R_1 + R_2)||(R_3 + R_4) = \frac{(R_1 + R_2)(R_3 + R_4)}{R_1 + R_2 + R_3 + R_4}$$

ANS:: (a) $R_1 + R_2 + R_3$, (b) $\frac{R_1 R_2 + R_3(R_1 + R_2)}{R_1 + R_2}$ (c) $\frac{R_1(R_2 + R_3)}{R_1 + R_2 + R_3}$ (d) $\frac{R_1 R_2}{R_1 + R_2} + \frac{R_3 R_4}{R_3 + R_4}$ (e) $\frac{(R_1 + R_2)(R_3 + R_4)}{R_1 + R_2 + R_3 + R_4}$

Exercise 2.6 In the circuit in Figure 2.9, v, i, and R_1 are known. Find R_2.

$$v = 5V$$

$$i = 40\mu A$$

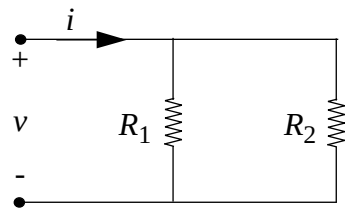


Figure 2.9:

$$R_1 = 150k\Omega$$

Solution:

KCL:

$$i + \frac{0-V}{R_1} + \frac{0-V}{R_2} = 0$$

$$R_2 = 750k\Omega$$

ANS:: 750 k Ω

Exercise 2.7 In the circuit in Figure 2.10, $v_o = 6V$, $R_1 = 100\Omega$, $R_2 = 25\Omega$, and $R_3 = 50\Omega$. Which of the resistors if any, are dissipating less than 1/4 watt?

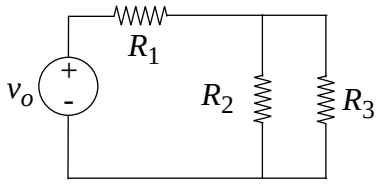


Figure 2.10:

Solution:

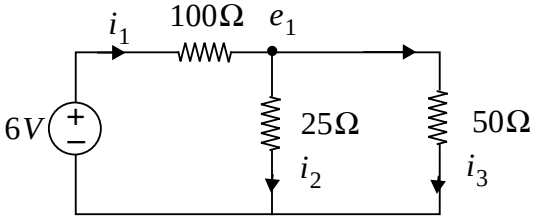


Figure 2.11:

KCL:

$$\frac{(6V - e_1)}{100\Omega} + \frac{(0 - e_1)}{25\Omega} + \frac{(0 - e_1)}{50\Omega} = 0$$

$$e_1 = \frac{6}{7} volts$$

$$i_1 = \frac{6V - e_1}{100\Omega} = 0.05143A$$

$$i_2 = \frac{e_1 - 0}{25\Omega} = 0.03429A$$

$$i_3 = \frac{e_1 - 0}{50\Omega} = 0.01714A$$

Power in 100Ω resistor $= \mathbb{P}(100)$

$$\mathbb{P}(100) = {i_1}^2 \cdot 100 = 0.264\ watts$$

$$\mathbb{P}(25) = {i_2}^2 \cdot 25 = 0.0294\ watts$$

$$\mathbb{P}(50) = {i_3}^2 \cdot 50 = 0.0147\ watts$$

R_2 and R_3 dissipate less than $1/4$ watt of power.

ANS:: R_2 and R_3

Exercise 2.8 Sketch the i-v characteristics for the networks in Figure 2.12. Label intercepts and slopes.

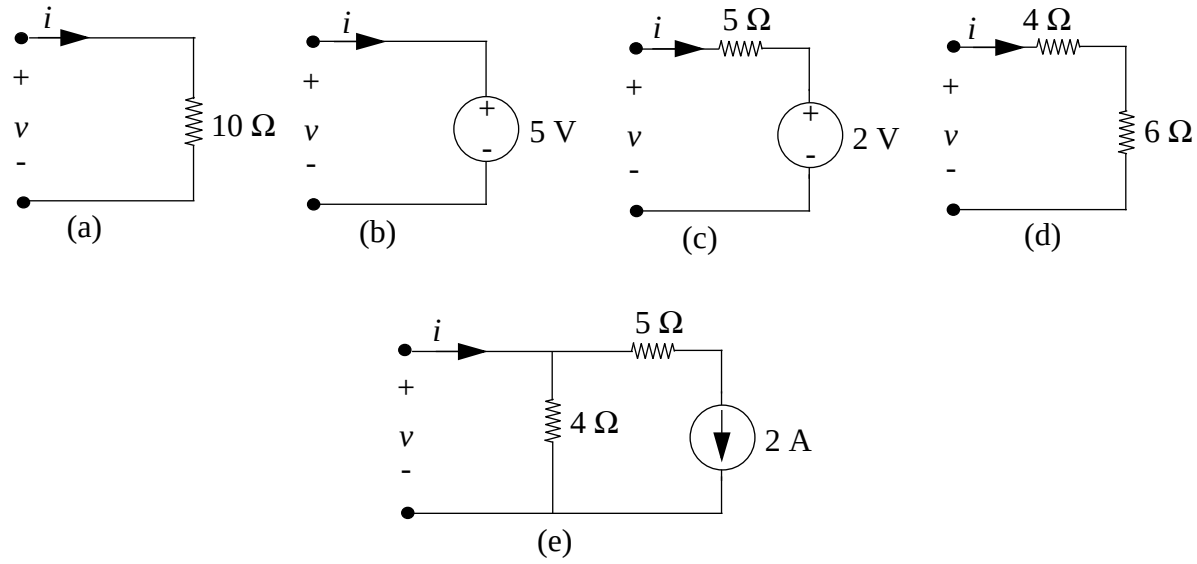


Figure 2.12:

Solution:

a) See Figure 2.13

$$v = i(10)$$

$$i = \frac{1}{10}v$$

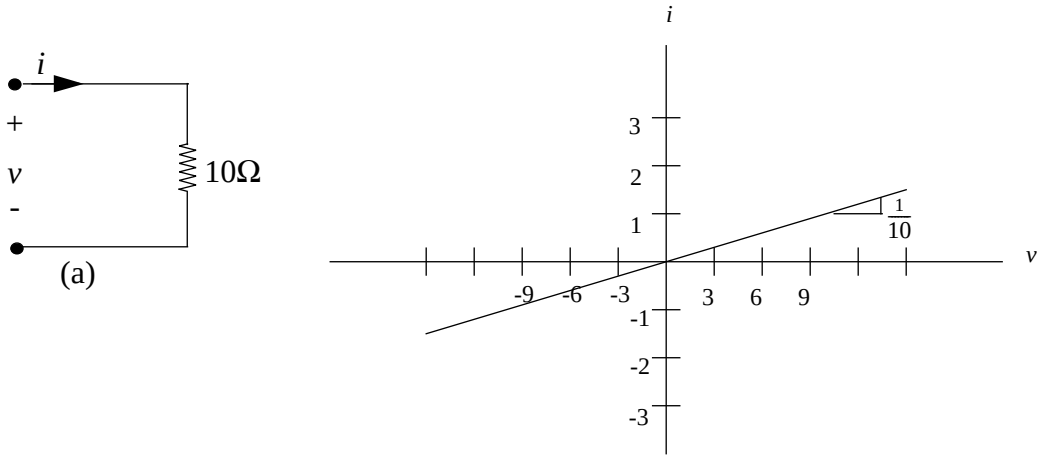


Figure 2.13:

b) See Figure 2.14

$$v = 5$$

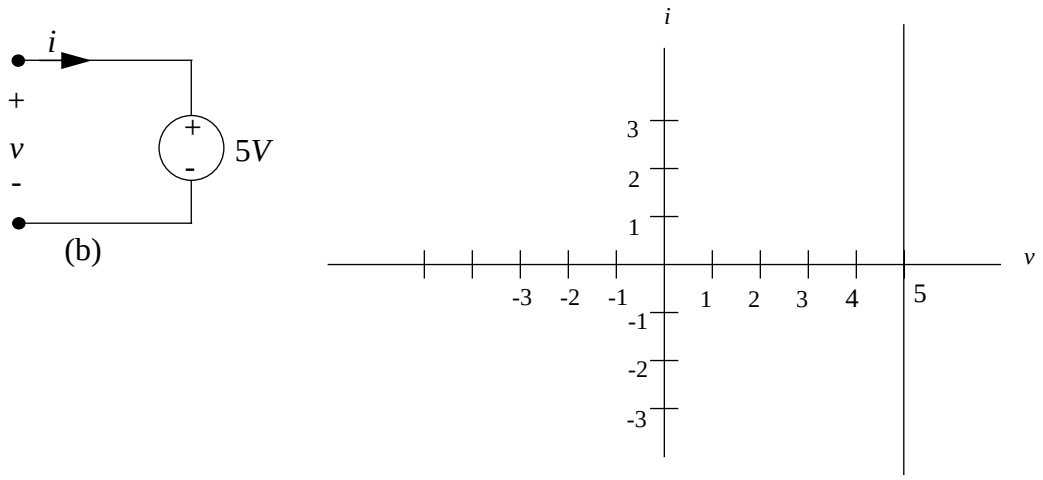


Figure 2.14:

c) See Figure 2.15

$$v = 5i + 2$$

$$i = \frac{1}{5}v - \frac{2}{5}$$

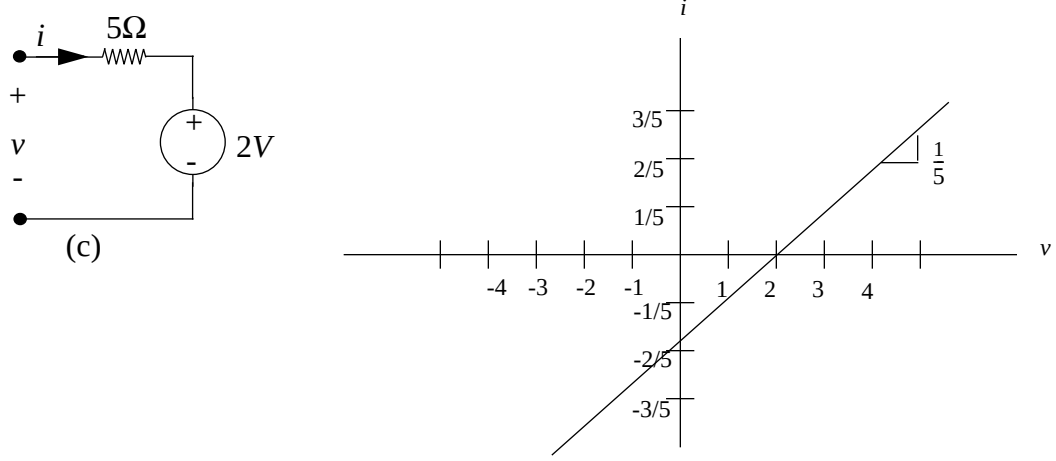


Figure 2.15:

d) See Figure 2.16

$$v = 10i$$
$$i = \frac{1}{10}v$$

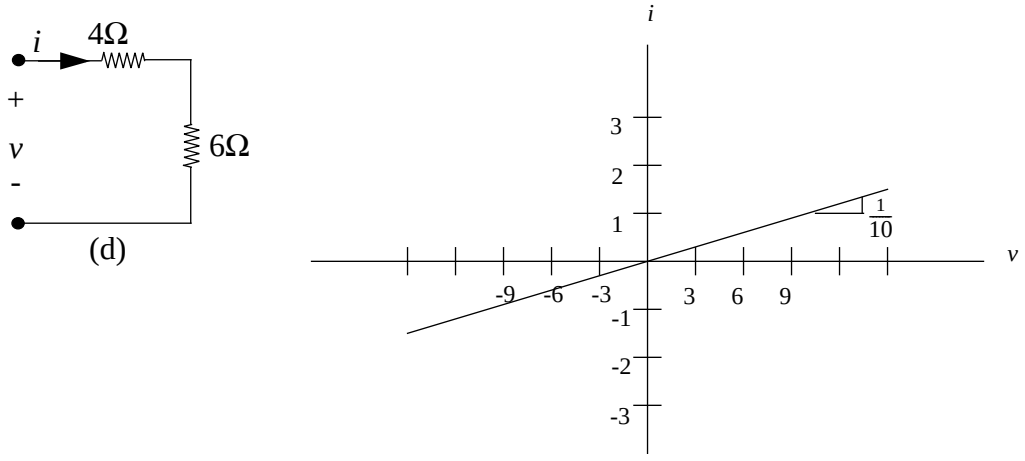


Figure 2.16:

e) See Figure 2.17

$$i = (v/4) + (v/5 + 2)$$
$$i = \frac{9}{20}v + 2$$

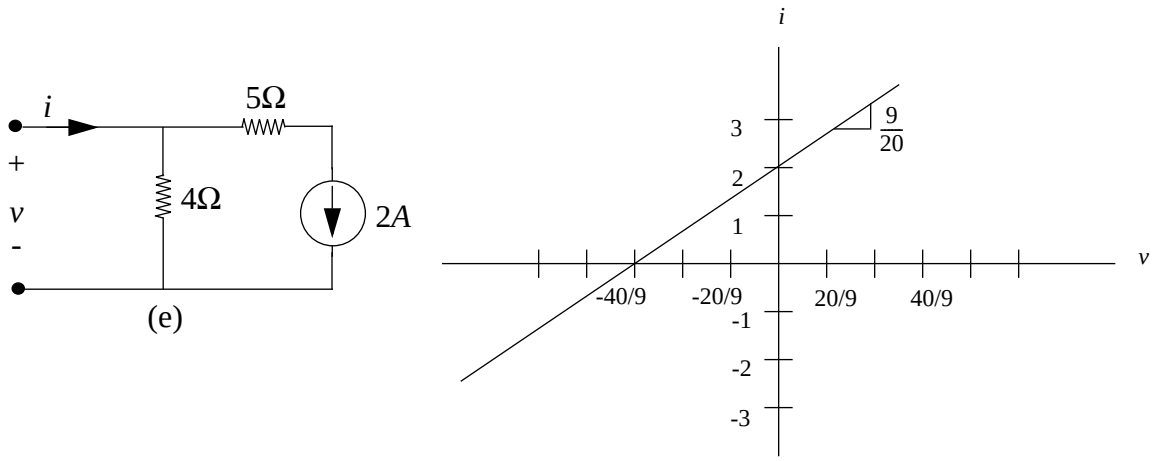


Figure 2.17:

Exercise 2.9 a) Assign branch voltages and branch current variables to each element in the network in Figure 2.18. Use associated reference directions.

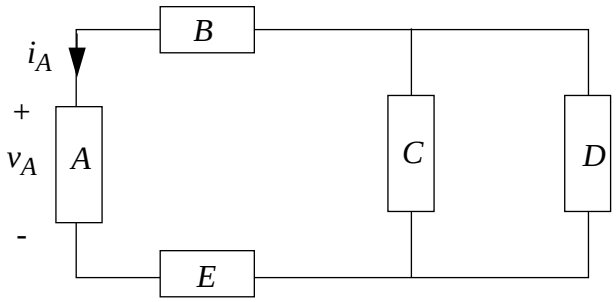


Figure 2.18:

b) How many linearly independent KVL equations can be written for this network?

c) How many linearly independent KCL equations can be written for this network?

d) Formulate a set of KVL and KCL equations for the network.

e) Assign non-zero numbers to each branch current such that your KCL equations are satisfied

f) Assign non-zero numbers to each branch voltage such that your KVL equations are satisfied.

g) As a check on your result, you can draw on the fact that power is conserved in a network that obeys KVL and KCL. Therefore calculate the quantity $\sum v_n i_n$. It should be zero.

Solution:

a) See Figure 2.19.

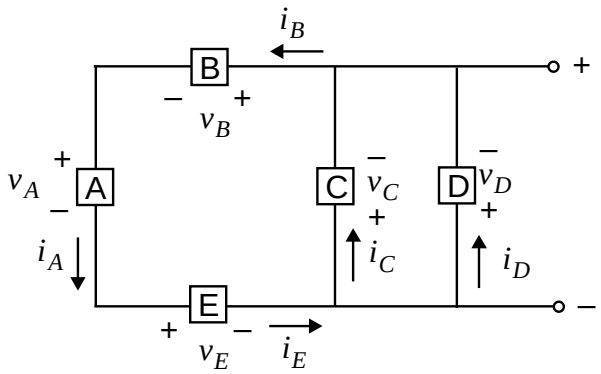


Figure 2.19:

b) 2

c) 3

d) KVL:

(1)

$$V_A + V_E + V_C + V_B = 0$$

(2)

$$V_C - V_D = 0$$

KCL:

(1)

$$i_B - i_C - i_D = 0$$

(2)

$$i_A - i_B = 0$$

(3)

$$-i_A + i_E = 0$$

e) Satisfy KCL:

$i_A = i_B = i_E = .2A \qquad i_C = 1A \qquad i_D = -0.8A$

f) Satisfy KVL:

$V_D = -2V, \qquad V_C = -2V$

$V_E = 2V, \qquad V_B = 1V$

$V_A = -1V$

g) Power conservation:

$\Sigma\, i_n V_n = 0$

$$i_E V_E + i_A V_A + i_B V_B + i_C V_C + i_D V_D = 0$$

Check:

$$0.2 \times 2 + 0.2 \times (-1) + 0.2 \times 1 + 1 \times (-2) + (-0.8)(-2) = 0V$$

$$0 = 0V \quad \text{so, correct}$$

ANS:: (b) 2 (c) 3 (d) (Depending on your assignment of branch variables, your answer may be different). KVL: $V_A + V_E + V_C + V_B = 0$, $V_C - V_D = 0$ KCL: $i_B - i_C - i_D = 0$, $i_A - i_B = 0$, $-i_A + i_E = 0$ (e) $i_A = i_B = i_E = .2A \qquad i_C = 1A \qquad i_D = -0.8A$ (f) $V_D = -2V$, $V_C = -2V$, $V_E = 2V$, $V_B = 1V$, $V_A = -1V$

Exercise 2.10 A portion of a larger network is shown in Figure 2.20. Show that the algebraic sum of the currents into this portion of the network must be zero.

Solution:

Prove: $i_A + i_B + i_C = 0$

Use KCL at node A (X is a fraction of i_C that flows to the left at node B):

$$i_B + X i_C + i_A + (1 - X)\, i_C = 0$$

$$i_A + i_B + i_C = 0$$

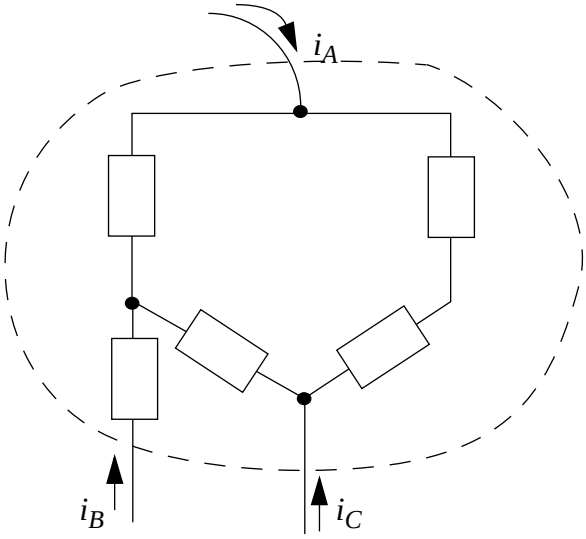


Figure 2.20:

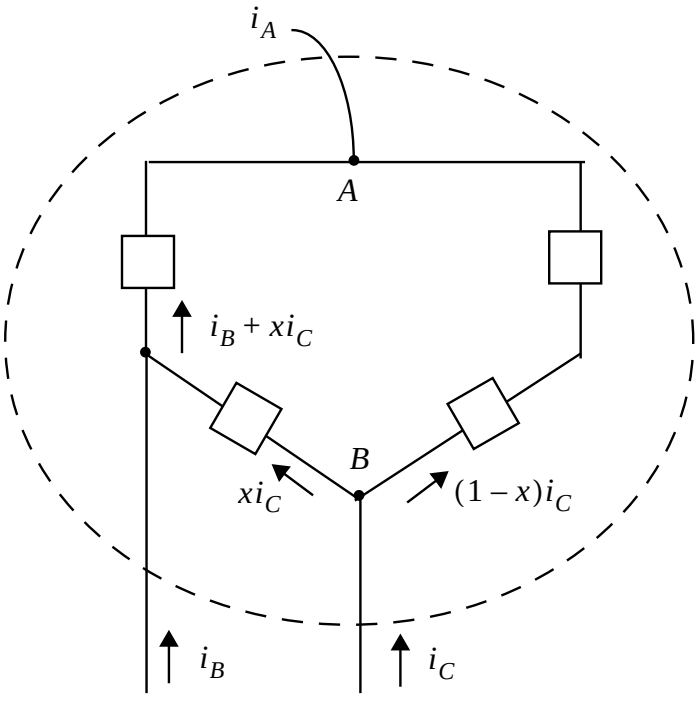


Figure 2.21:

Problems

Problem 2.1 A pictorial diagram for a flashlight is shown in Figure 2.22. The two batteries are identical, and each has an open-circuit voltage of 1.5 volts. The lamp has a resistance of 5Ω when lit. With the switch closed, 2.5 volts is measured across the lamp. What is the internal resistance of each battery?

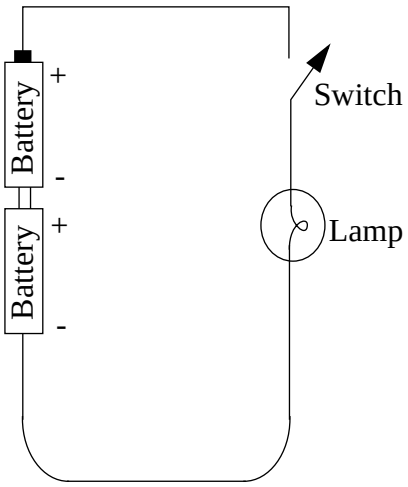


Figure 2.22:

Solution:

Redraw circuit:

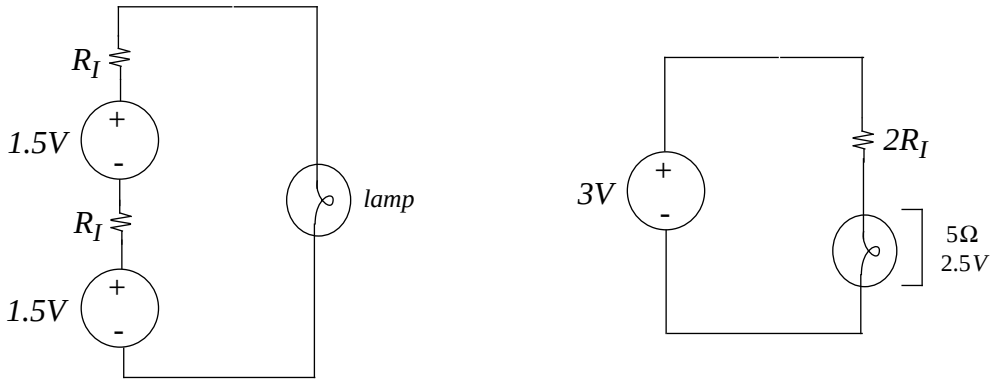


Figure 2.23:

Use a voltage divider relation to find R_I:

$$\frac{R_{lamp}}{R_{lamp}+2R_I}\cdot 3V = 2.5V$$

$$\frac{5}{5+2R_I}\cdot 3V = 2.5V$$

$$R_I = 0.5\Omega$$

ANS:: 0.5Ω

Problem 2.2 Determine the current i_0 in the circuit in Figure 2.24 by working with resistors in series and parallel.

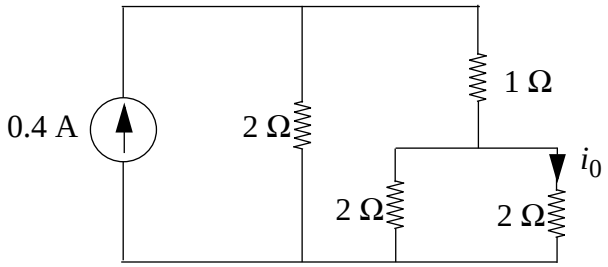


Figure 2.24:

Solution:

The circuit simplifies to 2Ω in parallel with 2Ω. The current divides into 0.2A for each branch. On the right branch, the current divides evenly again among the 2Ω resistors. So $i_0 = 0.1A$.

ANS:: 0.1A

Problem 2.3 Find the resistance between nodes A and B in Figure 2.25. All resistors equal 1Ω.

Solution:

One possible way to solve this problem is by using vertical symmetry. The current going in and out of the radial branches must be equal in magnitude. In fact, the radial resistors may be detached from the middle node completely. The circuit simplifies to $\frac{8}{3}\Omega$, $\frac{8}{3}\Omega$, and 2Ω all in parallel. Resulting resistance is $= \frac{4}{5}\Omega$.

See example 4 in section 1.5 for an alternative approach also using symmetry.

ANS:: $\frac{4}{5}\Omega$

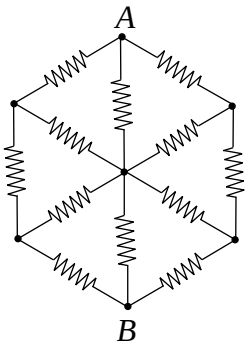


Figure 2.25:

Problem 2.4 For the circuit in Figure 2.26, find values of R_1 to satisfy each of the following conditions:

a) v = 3 V

b) v = 0 V

c) i = 3 A

d) The power dissipated in R_1 is 12 watts.

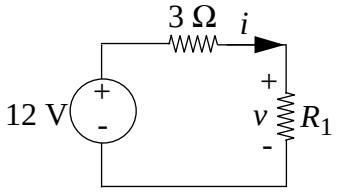


Figure 2.26:

Solution:

a) Voltage divider. Solve $12V * \frac{R_1}{3+R_1} = 3V$
$R_1 = 1\Omega$

b) $v = i * R_1$. Since the current is not 0, the resistance must be zero.
$R_1 = 0$

c) Solve $i = 3A = \frac{12V}{R_{eq}} = \frac{12V}{3\Omega+R_1}$
$R_1 = 1\Omega$

d) Power dissipated in $R_1 = 12W = i * v$ where $v = 12V * \frac{R_1}{3+R_1}$ and $i = \frac{12V}{3+R_1}$.
$R_1 = 3\Omega$

ANS:: (a) $R_1 = 1\Omega$ (b) $R_1 = 0$ (c) $R_1 = 1\Omega$ (d) $R_1 = 3\Omega$

Problem 2.5 Find the equivalent resistance R_T at the indicated terminals for each of the networks in Figure 2.27.

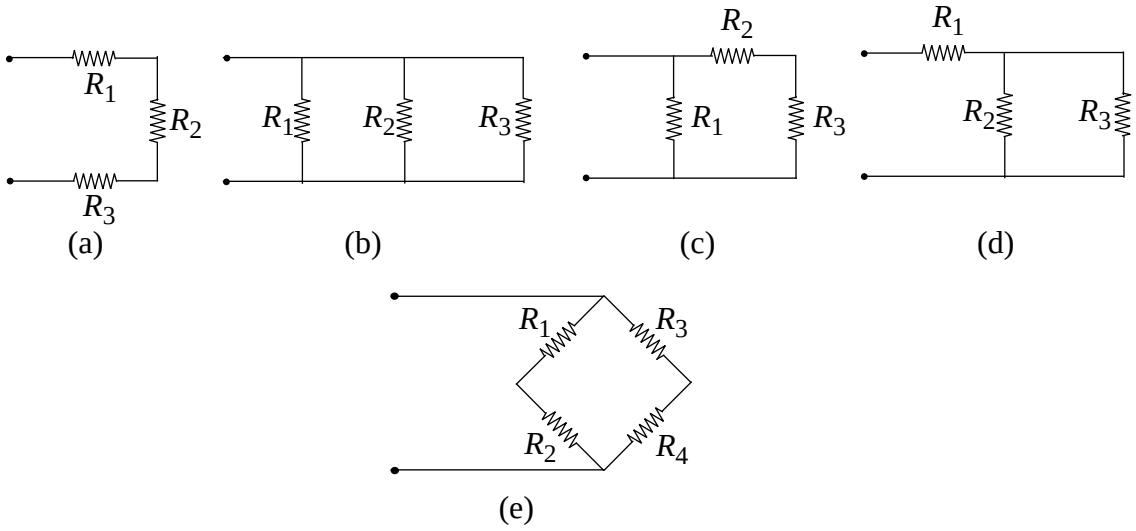


Figure 2.27:

Solution:

a) $R_T = R_1 + R_2 + R_3$

b) $R_T = \frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}}$
$R_T = \frac{R_1 R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}$

c) $R_T = \frac{1}{\frac{1}{R_2+R_3}+\frac{1}{R_1}}$
$R_T = \frac{R_1 R_2 + R_1 R_3}{R_1 + R_2 + R_3}$

d) $R_T = R_1 + \frac{R_2 R_3}{R_2 + R_3}$

e) $R_T = \frac{1}{\frac{1}{R_1+R_2}+\frac{1}{R_3+R_4}}$
$R_T = \frac{R_1 R_3 + R_1 R_4 + R_2 R_3 + R_2 R_4}{R_1 + R_2 + R_3 + R_4}$

ANS:: (a) $R_T = R_1 + R_2 + R_3$ (b) $R_T = \frac{R_1 R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}$ (c) $R_T = \frac{R_1 R_2 + R_1 R_3}{R_1 + R_2 + R_3}$ (d) $R_T = R_1 + \frac{R_2 R_3}{R_2 + R_3}$ (e) $R_T = \frac{R_1 R_3 + R_1 R_4 + R_2 R_3 + R_2 R_4}{R_1 + R_2 + R_3 + R_4}$

Problem 2.6 In each network in Figure 2.28, find the *numerical* values of the indicated variables (Units are Amperes, Volts and Ohms).

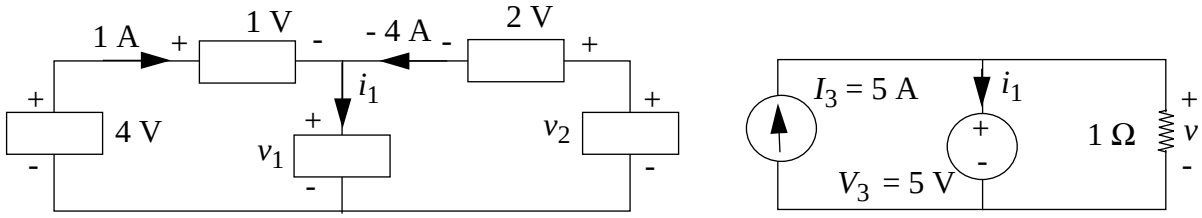


Figure 2.28:

Solution:

Top figure, $v_1 = 4V - 1V = 3V$, $v_2 = 3V + 2V = 5V$, $i_1 = -3A$

Bottom figure, since 5V is in parallel across the 1Ω resistor, all 5A of I_3 go through the resistor. $v = 5V, i_1 = 0A$

Top: $v_1 = 3V, v_2 = 5V, i_1 = -3A$, Bottom: $v = 5V, i_1 = 0A$.

ANS:: Top: $v_1 = 3V, v_2 = 5V, i_1 = -3A$, Bottom: $v = 5V, i_1 = 0A$.

Problem 2.7 For the circuit in Figure 2.29, determine the current i_3 explicitly in terms of all circuit parameters.

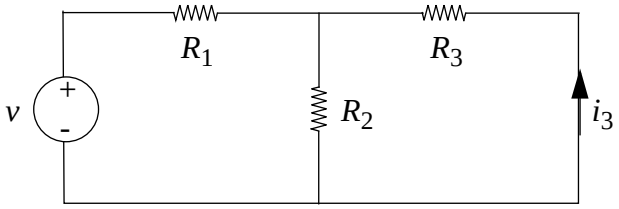


Figure 2.29:

Solution:

$R_T = R_1 + \frac{R_2 R_3}{R_2 + R_3}$

$i_T = \frac{v}{R_T} = \frac{v(R_2 + R_3)}{R_1 R_2 + R_1 R_3 + R_2 R_3}$

$i_3 = -i_T * \frac{R_2}{R_2 + R_3}$

$i_3 = -\frac{v R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3}$

ANS:: $i_3 = -\frac{v R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3}$

Problem 2.8 Determine explicitly the voltage v_3 in the circuit in Figure 2.30.

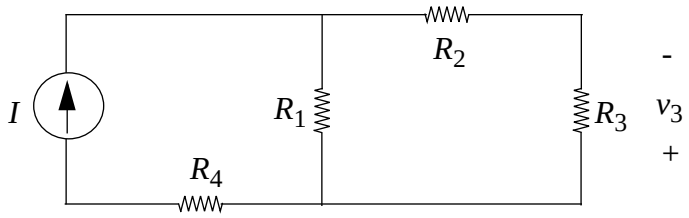


Figure 2.30:

Solution:

$R_T = R_4 + \frac{R_1R_2+R_1R_3}{R_1+R_2+R_3}$

Voltage across current source is not zero. $V_T = I * (R_4 + \frac{R_1R_2+R_1R_3}{R_1+R_2+R_3})$

Using voltage divider, $-v_3 = IR_T * \frac{\frac{R_1R_2+R_1R_3}{R_1+R_2+R_3}}{R_T} * \frac{R_3}{R_2+R_3}$

$v_3 = -I * \frac{R_1R_2+R_1R_3}{R_1+R_2+R_3} * \frac{R_3}{R_2+R_3}$

ANS:: $v_3 = -I * \frac{R_1R_2+R_1R_3}{R_1+R_2+R_3} * \frac{R_3}{R_2+R_3}$

Problem 2.9 Calculate the power dissipated in the resistor R in Figure 2.31.

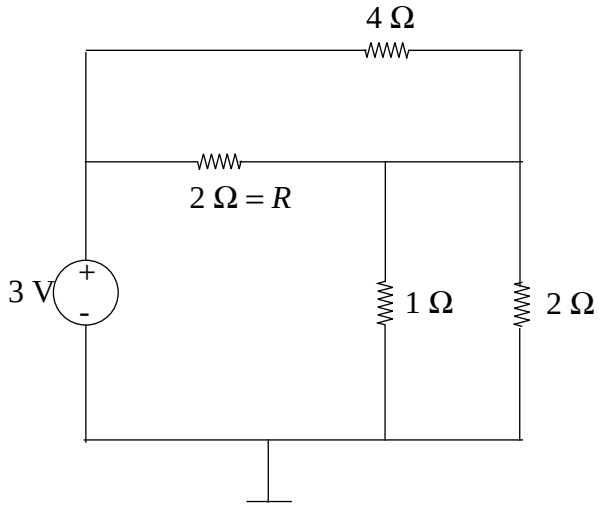


Figure 2.31:

Solution:

The equivalent resistance is 2Ω, so $\frac{3}{2}A$ of current is split between the 2Ω and 4Ω resistors. Therefore, $1A$ current goes through R.

Power $= 2W$

ANS:: Power $= 2W$

Problem 2.10 Design a resistor attenuator to make $v_o = v_i/1000$, using the circuit configuration given in Figure 2.32, and resistor values available in your lab. This problem is underconstrained so has many answers.

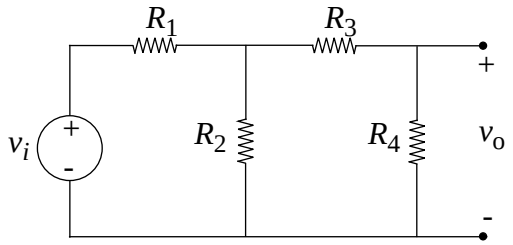


Figure 2.32:

Solution:

Here is one possibility with the resistors available in lab kits.

$R_1 = 220k\Omega$, $R_2 = 560\Omega$, $R_3 = 340\Omega = 330\Omega + 10\Omega$, $R_4 = 220\Omega$

ANS:: $R_1 = 220k\Omega$, $R_2 = 560\Omega$, $R_3 = 340\Omega = 330\Omega + 10\Omega$, $R_4 = 220\Omega$

Problem 2.11 Consider the network in Figure 2.33 in which a non-ideal battery drives a load resistor R_L. The battery is modeled as a voltage source V_S in series with a resistor R_S. The following are some proofs about power transfer.

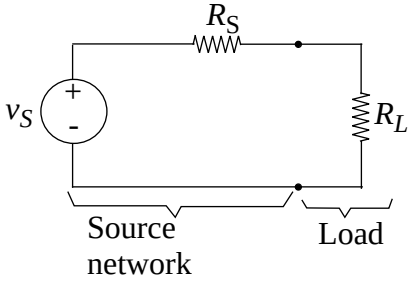


Figure 2.33:

a) Prove that for R_S variable and R_L fixed, the power dissipated in R_L in maximum when $R_S = 0$.

b) Prove that for R_S fixed and R_L variable, the power dissipated in R_L is maximum when $R_S = R_L$ (“matched resistances”).

c) Prove that for R_S fixed and R_L variable, the condition that maximizes the power delivered to the load R_L requires that an equal amount of power be dissipated in the source resistance R_S.

Solution:

a) Power dissipated in resistor R_L:

$$P = I_{circuit}^2 R_L$$
$$P = \frac{V_S^2}{(R_S + R_L)^2} R_L$$

$$P|_{R_S=0} = \frac{V_S^2}{(0 + R_L)^2} R_L = \frac{V_S^2}{R_L}$$
$$lim_{R_S \to \infty} \frac{V_S^2}{(R_S + R_L)^2} R_L = 0$$

So, power dissipated in R_L maximum when $R_S = 0$. Otherwise power in R_L decreases as R_S increases.

b)

$$P = I_{circuit}^2 R_L$$
$$P = \frac{V_S^2}{(R_S + R_L)^2} R_L$$

Maximize with respect to R_L:

$$\frac{dP}{dR_L} = \frac{(R_S + R_L)^2(V_S^2) - (V_S^2 R_L)(2(R_S + R_L))}{(R_S + R_L)^4} = 0$$
$$\frac{V_S^2}{(R_S + R_L)^2} = \frac{2V_S^2 R_L}{(R_S + R_L)^3}$$
$$(R_S + R_L)V^2 = 2V^2 R_L$$
$$\rightarrow R_S = R_L \text{ (when this holds power maximized in } R_L)$$

c) Maximum power in circuit is dissipated when $R_S = R_L$:

$$P(R_L) = \frac{V_S^2}{(R_S + R_L)^2} R_L$$

$$P_{circuit} = \frac{V^2}{(R_S + R_L)^2}$$

$$P(R_L = R_S) = \frac{V_S^2}{4R_S}$$

$$P_{RS} = P_{circuit} - P_{R_L = R_S}$$

$$P_{RS} = \underbrace{\frac{V^2}{R_S + R_L}}_{R_S = R_L} - \frac{V^2}{4R_S} = \frac{V^2}{2R_S} - \frac{V^2}{4R_S} = \frac{V^2}{4R_S}$$

Problem 2.12 Sketch the v-i characteristics for the networks in Figure 2.34. Label intercepts and slopes.

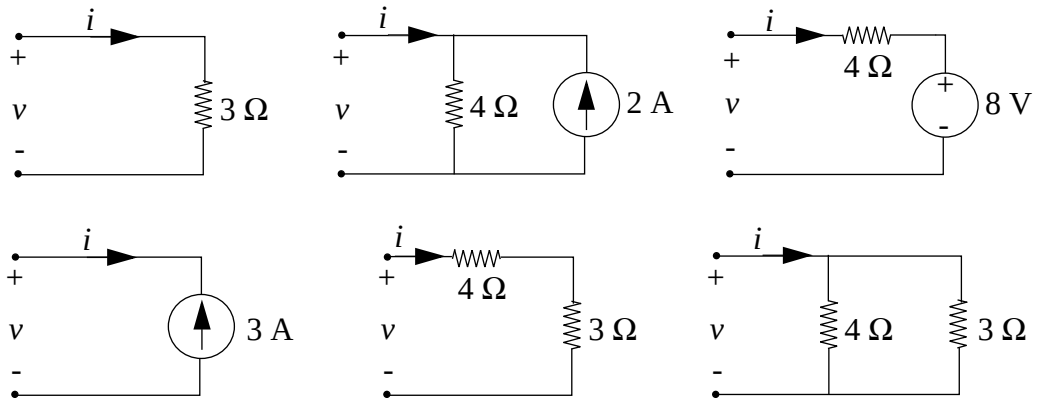


Figure 2.34:

Solution:

a) See Figure 2.35

$$v = 3i$$

$$i = \frac{v}{3}$$

b) See Figure 2.36

$$v = 4(i + 2)$$

$$i = \frac{v}{4} - 2$$

c) See Figure 2.37

$$v = 4i + 8$$

$$i = \frac{(v - 8)}{4} = \frac{v}{4} - 2$$

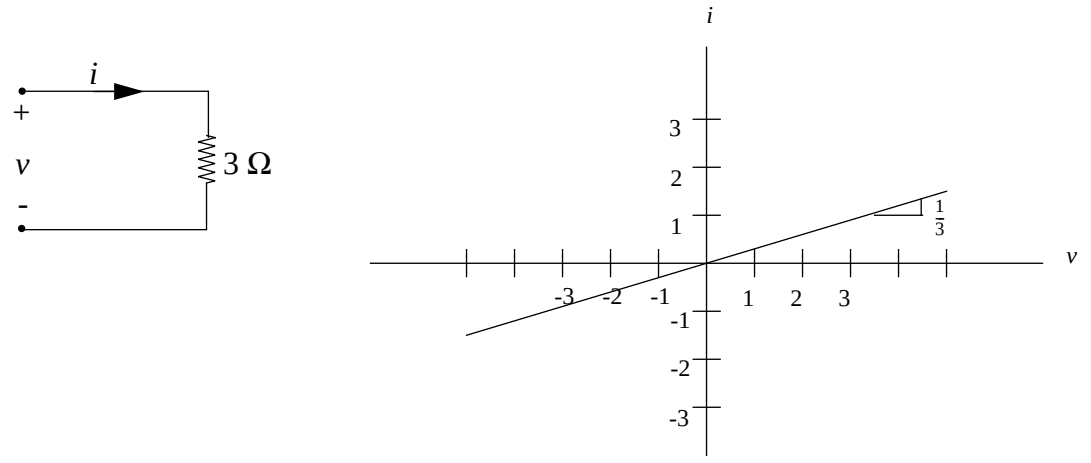


Figure 2.35:

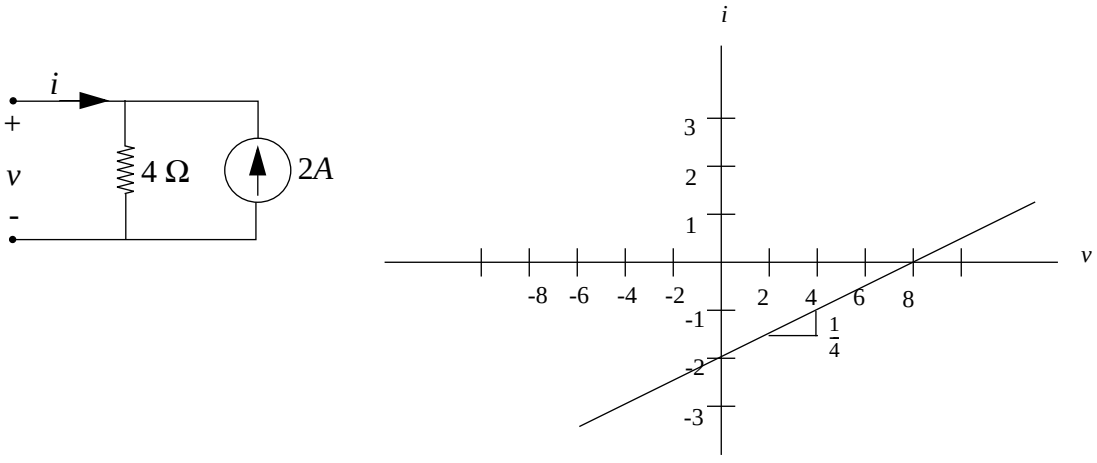


Figure 2.36:

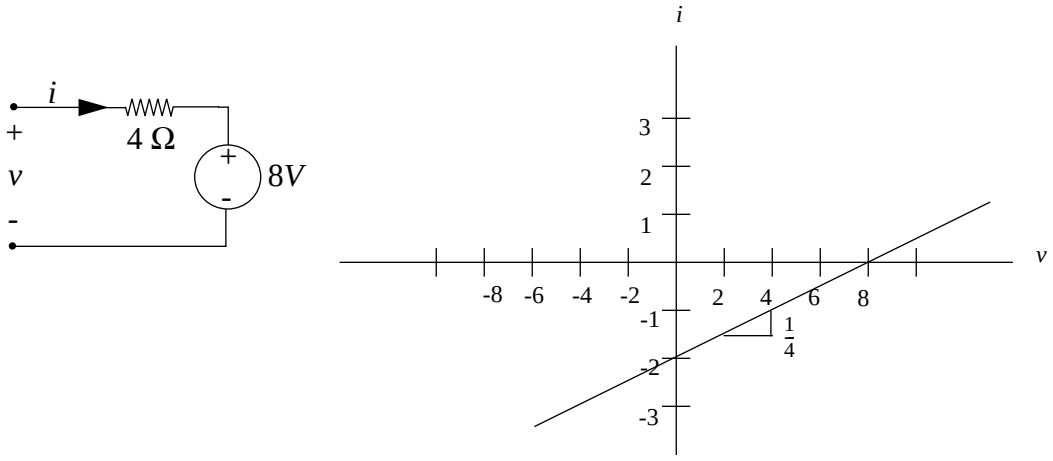


Figure 2.37:

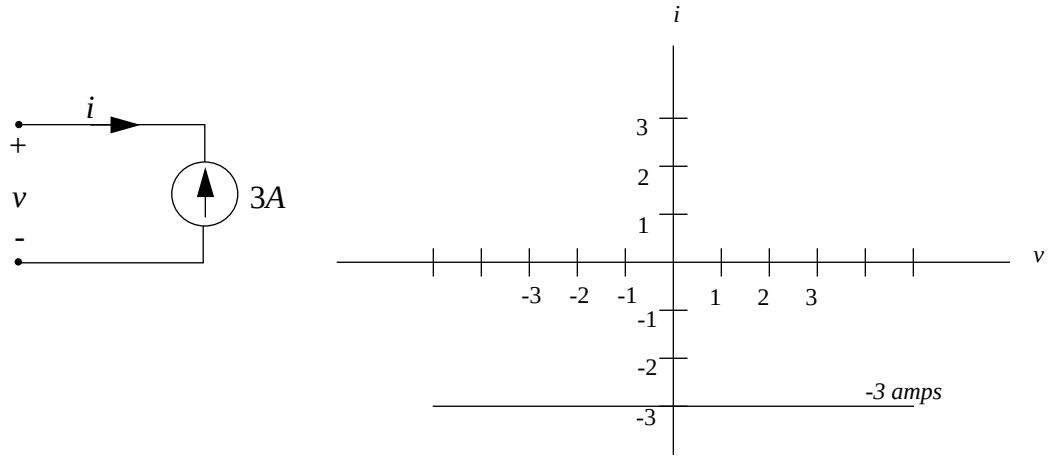


Figure 2.38:

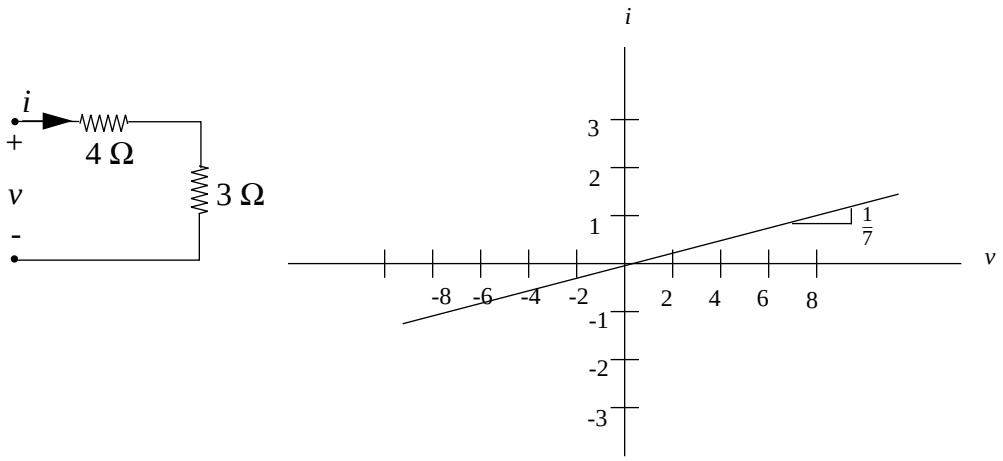


Figure 2.39:

d) See Figure 2.38

e) See Figure 2.39

$$v = 7i$$

$$i = \frac{v}{7}$$

f) See Figure 2.40

$$v = \frac{R_1 R_2}{R_1 + R_2} \cdot i = \frac{12}{7} i$$

$$i = \frac{7}{12} v$$

Problem 2.13

a) Find i_1, i_2, and i_3 in the network in Figure 2.41. (Note that i_3 does not obey the standard convention for current direction).

b) Show that energy is conserved in this network.

Solution:

a) An easy way to do this problem is by superposition.

$$i_1 = \frac{v_A R_2 + v_A R_3 - v_B R_2}{R_1 R_2 + R_2 R_3 + R_1 R_3}$$

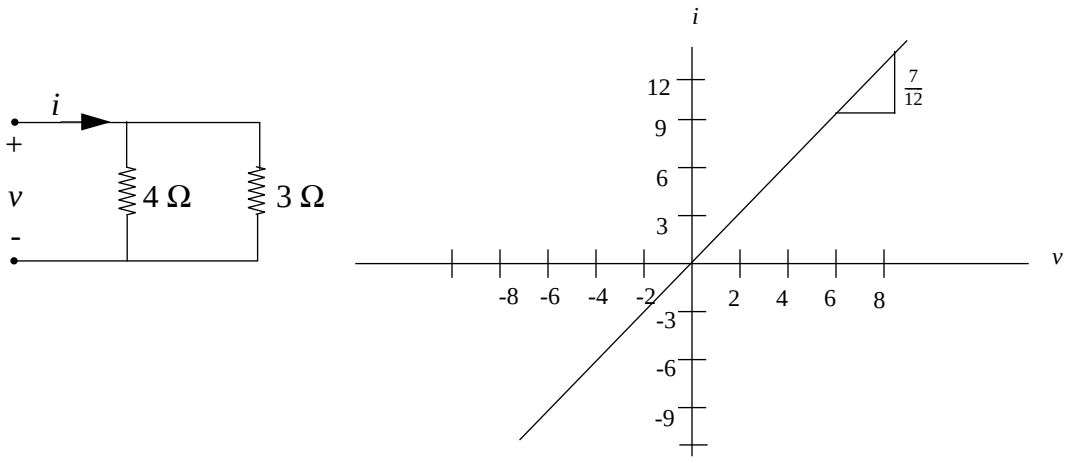


Figure 2.40:

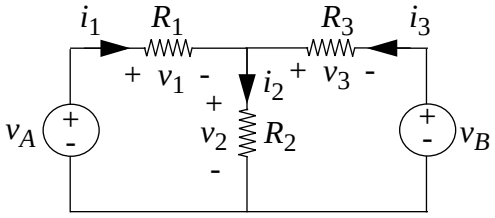


Figure 2.41:

$$i_2 = \frac{v_A R_3 + v_B R_1}{R_1 R_2 + R_2 R_3 + R_1 R_3}$$

$$i_3 = \frac{v_B R_2 + v_B R_1 - v_A R_2}{R_1 R_2 + R_2 R_3 + R_1 R_3}$$

b) KVL and KCL imply:

$$v_2 + v_1 = v_A \tag{2.1}$$
$$v_2 + v_3 = v_B \tag{2.2}$$
$$i_1 + i_3 = i_2 \tag{2.3}$$

We wish to show that

$$v_A i_1 + v_B i_3 \stackrel{?}{=} i_1 v_1 + i_2 v_2 + i_3 v_3$$

substitute (3) for i_2

$$\Rightarrow v_A i_1 + v_B i_3 \stackrel{?}{=} i_1 v_1 + (i_1 + i_3) v_2 + i_3 v_3$$

rearrange

$$\Rightarrow v_A i_1 + v_B i_3 \stackrel{?}{=} (v_1 + v_2) i_1 + (v_2 + v_3) i_3$$

substitute (1) and (2)

$$\Rightarrow v_A i_1 + v_B i_3 \stackrel{\surd}{=} v_A i_1 + v_B i_3$$

Note: Power and, more generally, any sum of products of currents and voltages will always be zero. Note that we did *not* use any information other than KVL and KCL. The currents and voltages don't even have to belong to the same network. This powerful theorem is known as *Tellegen's Theorem*.

ANS:: (a) $i_1 = \frac{v_A R_2 + v_A R_3 - v_B R_2}{R_1 R_2 + R_2 R_3 + R_1 R_3}$, $i_2 = \frac{v_A R_3 + v_B R_1}{R_1 R_2 + R_2 R_3 + R_1 R_3}$, $i_3 = \frac{v_B R_2 + v_B R_1 - v_A R_2}{R_1 R_2 + R_2 R_3 + R_1 R_3}$

Problem 2.14 Assume that you have an arbitrary network of passive two-terminal resistive elements in which the i-v characteristic of each element does not touch either the v-axis or the i-axis, except that each i-v characteristic passes through the origin. Prove that all branch currents and branch voltages in the network are zero.

Solution:

Assume that there is a voltage across any element. Therefore, since the v-i characteristic is such that it intersects the axes at only the origin, there is a current through that element. The element thus consumes power. Due to the conservation of power rule, some element must be producing that power. This contradicts the assumption that all the elements are passive. Therefore there cannot be any voltage across any element, and consequently no current through any element either.

Problem 2.15 Solve for the voltage across resistor R_4 in the circuit in Figure 2.42 by assigning voltage and current variables for each resistor.

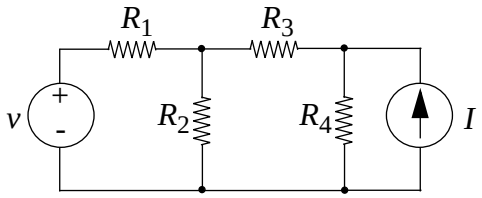


Figure 2.42:

Solution:

Label currents and voltages (see Figure 2.43).

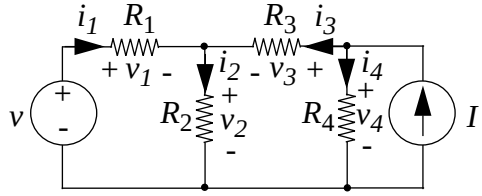


Figure 2.43:

From KCL:

1) $i_2 = i_1 + i_3$

2) $I = i_3 + i_4$

From KVL:

3) $-v + v_1 + v_2 = 0$

4) $v_3 - v_4 + v_2 = 0$

From Ohm's Law:

5) $v_1 = i_1 R_1$

6) $v_2 = i_2 R_2$

7) $v_3 = i_3 R_3$

8) $v_4 = i_4 R_4$

Solving for v_4, the voltage across R_4:

$$v_4 = \frac{vR_2R_4 + IR_1R_2R_4 + IR_1R_3R_4 + IR_2R_3R_4}{R_1R_2 + R_1R_3 + R_1R_4 + R_2R_3 + R_2R_4}$$

ANS:: $v_4 = \frac{vR_2R_4+IR_1R_2R_4+IR_1R_3R_4+IR_2R_3R_4}{R_1R_2+R_1R_3+R_1R_4+R_2R_3+R_2R_4}$

Problem 2.16 Find the potential difference between each of the lettered nodes (A, B, C, and D) in Figure 2.44 and ground. All resistances are in ohms.

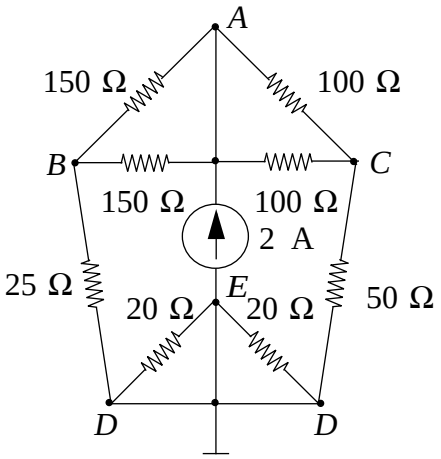


Figure 2.44:

Solution:

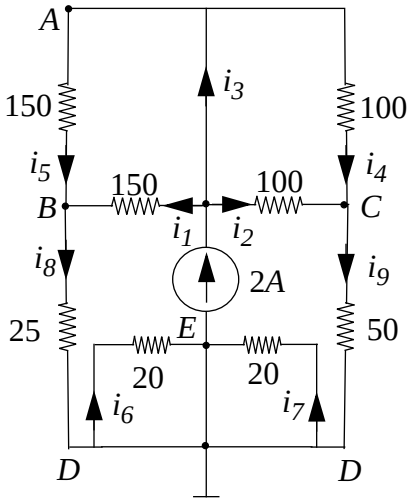


Figure 2.45:

Redraw circuit (see Figure 2.45)

From KCL:

1) $2A = i_1 + i_2 + i_3$

2) $i_3 = i_4 + i_5$

3) $i_8 = i_1 + i_5$

4) $i_9 = i_2 + i_4$

5) $2A = i_6 + i_7$

From KVL:

1) $20i_7 - 20i_6 = 0$

2) $150i_1 - 150i_5 = 0$

3) $100i_2 - 100i_4 = 0$

4) $150i_1 + 25i_8 - 50i_9 - 100i_2 = 0$

Solve for currents: $i_1 = \frac{1}{2}A$, $i_2 = \frac{1}{2}A$, $i_3 = 1$, $i_4 = \frac{1}{2}A$, $i_5 = \frac{1}{2}A$, $i_6 = 1$, $i_7 = 1$, $i_8 = 1$, $i_9 = 1$

Find voltages relative to ground (D):

$$v_{AD} = 150i_5 + 25i_8 = 150(\frac{1}{2}) + 25(1) = 100V$$

$$v_{BD} = 25i_8 = 25V$$

$$v_{CD} = 50i_9 = 50V$$

$$v_{ED} = 0V since the 20\Omega resistors are shorted.$$

ANS:: $v_{AD} = 100V$, $v_{BD} = 25V$, $v_{CD} = 50V$, $v_{ED} = 0V$

Problem 2.17 Find the voltage between node C and the ground node in Figure 2.46. All resistances are in ohms.

Solution:

Since the network to the right of the 25Ω resistor is not grounded, there is no loop for current to flow through it. Therefore, apply a voltage divider to the left loop:

$$v_{CD} = \frac{40\Omega}{40\Omega + 35\Omega + 85\Omega} 100V = 25V$$

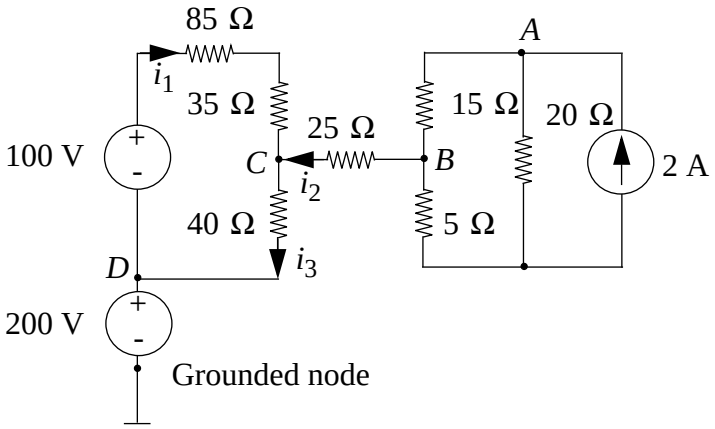


Figure 2.46:

Note that node D is at $200V$:

$$v_D = 200V \Rightarrow v_C = v_{CD} + v_D = 200V + 25V = 225V$$

ANS:: $v_C = 225V$

Chapter 3

Network Theorems

Exercises

Exercise 3.1 Write node equations for the network in Figure 3.1. Solve for the node voltages, and use these voltages to find the branch current i. To minimize errors and facilitate answer-checking, it is helpful to obtain literal expressions before substituting numerical values for the parameters.

$V = 2$ volts $\quad R_3 = 3\Omega \quad R_1 = 2\Omega \quad R_4 = 2\Omega \quad R_2 = 4\Omega \quad R_5 = 1\Omega$

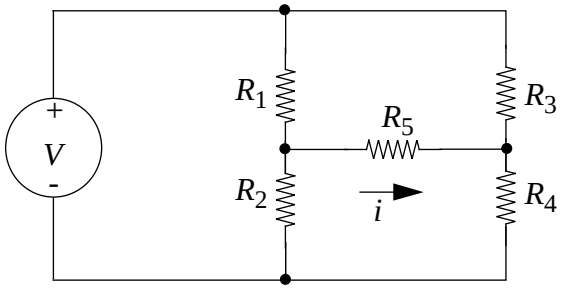


Figure 3.1:

Solution:

Node equations:

$$\frac{V - e_1}{R_1} + \frac{0 - e_1}{R_2} + \frac{e_2 - e_1}{R_5} = 0$$

$$\frac{V - e_2}{R_3} + \frac{0 - e_2}{R_4} + \frac{e_1 - e_2}{R_5} = 0$$

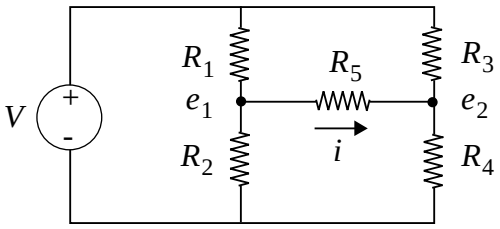


Figure 3.2:

Solving the above two equations,

$$e_1 = 1.13207\ V$$

$$e_2 = 0.98113\ V$$

$$i = \frac{e_1 - e_2}{R_5} = 0.15094\ A$$

$$i = \frac{8}{53}\ A$$

ANS:: 8/53 A

Exercise 3.2 Find the Norton equivalent at the indicated terminals for each network in Figure 3.3.

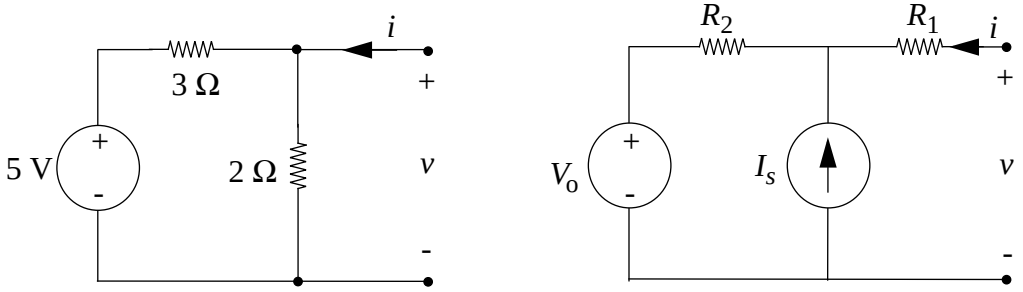


Figure 3.3:

Solution:

Left network:

$R_T = 3||2 = 1.2\ \Omega$ when $5\ V$ source is made a short circuit.

$I = 5/3\ A$ when the indicated terminals are connected with a wire ("shorted") since then no current flows through the $2\ \Omega$ resistor.

Right network:

$R_T = R_1 + R_2$, when the V_0 source is shorted and the I_S source is made an open circuit.

$$I = \underbrace{\frac{R_2}{R_1 + R_2}}_{\substack{\text{current}\\ \text{divider}\\ \text{for}\\ V_0 = 0}} \cdot I_S + \underbrace{\frac{V_0}{R_1 + R_2}}_{\substack{\text{contribution}\\ \text{from } V_0\\ \text{when } I_S = 0}} \quad \text{by superposition}$$

ANS:: Left: $1.2\Omega, 5/3A$, Right: $R_1 + R_2$, $\frac{R_2}{R_1+R_2} I_S + \frac{V_0}{R_1+R_2}$

Exercise 3.3 Find the Thévenin Equivalent for each network in Figure 3.4.

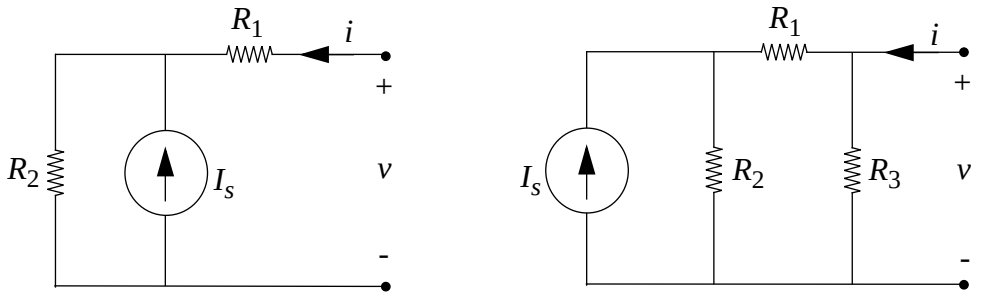


Figure 3.4:

Solution:

Left network:

$R_T = R_1 + R_2$ when I_S is made an open circuit.

$V_{OC} = I_S R_2$ since no current flows through R_1 in the open circuit case.

$R_T = R_3 || (R_1 + R_2)$ when I_S current source is made an open circuit.

Since $V_{OC} = R_3 \cdot$ (current through R_3) by Ohm's Law,

$$V_{OC} = \underbrace{\frac{I_S \cdot R_2}{R_1 + R_2 + R_3}}_{\text{current divider relation for fraction of } I_S \text{ that will flow through } R_1 \text{ and } R_3} \cdot R_3$$

ANS:: Left: $V_{OC} = I_S R_2, R_T = R_1 + R_2$, Right: $V_{OC} = \frac{I_S R_2 R_3}{R_1+R_2+R_3}, R_T = R_3||(R_1 + R_2)$

Exercise 3.4 Find v_0 in (a) and (b) by superposition in Figure 3.5.

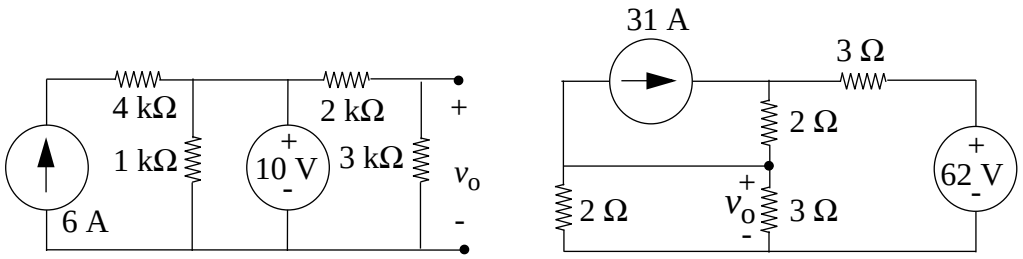


Figure 3.5:

Solution:

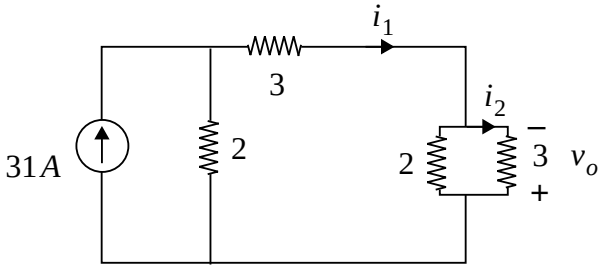


Figure 3.6:

(a):

1. Set voltage source to zero (short circuit):

$$v_0 = 0$$

2. Set current source to zero (open circuit):

$$v_0 = 10\ V \cdot \underbrace{\frac{3000}{3000 + 2000}}_{\text{voltage divider}}$$

$$v_0 = 6\ Volts$$

$$v_0 = 0 + 6V \text{ [superposition]}$$

$$v_0 = 6\ Volts$$

(b):

1. Set current source to zero (open circuit):

$$v_0 = \left[\underbrace{\frac{2 \parallel 3}{2 \parallel 3 + 2 + 3}}_{\text{voltage divider}}\right] \cdot 62\ V = 12\ Volts \text{ since } 2 \parallel 3 = 1.2$$

2. Set voltage source to zero (short circuit):

$$i_1 = 31\ A \left[\underbrace{\frac{2}{3 + 2 \parallel 3 + 2}}_{\text{current divider}}\right] = 10\ A$$

$$v_0 = 3 \cdot (-i_2) = -12\ Volts \qquad i_2 = \left[\frac{2}{3 + 2}\right] \cdot i_1 = 4\ A$$

$$v_0 = 12 + (-12) \quad \text{[superposition]}$$

$$v_0 = 0$$

ANS:: (a) 6V (b) 0V

Exercise 3.5 Use superposition to find the voltage v in the network in Figure 3.7.

Solution:

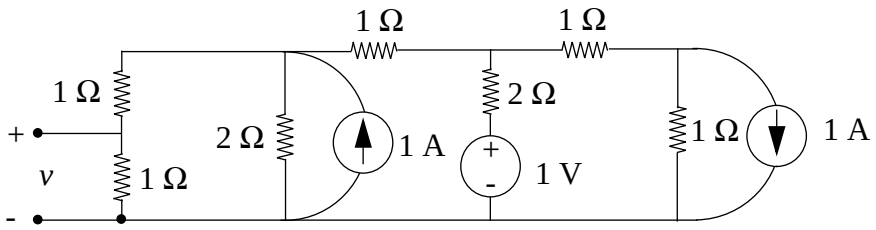


Figure 3.7:

$$V = \underbrace{\frac{1}{3}V}_{\substack{\text{from left}\\ \text{current}\\ \text{source}}} + \underbrace{\frac{1}{12}V}_{\substack{\text{from}\\ \text{voltage}\\ \text{source}}} + \underbrace{\left(-\frac{1}{12}\,V\right)}_{\substack{\text{from right}\\ \text{current}\\ \text{source}}} = \frac{1}{3}\,Volts$$

ANS:: 1/3V

Exercise 3.6 Determine (and label carefully) the Thévenin equivalent for the network in Figure 3.8.

$R_1 = 2k\Omega \quad R_2 = 1k\Omega \quad i_0 = 3\ \cos\omega t$ (in mA)

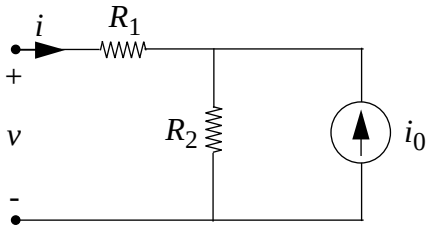


Figure 3.8:

Solution:

$V_{OC} = 3\ \cos\ \omega t$ [volts] since no current flows through R_1 in the open-circuit case.

$R_T = R_1 + R_2 = 3\ k\Omega$, when i_0 current source set to zero (open circuit)

ANS:: $V_{OC} = 3\ \cos\ \omega t$ volts, and $R_T = 3\ k\Omega$

Exercise 3.7 Determine and label carefully the Norton equivalent for the network in Figure 3.9.

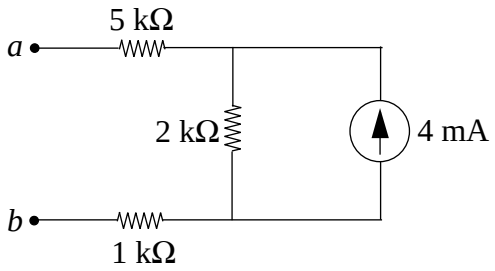


Figure 3.9:

Solution:

$$I_{SC} = \underbrace{\left[\frac{2k}{2k+5k+1k}\right]}_{\text{current divider}} \cdot 4\ mA = 1\ mA$$

$R_T = 5k + 2k + 1k = 8\ k\Omega$, when current source is "open-circuited"

ANS:: $I_{SC} = 1\ mA$, and $R_T = 8\ k\Omega$

Exercise 3.8 Find the Thévenin equivalent for the circuit at the terminals AA' in Figure 3.10.

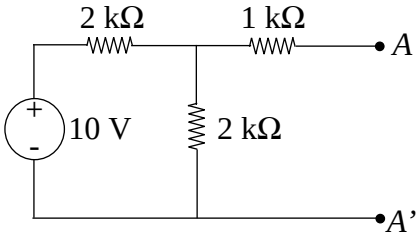


Figure 3.10:

Solution:

$R_T = 1k\Omega + 2k\Omega \,||\, 2k\Omega = 2k\Omega$ when voltage source is short-circuited.

$V_{OC} = 5\ Volts$, by voltage divider since no current flows through $1k\Omega$ resistor in the open-circuit case.

ANS:: $R_T = 2k\Omega$ and $V_{OC} = 5\ Volts$

Exercise 3.9 The resistive network shown in Figure 3.11 is excited by two voltage sources $v_1(t)$ and $v_2(t)$.

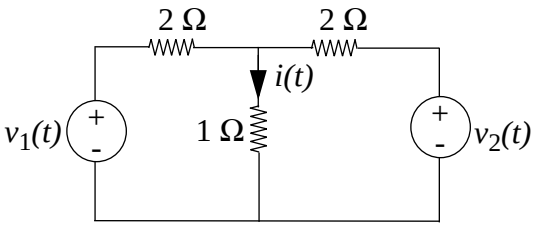


Figure 3.11:

a) Express the current $i(t)$ through the 1Ω resistor as a function of $v_1(t)$ and $v_2(t)$.

b) Determine the total energy dissipated in the 1Ω resistor due to both $v_1(t)$ and $v_2(t)$ from time T_1 to time T_2.

c) Derive the constraint between $v_1(t)$ and $v_2(t)$ such that the value for b) can be computed by adding the energies dissipated when each source acts alone (i.e. by superposition).

Solution:

a)

$$i(t) = \left[\frac{1 \mid\mid 2}{1 \mid\mid 2 + 2}\right](v_1(t) + v_2(t)) = \frac{1}{4}(v_1(t) + v_2(t))$$

b)

$$\text{Energy} = \frac{1}{16}\int_{T_1}^{T_2} (v_1(t) + v_2(t))^2 dt$$

c)

$$\text{For superposition to apply, } \int_{T_1}^{T_2} v_1 \cdot v_2 \cdot dt \equiv 0 \quad \text{[orthogonal]}$$

ANS:: (a) $i(t) = \frac{1}{4}(v_1(t) + v_2(t))$ (b) Energy $= \frac{1}{16}\int_{T_1}^{T_2} (v_1(t) + v_2(t))^2 dt$ (c) $\int_{T_1}^{T_2} v_1 \cdot v_2 \cdot dt \equiv 0$

Exercise 3.10 Find the Norton equivalent at the terminals marked xx in the circuit in Figure 3.12.

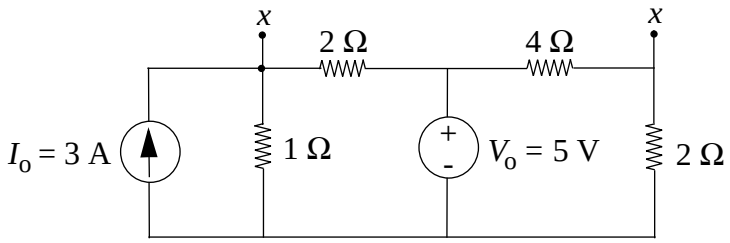


Figure 3.12:

Solution:

$$R_T = 2 \,||\, 1 + 4 \,||\, 2 = 2\Omega \quad \text{when both sources are "shut off"}$$

$$I_{SC} = \underbrace{1}_{\substack{\text{when} \\ \text{voltage} \\ \text{source} \\ \text{shut off}}} + \underbrace{0}_{\substack{\text{when} \\ \text{current} \\ \text{source} \\ \text{shut off}}} = 1\ A, \text{ by superposition}$$

ANS:: $R_T = 2\Omega$ and $I_{SC} == 1\ A$

Exercise 3.11 Find the Thévenin equivalent for the circuit in Figure 3.13 at the terminals AA'.

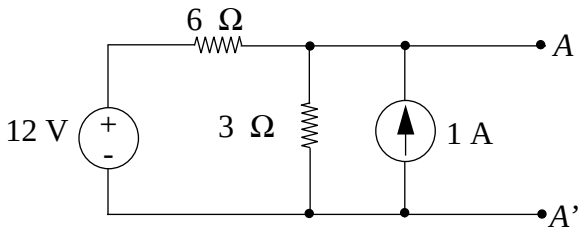


Figure 3.13:

Solution:

$R_T = 6 \,||\, 3 = 2\ \Omega$

$V_{OC} = 4\ V + 2\ V = 6\ Volts$

Find V_{OC} by superposition:

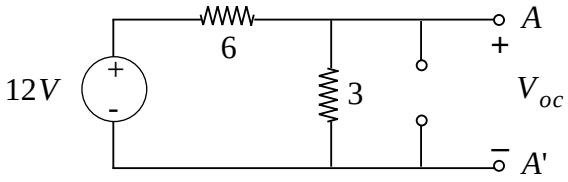


Figure 3.14:

When current source is off:

$$V_{OC} = \underbrace{\left(\frac{3}{3+6}\right)}_{\text{voltage divider}} \cdot 12\ V = 4\ Volts$$

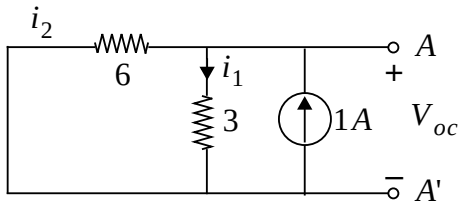


Figure 3.15:

When voltage source is off:

$$i_1 = \underbrace{\left(\frac{6}{3+6}\right)}_{\text{current divider}} \cdot 1\ A = \frac{2}{3}\ A$$

$$V_{OC} = i_1 \cdot\ 3\Omega = 2\ Volts$$

ANS:: $R_T = 2\ \Omega$ and $V_{OC} = 6\ Volts$

Exercise 3.12 In the network in Figure 3.16, find an expression for v_2.

Solution:

By superposition,

$$v_2 = v_3 \cdot \underbrace{\left(\frac{R_2}{R_1+R_2}\right)}_{\text{voltagedivider}} + I_3 \underbrace{\left(\frac{R_1}{R_1+R_2}\right)}_{\text{currentdivider}} \cdot R_2$$

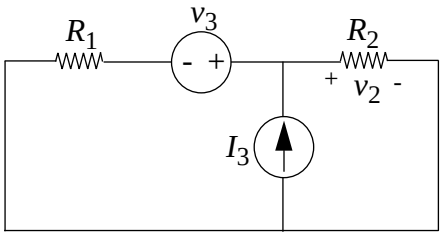


Figure 3.16:

ANS:: $v_2 = v_3 \cdot \left(\frac{R_2}{R_1+R_2}\right) + I_3 \left(\frac{R_1}{R_1+R_2}\right) \cdot \ R_2$

Exercise 3.13 The networks in Figure 3.17 are equivalent (i.e. have the same v-i relation) at terminals $A - A'$. Find v_T and R_T.

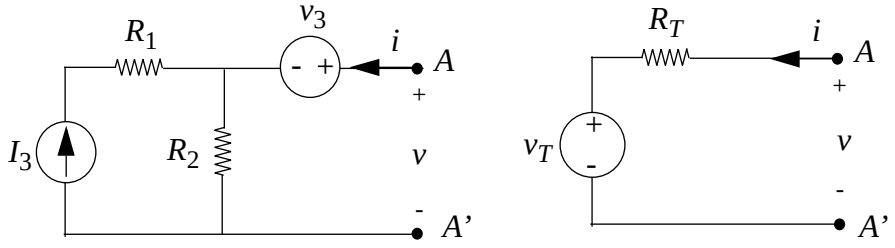


Figure 3.17:

Solution:

Right network is Thévenin Equivalent of left network.

$R_T = R_2$ since no current flows through R_1 when I_3 is shut off.

$v_T = V_{OC} = I_S \cdot \ R_2 + v_3$, by superposition.

ANS:: $R_T = R_2$ and $v_T = I_3 \cdot \ R_2 + v_3$

Exercise 3.14 For each of the circuits in Figure 3.18 give the *number* of independent node variables needed for a solution of the problem by the node method.

Solution:

a) 3 node variables

b) 3 node variables

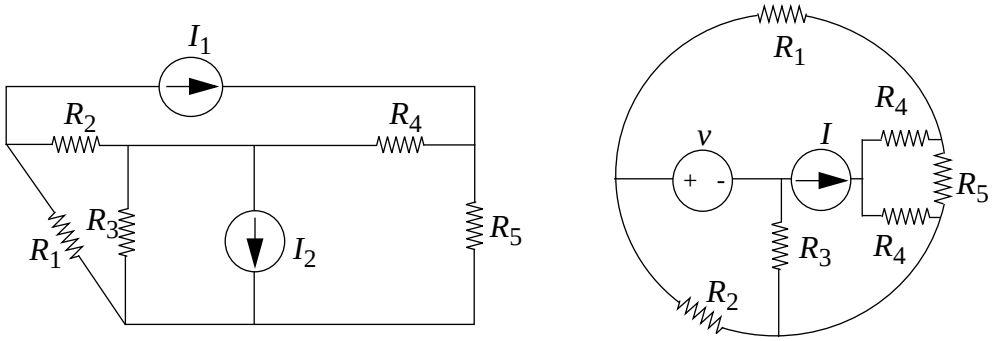


Figure 3.18:

ANS:: (a) 3 (b) 3

Exercise 3.15 For the circuit shown in Figure 3.19, write a complete set of node equations for the voltages v_a, v_b and v_c. Use conductance instead of resistance. Simplify the equations by collecting terms and arranging them in the "standard" form for n linear equations in n unknowns. *Do not solve the equations.*

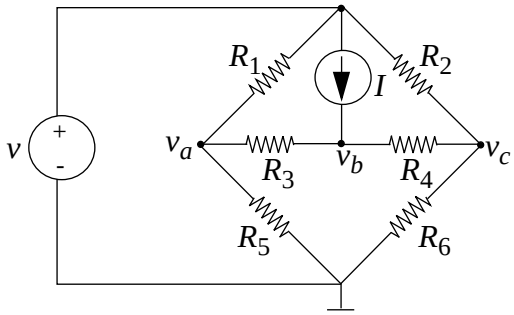


Figure 3.19:

Solution:

(1)

$$(g_1 + g_3 + g_5)\ v_a - g_3 \cdot\ v_b + 0 \cdot\ v_c = g_1 \cdot\ V$$

(2)

$$-g_3 \cdot\ v_a + (g_3 + g_4)\ v_b - g_4 \cdot\ v_c = I$$

(3)

$$0 \cdot\ v_a - g_4 \cdot\ v_b + (g_2 + g_4 + g_6) \cdot\ v_c = g_2 \cdot\ V$$

ANS:: (1) $(g_1+g_3+g_5)\ v_a-g_3 \cdot\ v_b+0 \cdot\ v_c = g_1 \cdot\ V$, (2) $-g_3 \cdot\ v_a+(g_3+g_4)\ v_b-g_4 \cdot\ v_c = I$, (3) $0 \cdot\ v_a - g_4 \cdot\ v_b + (g_2 + g_4 + g_6) \cdot\ v_c = g_2 \cdot\ V$

Exercise 3.16 For the circuit shown in Figure 3.20, use superposition to find v in terms of the R's and source amplitudes.

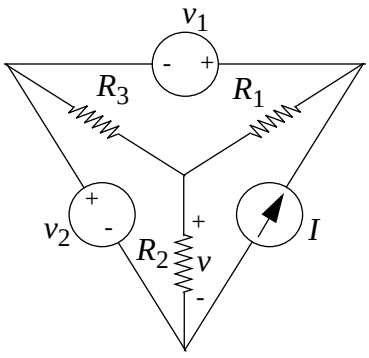


Figure 3.20:

Solution:

Redraw:

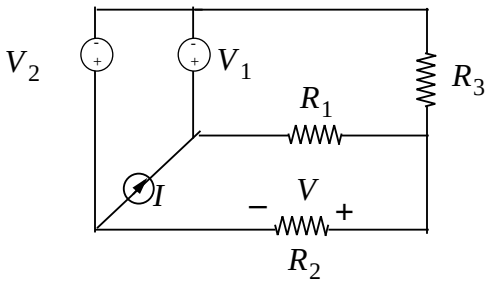


Figure 3.21:

Superposition:

1.

V_2, V_1 off; I on:

$V = 0$ since no current through R_2

2.

V_2 on; V_1 and I off:

$$V = \underbrace{-\frac{R_2}{R_2 + R_1 \,||\, R_3}}_{\text{voltage divider}} \cdot V_2$$

3.

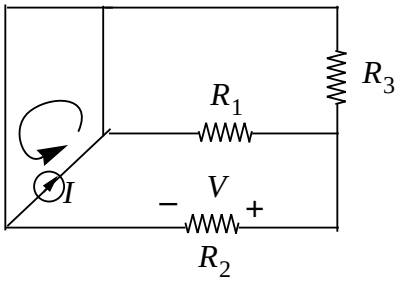


Figure 3.22:

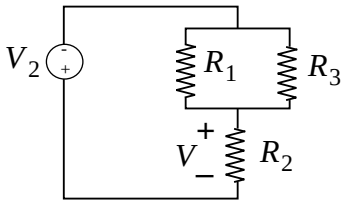


Figure 3.23:

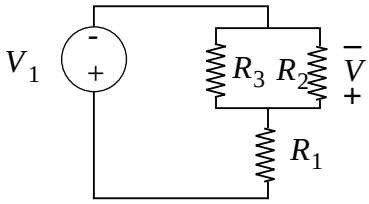


Figure 3.24:

V_1 on; V_2 and I off:

$$V = \frac{R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3} \cdot \; V_1$$

Superposition:

$$V = V_1 \cdot \; \frac{R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3} - V_2 \cdot \; \frac{R_2}{R_2 + R_1 \,||\, R_3}$$

ANS:: $V = V_1 \cdot \; \frac{R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3} - V_2 \cdot \; \frac{R_2}{R_2 + R_1 \,||\, R_3}$

Exercise 3.17 Find the Thévenin equivalent of the circuit in Figure 3.25 at the terminals indicated.

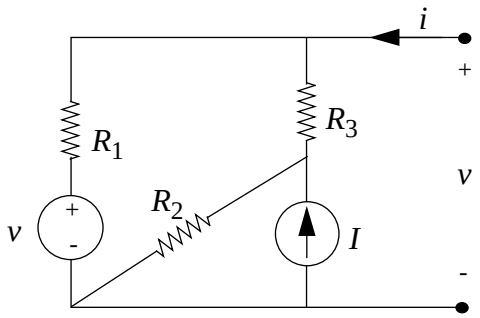


Figure 3.25:

Solution:

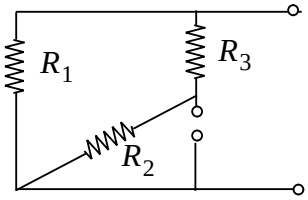


Figure 3.26:

To find R_T, shut off 2 sources:

$$R_T = R_1 \,||\, (R_2 + R_3) = \frac{R_1(R_2 + R_3)}{R_1 + R_2 + R_3}$$

To find V_{OC}, use superposition:

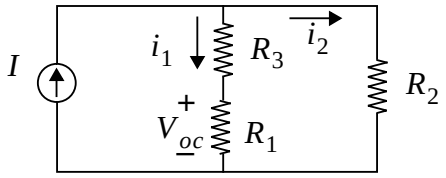


Figure 3.27:

1.

Shut off V:

$$i_1 = \frac{R_2}{R_1 + R_2 + R_3} \cdot I$$

$$V_{OC} = i_1 \cdot R_1 = \frac{R_1 R_2 \cdot I}{R_1 + R_2 + R_3}$$

2.

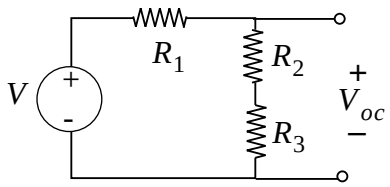


Figure 3.28:

Shut off I:

$$V_{OC} = \frac{(R_2 + R_3) \cdot V}{R_1 + R_2 + R_3}$$

$$V_{OC} = \frac{R_1 R_2 \cdot I + (R_2 + R_3)\, V}{R_1 + R_2 + R_3}$$

ANS:: $R_T = \frac{R_1(R_2+R_3)}{R_1+R_2+R_3}$, $V_{OC} = \frac{R_1 R_2 \cdot I + (R_2+R_3)\, V}{R_1+R_2+R_3}$

Exercise 3.18 In the circuit shown in Figure 3.29 there are 5 nodes, only 3 of which are independent. Take node E as a reference node, and treat nodes A, B, and D as the independent nodes.

a) Write an expression for v_C, the voltage on node C, in terms of v_A, v_B, v_D, and V_1.

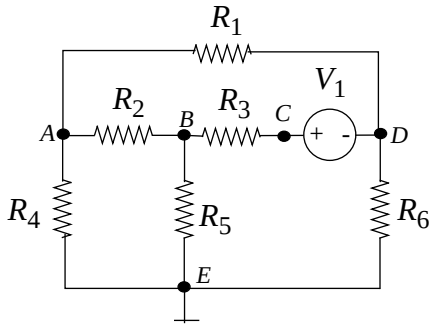


Figure 3.29:

b) Write a complete set of node equations which can be solved to find the unknown voltages in the circuit. Do not solve the set of equations but do group them neatly.

Solution:

a) $v_C = v_D + V_1$

b) $(g_1 + g_2 + g_4) \cdot\ v_A - g_2 \cdot\ v_8 - g_1 v_D = 0$
$-g_2 \cdot\ v_A + (g_2 + g_3 + g_5)\ v_B - g_3\ v_D = g_3\ V_1$
$-g_1 \cdot\ v_A - g_3\ v_B + (g_1 + g_3 + g_6) \cdot\ v_D = g_3\ V_1$

ANS:: (A) $v_C = v_D + V_1$ (b) $(g_1 + g_2 + g_4) \cdot\ v_A - g_2 \cdot\ v_8 - g_1 v_D = 0$, $-g_2 \cdot\ v_A + (g_2 + g_3 + g_5)\ v_B - g_3\ v_D = g_3\ V_1$, $-g_1 \cdot\ v_A - g_3\ v_B + (g_1 + g_3 + g_6) \cdot\ v_D = g_3\ V_1$

Exercise 3.19 Consider the circuit in Figure 3.30.

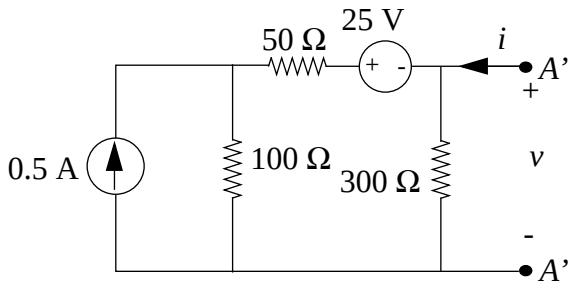


Figure 3.30:

a) Find a Norton equivalent circuit for this circuit at terminals $A - A'$.

b) Find the Thévenin equivalent circuit corresponding to your answer in Part a).

Solution:

a) $R_T = (100 + 50) \,||\, 300 = 100\ \Omega$

$$V_{OC} = \underbrace{\left(\frac{100}{100 + 50 + 300}\right) \cdot \ (0.5\ A)}$$

Current divider:

$$\cdot\ 300 + \left(\frac{-300}{300 + 100 + 50}\right) \cdot \ 25\ V$$

$$V_{OC} = 16\frac{2}{3}\ Volts$$

From this, one can find the short-circuit current:

$$I_{SC} = \frac{V_{OC}}{R_T} = 1/6\ Amperes$$

b) The open-circuit voltage was found in the previous part.

ANS:: $R_T = 100\ \Omega$, $V_{OC} = 16\frac{2}{3}$ Volts, $I_{SC} = 1/6$ Amperes

Exercise 3.20 Measurements made on terminals $B - B'$ of a linear circuit in Figure 3.31(i), which is known to be made up only of independent voltage sources and current sources, and resistors, yield the current-voltage characteristics shown in Figure 3.31(ii).

a) Find the Thévenin equivalent of this circuit.

b) Over what portions, if any, of the i-v characteristic does this circuit absorb power.

Solution:

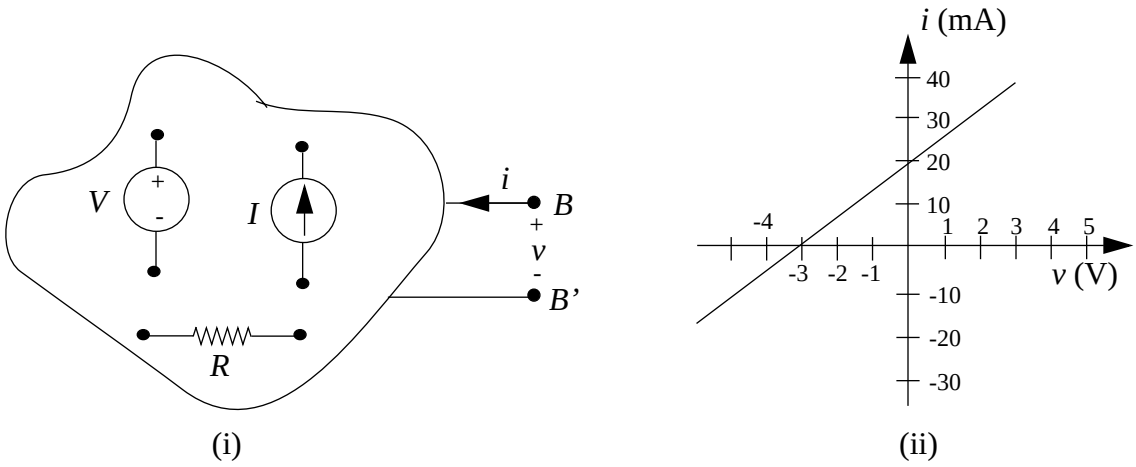


Figure 3.31:

a) $V_{OC} = -3\ Volts$ (voltage when current, $i = 0$)

$$R_T = \frac{1}{slope} = \frac{3\ V}{0.02\ A} = 150\ \Omega$$

We find $Power = i \cdot\ v$

b) In quadrants 1 and 3, the product $i \cdot\ v$ is positive. Thus, the circuit *absorbs* power within this range.

ANS:: (a) $V_{OC} = -3$ Volts, $R_T = 150\ \Omega$, (b) In quadrants 1 and 3

Exercise 3.21

a) Write in standard form the minimum number of node equations needed to analyze the circuit in Figure 3.32.

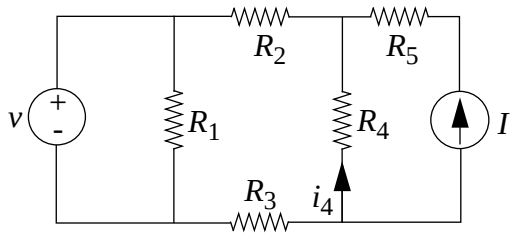


Figure 3.32:

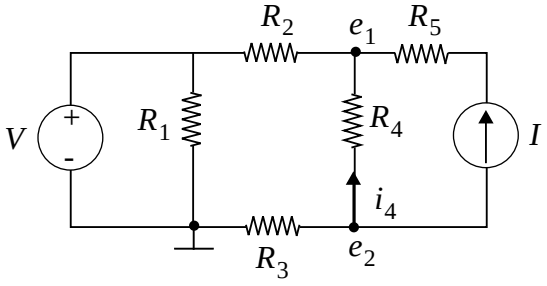


Figure 3.33:

b) Determine explicitly the current i_4.

Solution:

a)

$$i_4 = \frac{(e_2 - e_1)}{R_4}$$

Thus we need to find e_2, e_1.

$g_1 = \frac{1}{R_1}$, etc.

Node equations: ***Standard form:***

(1) At e_1:

$$\frac{(V - e_1)}{R_2} + I + \frac{(e_2 - e_1)}{R_4} = 0 \quad \Rightarrow \quad e_1\,(-g_2 - g_4) + e_2\; g_4 = -V\; g_2 - I$$

(2) At e_2:

$$\frac{(0 - e_2)}{R_3} - I + \frac{(e_1 - e_2)}{R_4} = 0 \quad \Rightarrow \quad e_1 \cdot\; g_4 + e_2(-g_4 - g_3) = I$$

b) We find that:

$$e_2 = \frac{I\; g_2 - V\; g_2 g_4}{g_4\; g_2 + g_3\; g_2 + g_3\; g_4}$$

$$e_1 = \frac{I\;(g_4\; g_2 + g_3\; g_2 + g_3\; g_4) - g_2\;(I - V\; G_4)\;(g_4 + g_3)}{g_4 \cdot\;(g_4\; g_2 + g_3\; g_2 + g_3\; g_4)}$$

$$(e_2 - e_1) = \frac{-(V \cdot\; g_2 \cdot\; g_3) + I \cdot\;(g_2 + g_3))}{g_2\; g_4 + g_2\; g_3 + g_3\; g_4}$$

$$i_4 = \frac{-g_4 \cdot\;(V \cdot\; g_2 \cdot\; g_3 + I \cdot\;(g_2 + g_3))}{g_2\; g_4 + g_2\; g_3 + g_3\; g_4}$$

ANS:: (a) $e_1\ (-g_2 - g_4) + e_2\ g_4 = -V\ g_2 - I$, and $e_1 \cdot\ g_4 + e_2(-g_4 - g_3) = I$, (b) $i_4 = \frac{-g_4 \cdot (V \cdot g_2 \cdot g_3 + I \cdot (g_2 + g_3))}{g_2\ g_4 + g_2\ g_3 + g_3\ g_4}$

Exercise 3.22

a) Find the Thévenin equivalent of the circuit in Figure 3.34.

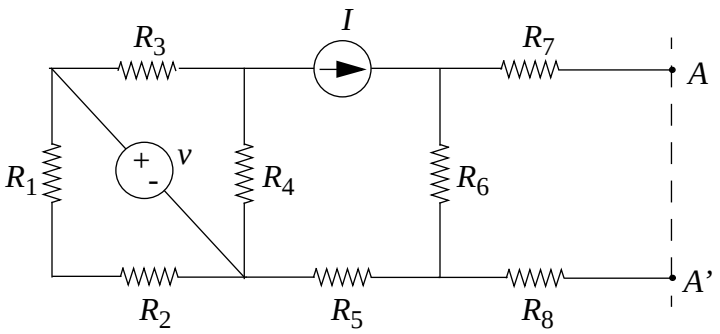


Figure 3.34:

b) Find the Norton equivalent of the circuit in Figure 3.35.

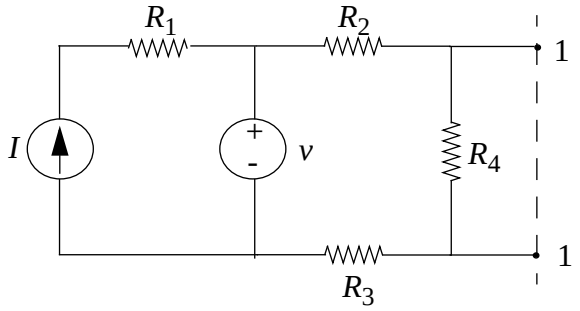


Figure 3.35:

Solution:

a) $R_T = R_6 + R_7 + R_8$, since the current source cuts off the subcircuit to its left, for the purpose of determining the Thevenin resistance.

$V_{OC} = I \cdot R_6$

b) $R_T = R_4 \,||\, (R_2 + R_3)$, since no current flows through R_1

$I_{SC} = \frac{V}{R_2 + R_3}$

ANS:: (a) $R_T = R_6 + R_7 + R_8$ and $V_{OC} = I \cdot \ R_6$, (b) $R_T = R_4 \ || \ (R_2 + R_3)$, and $I_{SC} = V/(R_2 + R_3)$

Exercise 3.23

a) Find the Norton equivalent of the circuit in Figure 3.36.

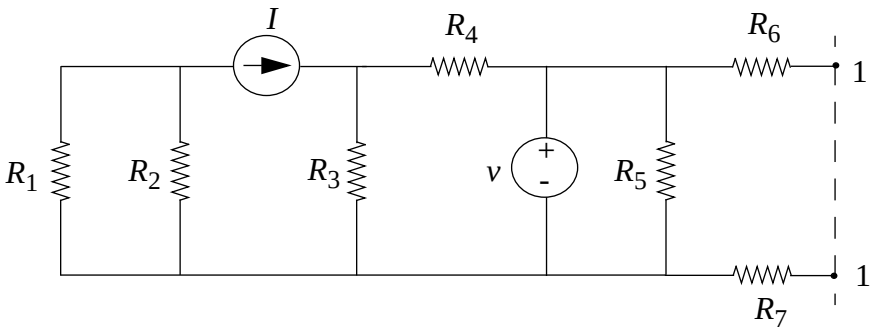


Figure 3.36:

b) Find the Thévenin equivalent of the circuit in Figure 3.37.

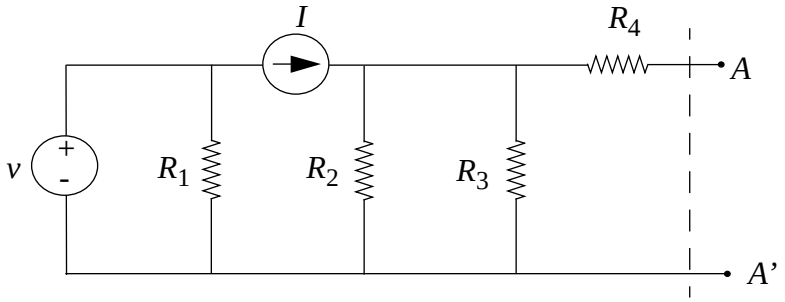


Figure 3.37:

Solution:

a) $R_T = R_6 + R_7$
$I_{sc} = V/(R_6 + R_7)$

b) $R_T = (R_2 \ || \ R_3) + R_4$
$V_{OC} = I \ (R_2 \ || \ R_3)$

ANS:: (a) $R_T = R_6 + R_7$, $I_{sc} = V/(R_6 + R_7)$, (b) $R_T = (R_2 \ || \ R_3) + R_4$, $V_{OC} = I \ (R_2 \ || \ R_3)$

Exercise 3.24 Find the Thévenin equivalent circuit as seen from the terminals $a - b$ in Figure 3.38.

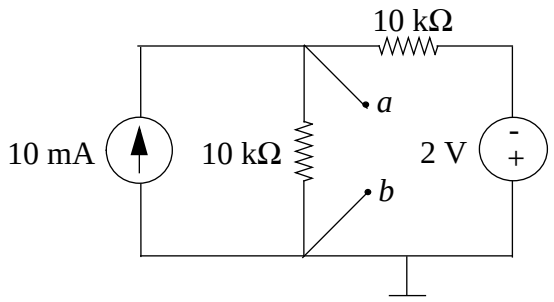


Figure 3.38:

Solution:

$R_T = 10k\Omega \,||\, 10k\Omega = 5k\Omega$

By superposition,

$$V_{OC} = (10mA)[10k\Omega \,||\, 10k\Omega] + (-2V)\left(\frac{10k}{10k + 10k}\right) = 49Volts$$

ANS:: $R_T = 5k\Omega$, $V_{OC} = 49$ Volts

Exercise 3.25 Find the node potential E in Figure 3.39.

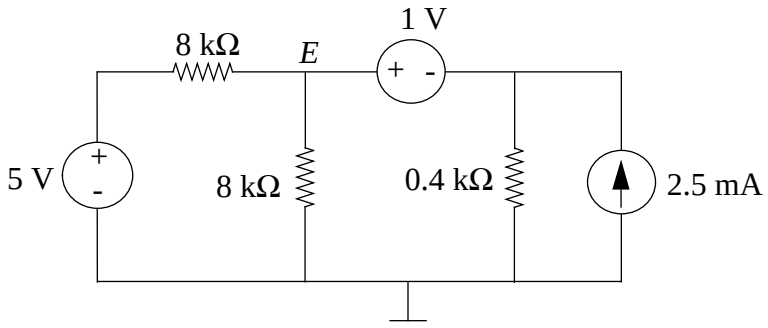


Figure 3.39:

Solution:

$E = 0.8V + 0.8V + 0.8V = 2.4V$, by superposition.

ANS:: 2.4 Volts

Exercise 3.26 For the circuit in Figure 3.40, write the node equations. Do not solve, but write in matrix form: source terms on the left, unknown variables on the right.

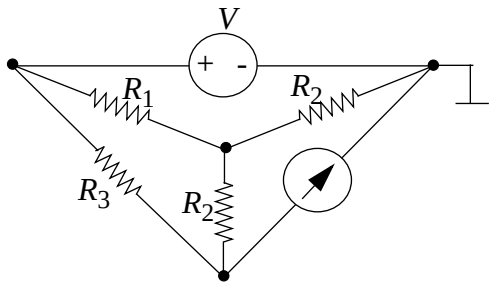


Figure 3.40:

Solution:

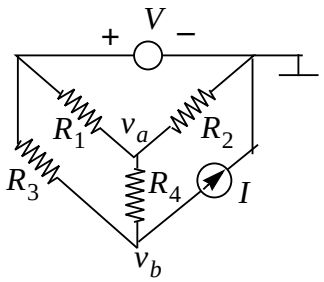


Figure 3.41:

(1) $V \cdot\ g_1 = v_a\ (g_1 + g_2 + g_4) - v_b \cdot\ g_4$

(2) $V \cdot\ g_3 - I = +v_a\ (-g_4) + v_b\ (g_3 + g_4)$

ANS:: $V \cdot\ g_1 = v_a\ (g_1 + g_2 + g_4) - v_b \cdot\ g_4$, and $V \cdot\ g_3 - I = +v_a\ (-g_4) + v_b\ (g_3 + g_4)$

Exercise 3.27 Find v_1 by superposition for the circuit in Figure 3.42.

Solution:

Superposition:

1.

V off, I on

$$v_i = I \cdot\ (R_2\ ||\ R_1)$$

2.

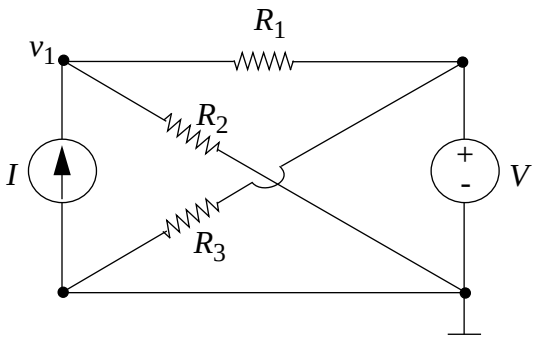


Figure 3.42:

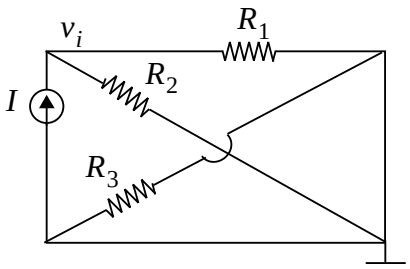


Figure 3.43:

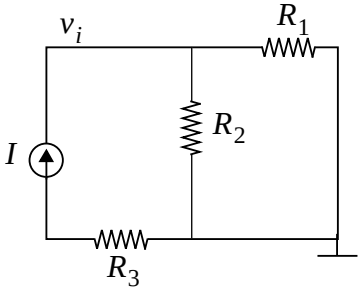


Figure 3.44:

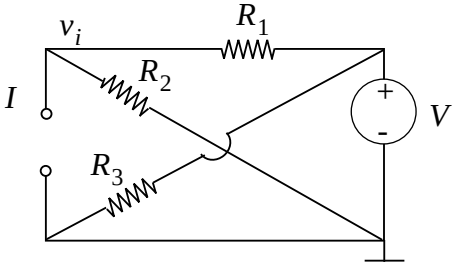


Figure 3.45:

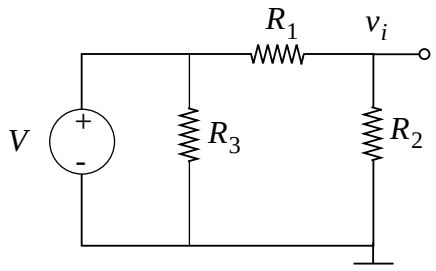


Figure 3.46:

V on, I off

$$v_i = V\frac{R_2}{R_1 + R_2}$$

$$v_i = I \cdot \left(\frac{R_1\ R_2}{R_1 + R_2}\right) + V \cdot \left(\frac{R_2}{R_1 + R_2}\right)$$

ANS:: $v_i = I \cdot \left(\frac{R_1\ R_2}{R_1+R_2}\right) + V \cdot \left(\frac{R_2}{R_1+R_2}\right)$

Problems

Problem 3.1 A fuse is a wire with a positive temperature coefficient of resistance (in other words, its resistance increases with temperature). When a current is passed through the fuse, power is dissipated in the fuse, which raises its temperature.

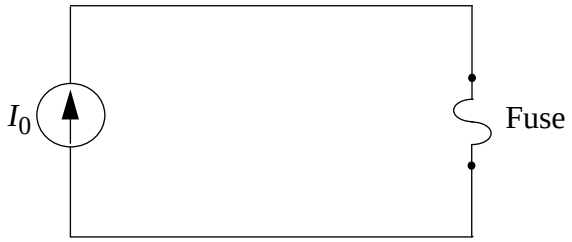


Figure 3.47:

Use the following data to determine the current I_0 at which the fuse (in Figure 3.47) will blow (i.e., its temperature goes up without limit).

Fuse Resistance:
$R = 1 + a\,T\ Ohms$
$a = .001\Omega/degrees\ C$
$T = Temperature\ rise\ about\ ambient$

Temperature rise:
$T = \beta P$
$\beta = \left(\frac{1}{.225}\right) degrees\ C/Watts$
$P = power\ dissipated\ in\ fuse$

Solution:

$R = 1 + a\beta P\ Ohms$

$R = 1 + a\beta I_0^2 R\ Ohms$

$R = \frac{1}{1 - a\beta I_0^2}\ Ohms$

$1 - a\beta I_0^2 = 0$

$I_0 = 15\ amps$

ANS:: 15 amps

Problem 3.2

a) Prove, if possible, each of the following statements. If a proof is not possible, illustrate the failure with a counter-example and restate the theorem with a suitable restriction so it can be proved.

   i) In a network containing only linear resistors, every branch voltage and branch current must be zero.

   ii) The equivalent of a one-port network containing only linear resistors is a linear resistor.

b) To demonstrate that you understand superposition, construct an example which shows explicitly that a network containing a nonlinear resistor will not obey superposition. You may select any nonlinear element (provided you show that it is not linear) and any simple network containing that element.

Solution:

a) i) This is true. Assume that there is a nonzero branch voltage. That must cause a nonzero branch current, due to the $v - i$ relationship of a linear resistor.

Therefore the resistor consumes power. Something must be producing this power, but linear resistors cannot produce power, so our hypothesis falls apart. Therefore there are no nonzero branch voltages or branch currents.

ii) This is true. This is the mathematical definition of linearity.

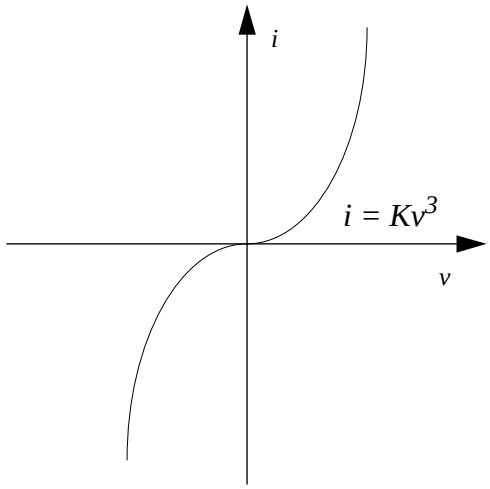


Figure 3.48:

b) Consider the nonlinear resistor with the $i - v$ relation shown in Figure 3.48, which is given by $i = Kv^3$. Let a voltage v_1 be applied across the resistor. A current $i_1 = Kv_1^3$ flows through the resistor. Similarly, a voltage v_2 produces a current $i_2 = Kv_2^3$. Suppose a voltage $v_3 = v_1 + v_2$ is applied. The $i - v$ relation tells us the resultant i_3 is $Kv_3^3 = K(v_1 + v_2)^3$. However, superposition tells us i_3 is $i_1 + i_2 = Kv_1^3 + Kv_2^3$, which in general is not equal to what the $i - v$ relation says.

Problem 3.3 Find V_0 in Figure 3.49. Solve by (1) Node Method, (2) Superposition. All resistances are in Ohms.

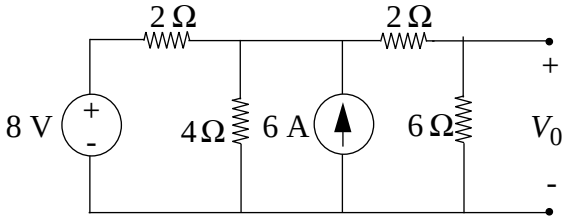


Figure 3.49:

Solution:

(1) Node Method
Label the nodes e_1 and e_2 as shown in Figure 3.50.

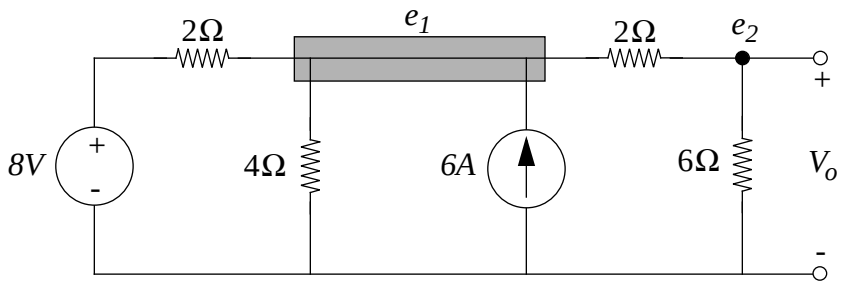


Figure 3.50:

By the node method, we obtain the following two equations:

$\frac{8\ V-e_1}{2\ Ohms} - \frac{e_1}{4\ Ohms} + 6\ A + \frac{e_2-e_1}{2\ Ohms} = 0$

$\frac{e_1-e_2}{2\ Ohms} - \frac{e_2}{6\ Ohms} = 0$

Thus, $V_0 = e_2 = 8.57\ V$

(2) Superposition
Find the voltage due to each source independently, as shown in Figure 3.51 and Figure 3.52.

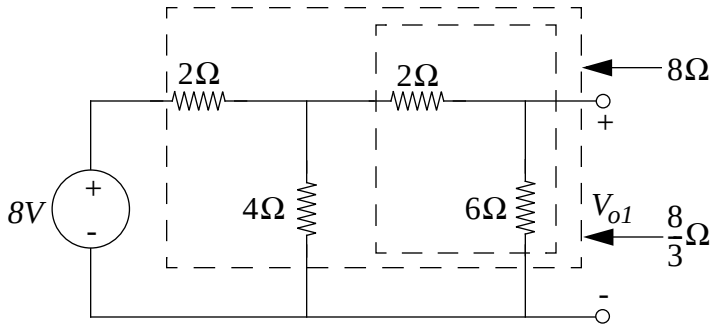


Figure 3.51:

$V_{01} = (8\ V)(\frac{\frac{8}{3}\ Ohms}{2+\frac{8}{3}\ Ohms}\frac{6\ Ohms}{8\ Ohms} = 3.43\ V$

$V_{02} = (6\ A)(\frac{\frac{4}{3}\ Ohms}{8+\frac{4}{3}\ Ohms}(6\ Ohms) = 5.14\ V$

$V_0 = V_{01} + V_{02} = 8.57\ V$

ANS:: 8.57 V

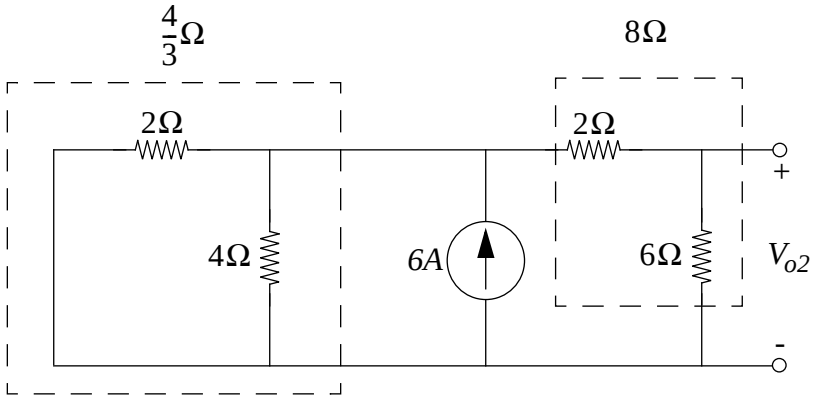


Figure 3.52:

Problem 3.4 Consider the figure you used for the previous problem (Figure 3.49). Find the Norton equivalent of the network as seen at the terminals on the right.

Solution:

Remove the sources to find R_{TH}, as shown in Figure 3.53.

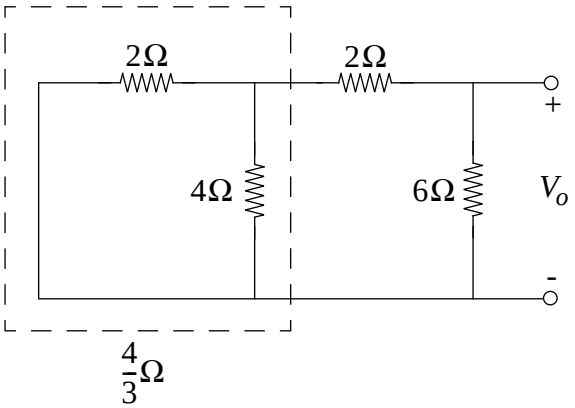


Figure 3.53:

$R_{TH} = \frac{(6\ Ohms)(2+\frac{4}{3}\ Ohms)}{6+2+\frac{4}{3}} = 2.14\ Ohms$

$i_N = \frac{v_{TH}}{R_{TH}} = \frac{v_{OC}}{R_{TH}} = 4\ A$

The Norton equivalent is shown in Figure 3.54.

ANS:: 2.14 Ohms and 4 A

Problem 3.5

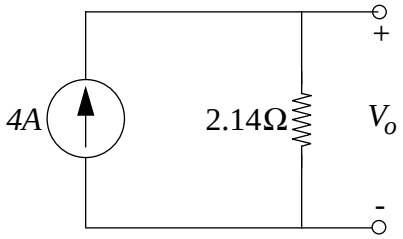


Figure 3.54:

a) Find R_{eq}, the equivalent resistance "looking into" the terminals on the right, of the circuit in Figure 3.55.

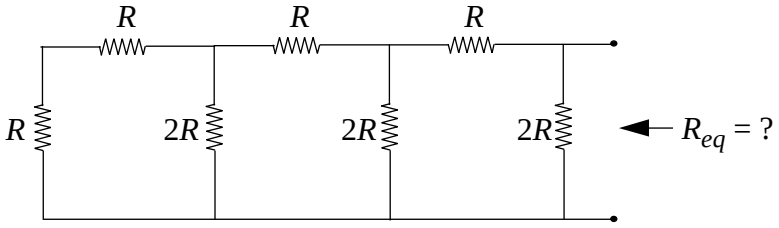


Figure 3.55:

b) Find the Thévenin equivalent, looking into the terminals on the right of the circuit in the figure in Figure 3.56.

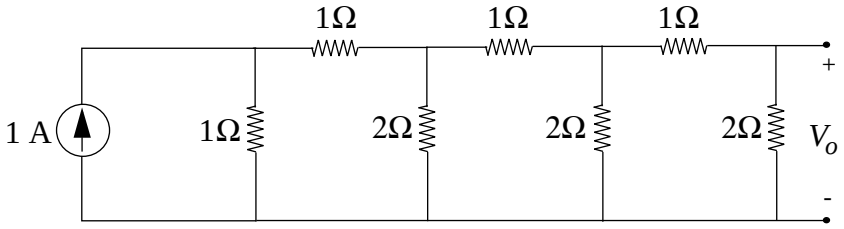


Figure 3.56:

Solution:

a) See Figure 3.57.

$R_{eq} = R$

b) Check out Figure 3.58.

$v_{TH} = v_{OC} = (2\ Ohms)(1\ A)\frac{1\ Ohms}{1+\frac{43}{21}\ Ohms}\frac{2\ Ohms}{2+\frac{11}{5}\ Ohms}\frac{2\ Ohms}{2+3\ Ohms} = .125\ V$

$R_{TH} = 1\ Ohm$

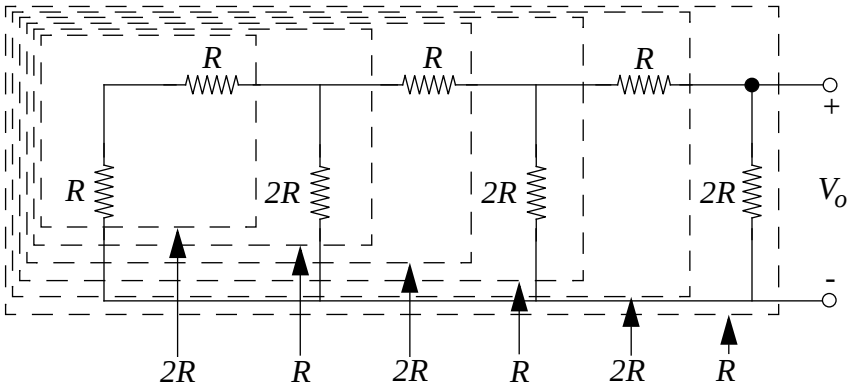


Figure 3.57:

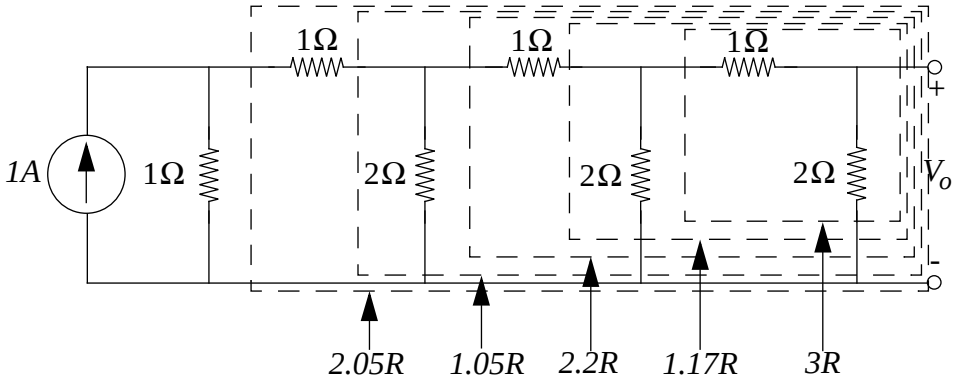


Figure 3.58:

ANS:: (a) $R_{eq} = R$, (b) $v_{TH} = .125V, R_{TH} = 1Ohm$

Problem 3.6 Find v_i for $I = 3$ amps, $V = 2$ volts in Figure 3.59. Strategy: to avoid numerical errors, derive expressions in literal form first, then check dimensions.

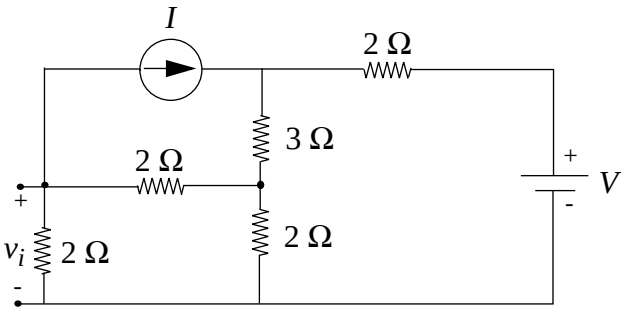


Figure 3.59:

Solution:

Use the node method. Label the nodes as shown in Figure 3.60.

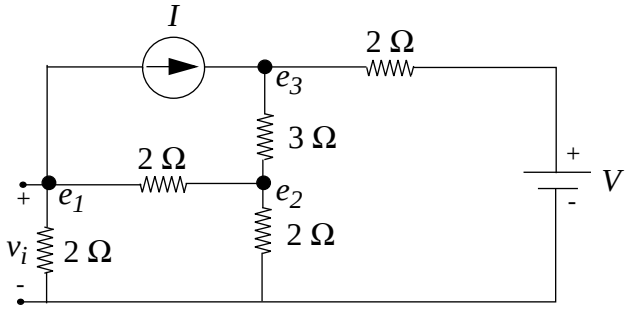


Figure 3.60:

Node equations:

$$e_1(\frac{1}{2\Omega} + \frac{1}{2\Omega}) - e_2\frac{1}{2\Omega} = -I$$

$$-e_1(\frac{1}{2\Omega}) + e_2(\frac{1}{2\Omega} + \frac{1}{2\Omega} + \frac{1}{3\Omega}) - e_3(\frac{1}{3\Omega}) = 0$$

$$-e_2\frac{1}{3\Omega} + e_3(\frac{1}{3\Omega} + \frac{1}{2\Omega}) = I + \frac{V}{2\Omega}$$

Solving with $I = 3A$ and $V = 2V$:

$$e_1 = -\frac{56}{19}V$$

$$e_2 = \frac{2}{19}V$$
$$e_3 = \frac{92}{19}V$$

Thus,

$$v_i = e_1 = -\frac{56}{19}V \approx \ -2.95V$$

ANS:: -2.95 V

Problem 3.7 For the circuits in Figures 3.61(i) and (ii):

a) Find v_o for $R_1 = R$.

b) Find v_o for $R_1 \neq R$

c) Find the Thévenin equivalent for the network to the right of points AB, assuming $R_1 = R$.

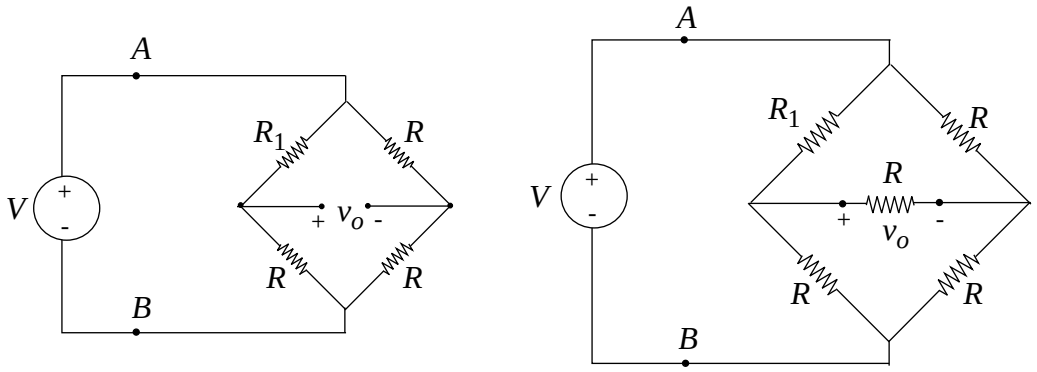


Figure 3.61:

Solution:

a) By symmetry, $v_O = 0$ in both cases.

b) For (i), we can use two voltage dividers:
$v_O = V(\frac{R}{R+R_1} - \frac{1}{2})$
Note that the $R_1 = R$ case reduces to part a.
For (ii), we must use the node method (See Figure 3.62).

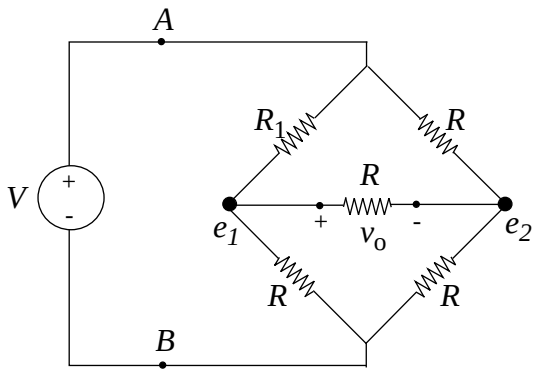


Figure 3.62:

$\frac{e_1-V}{R_1} + \frac{e_1-e_2}{R} + \frac{e_1}{R} = 0$
$\frac{e_2-V}{R} + \frac{e_2-e_1}{R} + \frac{e_2}{R} = 0$
So, $v_O = e_1 - e_2 = \frac{V(R-R_1)}{3R+5R_1}$

c) By symmetry, no current flows across the middle resistor for (ii), so we can replace it with an open circuit. Therefore, cases (i) and (ii) are identical. The equivalent resistance of the four resistors can be easily found, so in both cases, $R_{TH} = R$ and $v_{TH} = 0$.

ANS:: (a) 0, b) i) $V(\frac{R}{R+R_1} - \frac{1}{2})$, ii) $\frac{V(R-R_1)}{3R+5R_1}$, c) $R_{TH} = R, V_{TH} = 0$.

Problem 3.8

a) Determine the equation relating i to v in Figure 3.63.

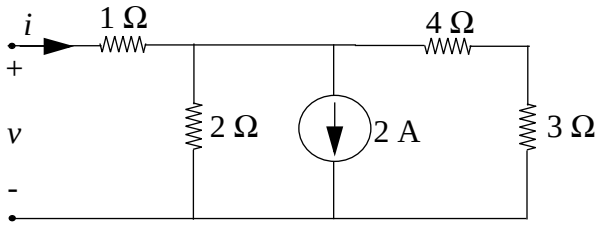


Figure 3.63:

b) Plot the i-v characteristic of the network.

c) Draw the Thévenin equivalent circuit.

d) Draw the Norton equivalent circuit.

Solution:

a) See Figure 3.64.

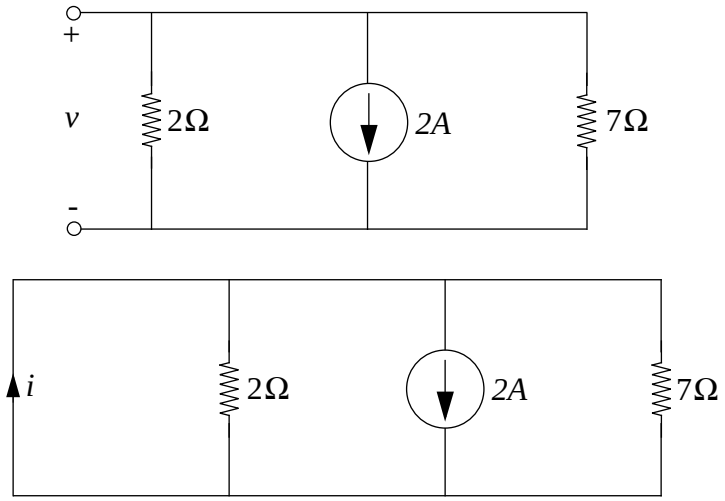


Figure 3.64:

In (i), $i = 0$, so $v = -(2\ A)\frac{(2\ Ohms)(7\ Ohms}{2+7\ Ohms} = -3.11\ V$.

In (ii), $v = 0$, so $i = (2\ A)\frac{\frac{14}{9}\ Ohms}{1+\frac{14}{9}Ohms} = 1.22\ A$.

Hence, by linearity, $v = (2.55\ Ohms)i - 3.11\ V$

b) See Figure 3.65.

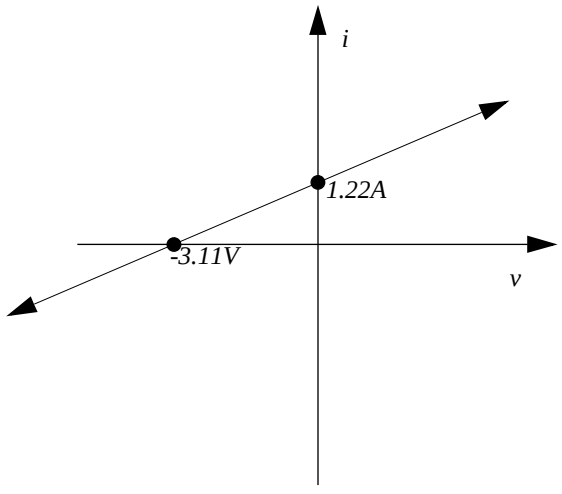


Figure 3.65:

c) See Figure 3.66.

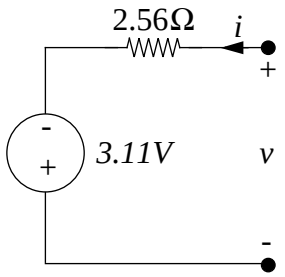


Figure 3.66:

d) See Figure 3.67.

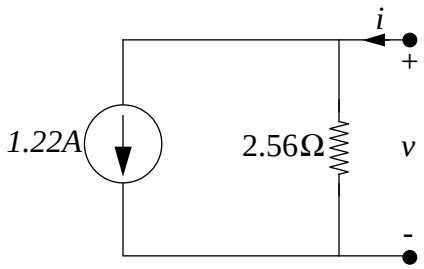


Figure 3.67:

ANS:: (a) $v = (2.55Ohms)i - 3.11V$

Problem 3.9 In Figure 3.68, find v_o via (a) superposition, (b) the node method.

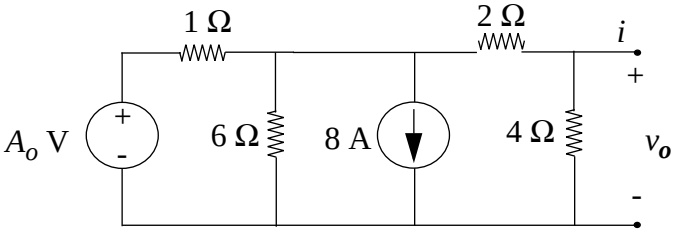


Figure 3.68:

Solution:

a) See Figure 3.69.

Find the voltage due to each source. So,

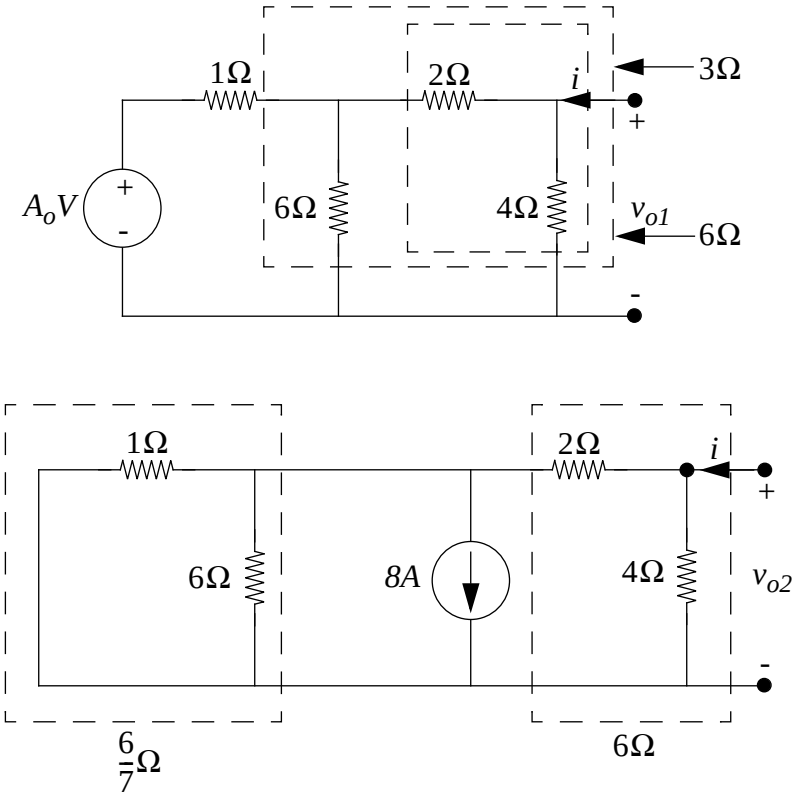


Figure 3.69:

$$v_{O1} = (A_0\ volts)\frac{3\ Ohms}{1+3\ Ohms}\frac{4\ Ohms}{2+4\ Ohms} = \frac{A_0}{2}\ volts$$

$$v_{O2} = (8\ A)\frac{\frac{6}{7}\ Ohms}{6+\frac{6}{7}\ Ohms}(-4\ Ohms) = -4\ volts$$

$$v_O = v_{O1} + v_{O2} = \frac{A_0}{2} - 4\ volts$$

b) See Figure 3.70.

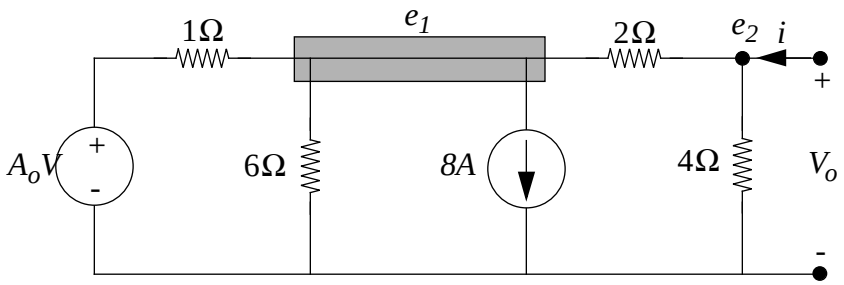


Figure 3.70:

$$\frac{e_2-e_1}{2\ Ohms} - 8\ A - \frac{e_1}{6\ Ohms} + \frac{A_0-e_1}{1\ Ohm} = 0$$

$$\frac{e_1-e_2}{2\ Ohms} - \frac{e_2}{4\ Ohms} = 0$$

$$v_O = e_2 = \frac{A_0}{2} - 4\ volts$$

ANS:: $\frac{A_0}{2} - 4$ volts

Problem 3.10 Use the following three different methods to find i in Figure 3.71:

1) Node Method

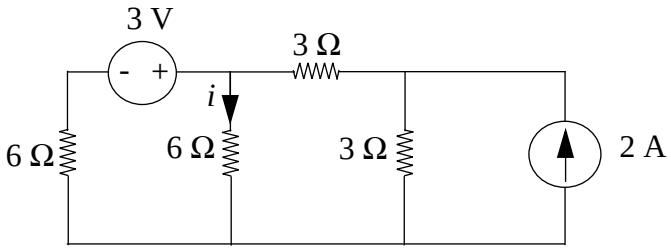


Figure 3.71:

2) Superposition

3) Alternate Thévenin/Norton Transformations

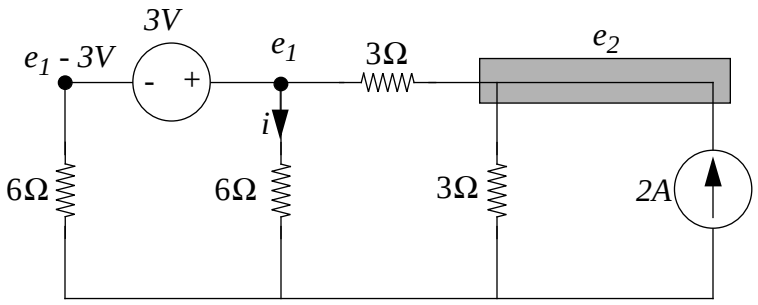


Figure 3.72:

Solution:

1) See Figure 3.72.

   From the node diagram, we get:

   $\frac{e_2-e_1}{3\ Ohms} - \frac{e_1}{6\ Ohms} + \frac{3\ Volts-e_1}{6\ Ohm} = 0$

   $2\ A - \frac{e_2}{3\ Ohms} + \frac{e_1-e_2}{3\ Ohm} = 0$

   So, $i = \frac{e_1}{6\ Ohms} = .5\ amps$

2) See Figure 3.73.

   From each source, we get:

   $i_1 = \frac{3\ V}{9\ Ohms}\frac{6\ Ohms}{6+6\ Ohms} = .167\ amps$

   $i_2 = (2\ A)\frac{3\ Ohms}{3+6\ Ohms}\frac{6\ Ohms}{6+6\ Ohms} = .333\ amps$

   So, $i = i_1 + i2 = .5\ amps$

3) See Figure 3.74.

   "Nortonize" the parts of the circuits on either side of the wire whose current we are finding, and simplify:

   So, $i = (1.5amps)/frac3\ Ohms3 + 6\ Ohms = .5\ amps$

ANS:: .5 amps

Problem 3.11 A student is given an unknown resistive network as illustrated in Figure 3.75. She wishes to determine whether the network is linear, and if it is, what its Thévenin equivalent is.

The only equipment available to the student is a voltmeter (assumed ideal), 100 kΩ and 1 MΩ test resistors that can be placed across the terminals during a measurement (Figure 3.76).

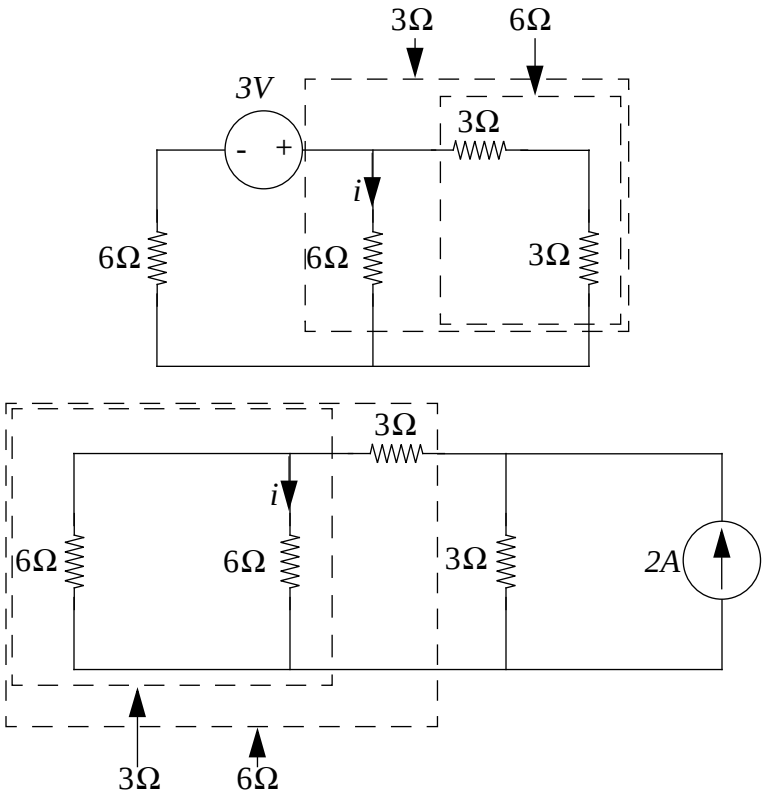


Figure 3.73:

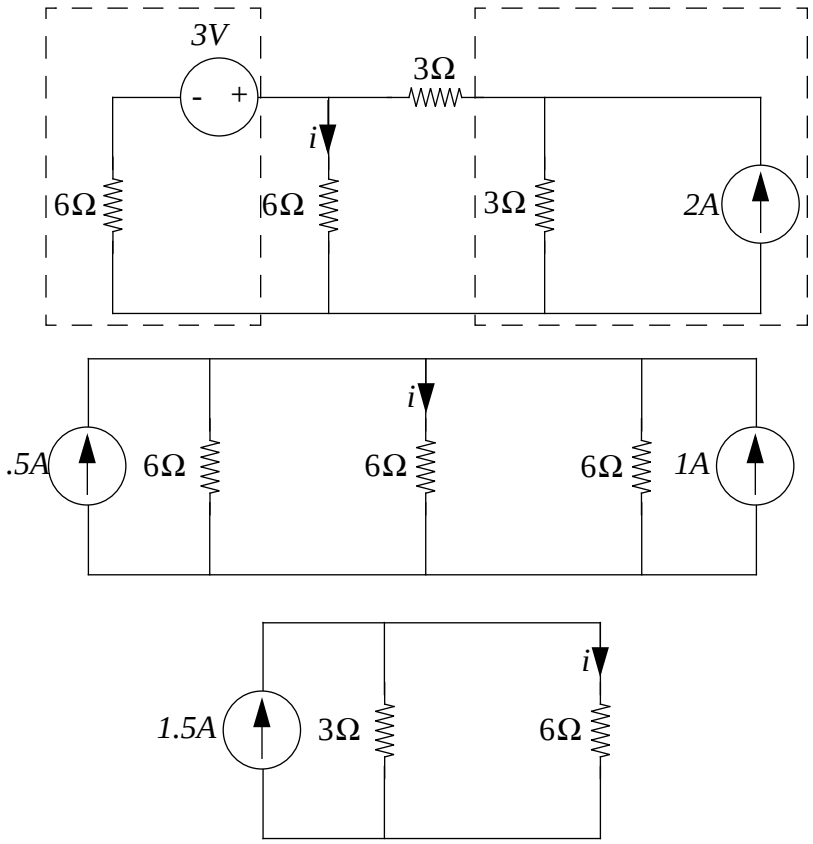


Figure 3.74:

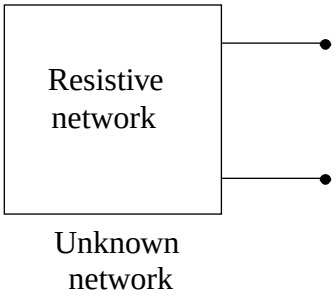


Figure 3.75:

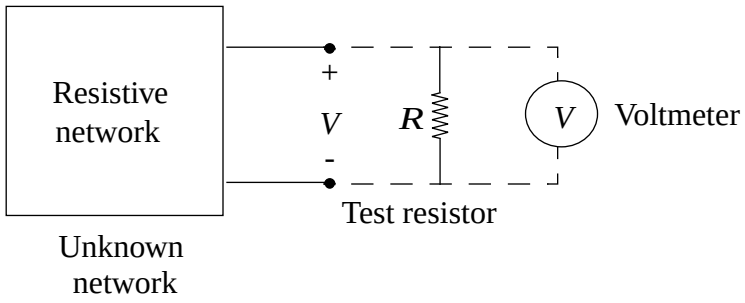


Figure 3.76:

The following data were recorded:

Test Resistor	Voltmeter Reading
Absent	$1.5v$
$100k\Omega$	$0.25v$
$1M\Omega$	$1.0v$

What should the student conclude about the network from these results? Support your conclusion with plots of the network v-i characteristics.

Solution:

Let us assume that the network is linear and that the Thévenin equivalent voltage of the network be denoted V_{TH} and resistance R_{TH}.

Without the test resistor, the measured voltage of 1.5V is the open circuit voltage. Thus $V_{TH} = 1.5V$.

With a 100k resistor, the voltage measured across the test resistor is

$$0.25 = \frac{1.5V100k}{100k + R_{TH}}$$

Thus $R_{TH} = 500k$.

With a 1M resistor, the voltage measured across the test resistor is

$$\frac{1.5V1M}{500k + 1M} = 1V$$

This is corroborated by our measurement. Thus, the network is a linear network, and can be represented by V_{TH} and R_{TH}.

Problem 3.12

a) Devise an electrical circuit of voltage sources and resistors that will "calculate" the balance point (center of mass) of the massless bar shown in Figure 3.77, for 3

arbitrary masses hung at 3 arbitrary places along the bar. We want the circuit to generate a voltage which is proportional to the position of the balance point. Write the equation for your network, and show that it performs the required calculation. (Work with conductances and superposition for a simple solution.)

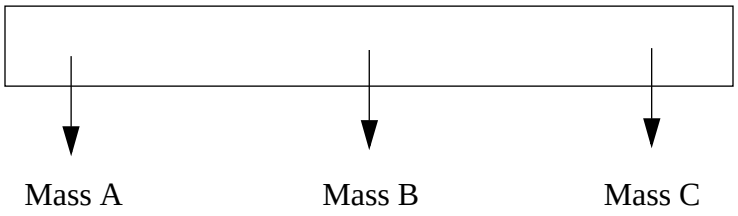


Figure 3.77:

b) Extend your result in part a) to two dimensions, that is, devise a new network (which will have more voltage sources and more resistors than above) that can find the center of mass of a triangle with arbitrary weights handing from its three corners. The network will now have to give you two voltages, one representing the x coordinate and the other the y coordinate of the center of mass. This system is a barycentric coordinate calculator, and can be used as the input for video games, or to simulate trichromatic color vision in the human eye.

Solution:

a) See Figure 3.78.

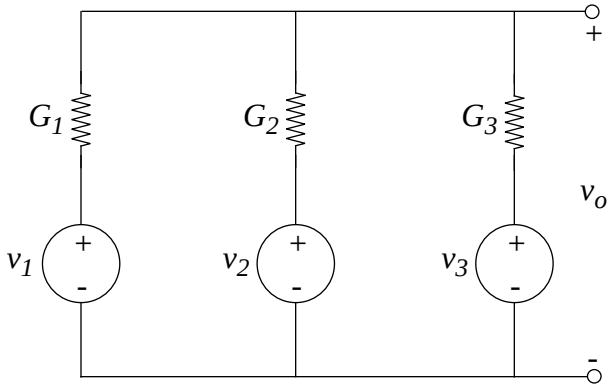


Figure 3.78:

The center of mass of the bar is given by the equation $x_{cm} = \frac{m_1 x_1 + m_2 x_2 + m3 x_3}{m_1 + m_2 + m3}$, where m_i and x_i are the mass and position of the i^{th} hanging object, respectively. Analogously, in Figure 3.78, the conductances represent the masses, and the voltages represent the positions. Thus, $v_O = \frac{G_1 V_1 + G_2 V_2 + G3 V_3}{G_1 + G_2 + G3}$, as needed.

b) See Figure 3.79.

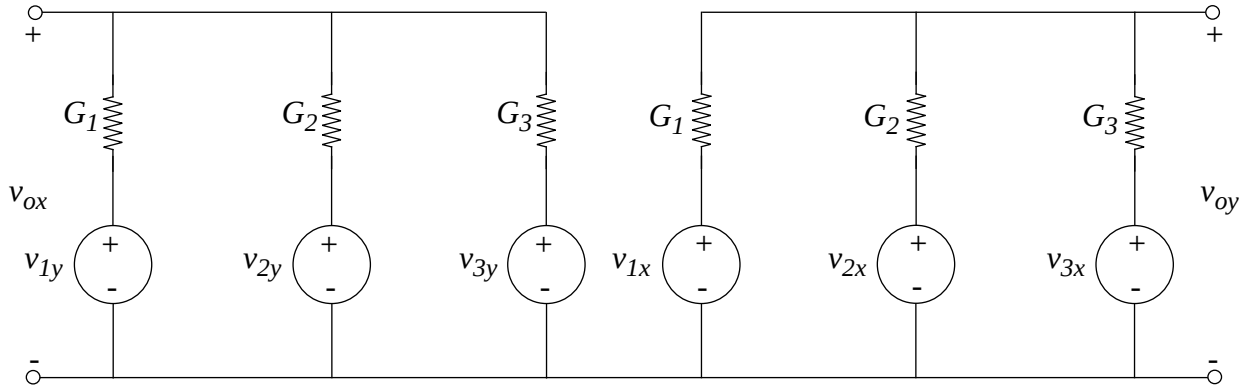


Figure 3.79:

Similar reasoning as in part a.

Problem 3.13

a) Find the Thévenin equivalent for the network in Figure 3.80 at the terminals CB. The current source is a *controlled source*. The current flowing through the current source is βI_1, where β is some constant. (We will discuss controlled sources in more detail in the later chapters.)

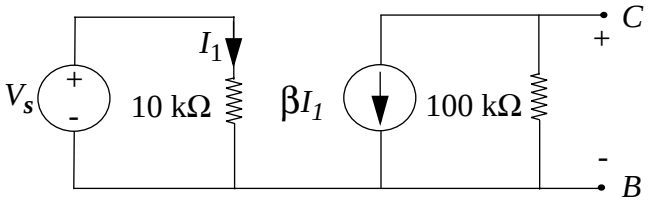


Figure 3.80:

b) Now suppose you connect a load resistor across the output of your equivalent circuit as shown in Figure 3.81. Find the value of R_L which will provide the maximum power transfer to the load.

Solution:

a) $R_{TH} = 100kOhms$

$v_T = v_{OC} = (100\ kOhms)(-\beta \frac{V_S}{10\ kOhms}) = -10\beta V_S$

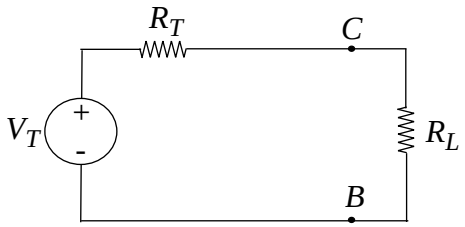


Figure 3.81:

b) $P = I^2R = R_L(\frac{V_T}{R_T+RL})^2 = V_T^2 R_L(R_T + R_L)^{-2}$

To maximize P, we write P as a function of R_L and set its derivative with respect to R_L equal to zero. So,

$P'(R_L) = V_T^2[(R_T + R_L)^{-2} - 2R_L(R_T + R_L)^{-3}] = 0$

$\Rightarrow R_L = R_T$

ANS:: (a) $R_{TH} = 100k\Omega$, $v_T = -10\beta V_S$ (b) $R_L = R_T$

Problem 3.14 You have been hired by the MITDAC Corporation to write a product description for a new 4-bit digital-to-analog-converter resistance ladder. Because of mask tolerances in VLSI chips, each resistor shown in Figure 3.82 is guaranteed to be only within 3% of its nominal value. That is, if R_0 is the nominal design resistance, then each resistance labeled R can have a resistance anywhere in the range $(1 \pm .03)R_0$ and each resistance labeled 2R can have a resistance anywhere in the range $(2 \pm .06)R_0$.

You are to write an *honest* description of the accuracy of this product. Remember that if you overstate the accuracy, your company will have many returns from dissatisfied customers, whereas if you understate the accuracy, your company won't have any customers.

NOTE: Part of this PROBLEM is to describe what the problem is: How should accuracy be specified? Is there an error level that is clearly unacceptable? Does your product avoid that error level? Is there an obvious "worst case" that can be easily analyzed? Have fun. And remember, common sense is an important ingredient of sound engineering.

Solution:

There are several approaches to this problem. This approach analyzed the circuit piece by piece to determine the effective error we can expect from the circuit.

Given: 3% tolerance, implies that $R = (1 \pm 0.03)R_0$, $2R = (2 \pm 0.06)R_0$.

Accuracy of $2R||2R$: high: $2.06||2.06 = 1.03$, low: $1.94||1.94 = 0.97$.

So the error for 2 $2R$ resistors in parallel is 3%.

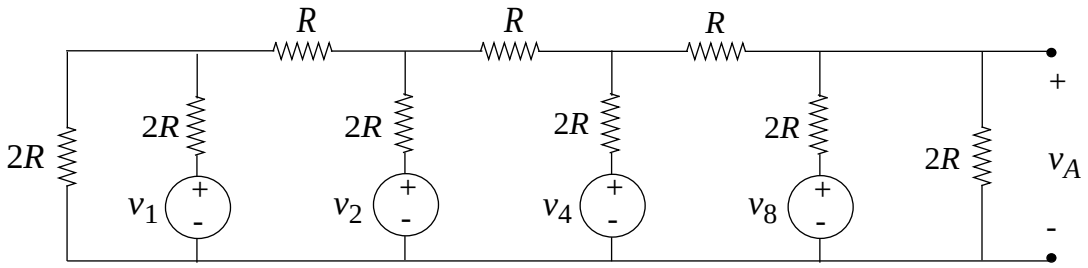
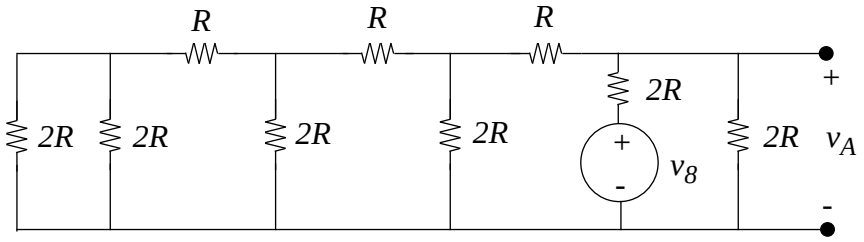


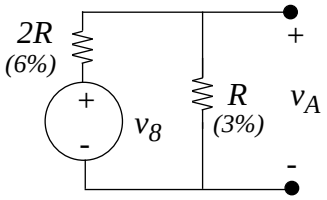
Figure 3.82:

Accuracy of $R + R$: high: $1.03 + 1.03 = 2.06$, low: $0.97 + 0.97 = 1.94$.

So the error for 2 R resistors in series is 6%.



(a)



(b)

Figure 3.83:

First, consider the highest-order bit (v_8) in isolation (see Figure 3.83(a)). We can simplify this circuit, keeping track of the effective errors incurred by taking the resistances in parallel and in series. The resulting simplified circuit is shown in Figure 3.83(b), with the effective errors of each resistor parenthesized.

We can now find the following voltage divider for v_A, considering the extreme error cases (high/low) in resistance values:

$$\frac{v_{A,h}}{v_8} = \frac{1 + 0.03}{2 - 0.06 + 1 + 0.03} = \frac{1 + 0.03}{3 - 0.03} = 0.38$$

$$\frac{v_{A,l}}{v_8} = \frac{1 - 0.03}{3 + 0.03} = 0.32$$

Now consider the lowest-order-bit (v_1) in isolation (see Figure 3.84. Again, we find voltage-divider relations:

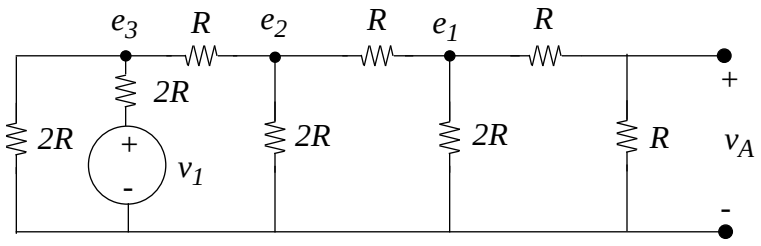


Figure 3.84:

$$\frac{v_{A,h}}{e_1} = \frac{1 + 0.03}{2} = 0.515$$
$$\frac{v_{A,l}}{e_1} = \frac{1 - 0.03}{2} = 0.485$$

And by symmetry:

$$\frac{v_{A,h}}{e_1} = \frac{e_{1,h}}{e_2} = \frac{e_{2,h}}{e_3}$$
$$\frac{v_{A,l}}{e_1} = \frac{e_{1,l}}{e_2} = \frac{e_{2,l}}{e_3}$$

Noting the similarity at e_3 to Figure 3.83(b):

$$\frac{e_{3,h}}{v_1} = \frac{v_{A,h}}{v_8}$$
$$\frac{e_{3,l}}{v_1} = \frac{v_{A,l}}{v_8}$$

We can now find the bit-conversion accuracies of the lowest-order bit:

$$\frac{v_{A,h}}{v_1} = \frac{v_{A,h}}{e_1} \cdot \frac{e_{1,h}}{e_2} \cdot \frac{e_{2,h}}{e_3} \cdot \frac{e_{3,h}}{v_1} = (0.515)^3 0.38$$

$$\frac{v_{A,l}}{v_1} = \frac{v_{A,l}}{e_1} \cdot \frac{e_{1,l}}{e_2} \cdot \frac{e_{2,l}}{e_3} \cdot \frac{e_{3,l}}{v_1} = (0.485)^3 0.32$$

Generalizing to a bit of order n:

$$\frac{v_{A,h}}{v_{2^n}} = 0.38 \cdot (0.515)^{3-n}$$

$$\frac{v_{A,l}}{v_{2^n}} = 0.32 \cdot (0.485)^{3-n}$$

Now consider the circuit as a whole. The worst case error-wise will be when all bits are "on". In this case:

$$v_{A,h} = 0.38 \cdot V_h \cdot (1 + 0.515 + 0.515^2 + 0.515^3) = 0.38 \cdot V_h \frac{1 - 0.515^4}{1 - 0.515} = 0.728 \cdot V_h$$

$$v_{A,l} = 0.32 \cdot V_h \cdot (1 + 0.485 + 0.485^2 + 0.485^3) = 0.32 \cdot V_h \frac{1 - 0.485^4}{1 - 0.485} = 0.587 \cdot V_h$$

As a point of comparison, the error-free case is: $v_A = \frac{5}{8} V_h = 0.625 \cdot V_h$.

Error high:

$$\frac{0.728 - 0.625}{0.625} = 16.5\%$$

Error low:

$$\frac{0.587 - 0.625}{0.625} = 6.1\%$$

Problem 3.15 You have a 6 volt battery (assumed ideal) and a 1.5 volt flashlight bulb, which is known to draw 0.5 amps when the bulb voltage is 1.5 volts (in Figure 3.85). Design a network of resistors to go between the battery and the bulb to give $v_s = 1.5$ volts when the bulb is connected, yet insures that v_s does not rise above 2 volts when the bulb is disconnected.

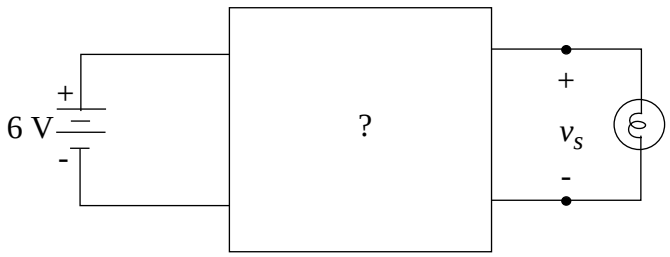


Figure 3.85:

Solution:

See Figure 3.86.

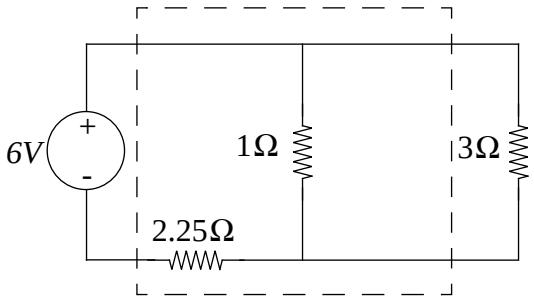


Figure 3.86:

The resistance of the bulb is $R_{BULB} = \frac{V}{I} = 3\ Ohms$.

When the bulb is connected, $v_S = (6\ V)\frac{\frac{(1\ Ohm)(3\ Ohms)}{1+3\ Ohms}}{2.25Ohms+\frac{(1\ Ohm)(3\ Ohms)}{1+3\ Ohms}} = 1.5\ V$

When the bulb is disconnected, $v_S = (6\ V)\frac{1\ Ohm}{1+2.25\ Ohms} = 1.85\ V$

Note: This scheme is not very practical, but it is simple.

Chapter 4

Analysis of Nonlinear Circuits

Exercises

Exercise 4.1 Consider a two-terminal nonlinear device (Figure 4.1) whose v-i characteristic is given by:

$$i_A = f(v_A) \tag{4.1}$$

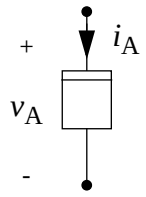


Figure 4.1:

Show that the incremental change in the current ($\Delta i_A = i_a$) for an incremental change in the voltage ($\Delta v_A = v_a$) at the DC operating point V_A, I_A is given by:

$$i_a = \left.\frac{df(v_A)}{dv_A}\right|_{v_A = V_A} \quad v_a$$

(Hint: Substitute $i_A = I_A + i_a$ and $v_A = V_A + v_a$ in Equation 4.1, expand using Taylor Series, ignore second order and higher terms in v_a, and equate corresponding DC and small signal terms.)

Solution:

$$i_A = f(v_A); i_A = I_A + i_a; v_A = V_A + v_a$$

Taylor series expansion (at V_A, I_A):

$$I_A + i_a = f(V_A) + \left.\frac{df}{dv_A}\right|_{v_A=V_A}(v_A - V_A) + \left.\frac{1}{2!}\frac{d^2f}{dv_A^2}\right|_{v_A=V_A}(v_A - V_A)^2 + ...$$

with: $v_a = v_A - V_A$, and ignoring high-order terms:

$$I_A + i_a = f(V_A) + \left.\frac{df}{dv_A}\right|_{v_A=V_A} v_a$$

Equating DC and small-signal components, we have: DC:

$$I_A = f(V_A)$$

Small-signal:

$$i_a = \left.\frac{df}{dv_A}\right|_{v_A=V_A} v_a$$

Exercise 4.2 Suppose the two-terminal nonlinear device from the previous exercise (Figure 4.1) has the following v-i characteristic:

$$i_A = f(v_A) = c_X v_A^2 + c_Y v_A + c_Z \;\; for \;\; v_A \geq 0, \; and \; f(v_A) = 0 \;\; otherwise$$

a) Find the operating point current I_A for an operating point voltage V_A, where $V_A > 0$.

b) Find the incremental change in the current i_a for an incremental change in the voltage v_a at the operating point V_A, I_A.

c) By what fraction does i_a change for a y percent change in v_a.

d) Suppose the nonlinear device is biased at V_A' instead of V_A, where V_A' is y percent greater than V_A. Find the incremental change in the current (i_a') for an incremental change in the voltage (v_a) at this new bias point. By what fraction is i_a' different from the i_a calculated in part (b).

e) Find the incremental change in the current i_{acx} for an incremental change in the parameter c_X (given by $\Delta c_X = c_x$) from its nominal value of C_X, assuming the operating point v-i values are V_A, I_A.

Hint: Observe that if i_A depends on the parameters x_A and y_B, in other words,

$$i_A = f(x_A, y_B),$$

then the incremental change in i_A for an incremental change in y_B is given by

$$i_{ayb} = \left.\frac{\delta f(x_A, y_B)}{\delta y_B}\right|_{y_B = Y_B} y_b$$

Solution:

a)

$$I_A = f(V_A)$$
$$= C_X V_A^2 + C_Y V_A + C_Z$$

b)

$$i_a = \left.\frac{df}{dv_A}\right|_{v_A = V_A} v_a$$
$$= [2c_x v_A + c_Y]_{v_A = V_A} \cdot v_A$$
$$i_a = v_a \cdot [2c_X V_A + c_Y]$$

c) For a y% change in $v_a : v_a' = (1 + \frac{y}{100}) v_a$,

$$i_a' = v_a' \cdot [2c_x V_A + c_Y]$$
$$i_a' = (1 + \frac{y}{100})(2c_X V_A + c_Y) v_a$$
$$\frac{i_a'}{i_a} = 1 + \frac{y}{100}$$

$\Rightarrow$ so i_a also changes by y%. This is expected since $i_a = f(v_a)$ is linear.

d) Incremental change at new bias point:

$$V_A' = (1 + \frac{y}{100}) V_A$$
$$i_a' = v_a(2c_X V_A' + c_Y)$$

Different from part (b):

$$\frac{i_a'}{i_a} = \frac{(2c_X V_A' + c_Y) \cdot v_a}{(2c_X V_A + c_Y) \cdot v_a}$$
$$= \frac{2c_X(1 + \frac{y}{100}) v_A + c_Y}{2c_X V_A + c_Y}$$
$$= \frac{(2c_X V_A + c_Y) + (2c_X V_A)(\frac{y}{100})}{(2c_X V_A + c_Y)}$$
$$\frac{i_a'}{i_a} = 1 + \frac{2c_X V_A (\frac{y}{100})}{2c_X V_A + c_Y}$$

e)

$$i_{acx} = \frac{\partial f(c_X, c_Y, c_Z)}{\partial c_X}\Big|_{c_X=C_X} \cdot c_X$$
$$= [v_A^2]_{c_X=C_X} \cdot c_X$$
$$= c_X \cdot (v_A)^2$$

At operating point:

$$i_{acx} = c_X \cdot (V_A)^2$$

ANS:: (a) $c_X V_A^2 + C_Y V_A + C_Z$ (b) $v_a \cdot [2c_X V_A + c_Y]$ (c) y% (d) $i'_a = v_a(2c_X V'_A + c_Y)$, $\frac{i'_a}{i_a} = 1 + \frac{2c_X V_A(\frac{y}{100})}{2c_X V_A + c_Y}$ (e) $i_{acx} = c_X \cdot (V_A)^2$

Exercise 4.3 The nonlinear device (NLD) in the circuit in Figure 4.2 has the $v - i$ characteristics shown. Find the operating point i_D and v_D for $R = 910\Omega$.

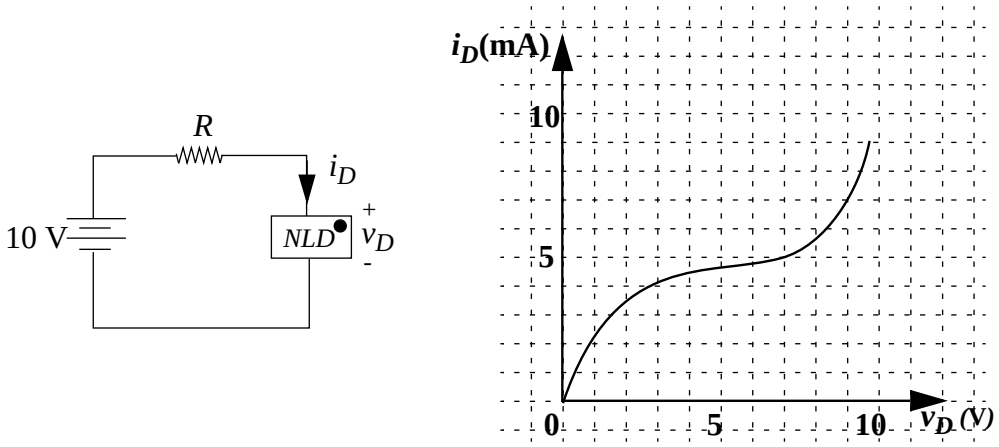


Figure 4.2:

Solution:

KVL:

$$10V - i_D \cdot\ 910 - v_D = 0$$
$$i_D = -1.1 \cdot\ v_D + 10.99mA$$

Draw this load line on graph.

Intersection of it and NLD $i - v$ plot is operating point.

$$i_D = 4.7mA$$

$$v_D = 5.7V$$

ANS:: $i_D = 4.7$ mA, $v_D = 5.7$ V

Exercise 4.4

a) Plot the i_A vs. v_A characteristics for the nonlinear network shown in Figure 4.3. Assume the diode is ideal.

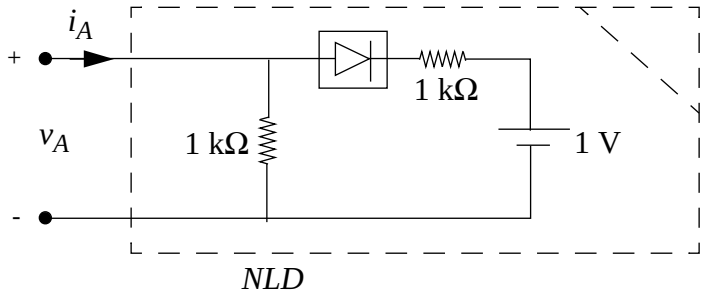


Figure 4.3:

b) The nonlinear network from part (a) is connected as shown in Figure 4.4. Draw the load line on your $i - v$ characteristic from part (a), and find i_T.

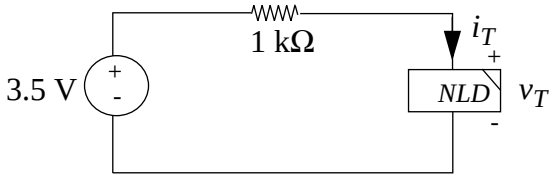


Figure 4.4:

Solution:

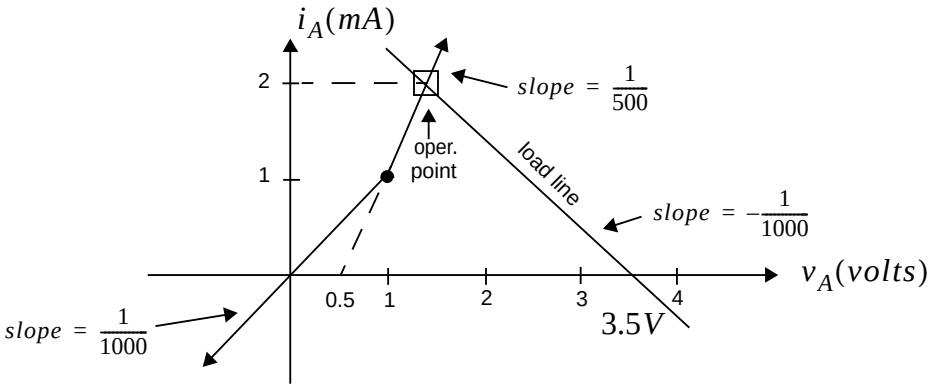


Figure 4.5:

a) $v_A > 1$: Diode on

$$i_A = \frac{v_A}{1000 \,||\, 1000}$$

$v_A < 1$: Diode off

$$i_A = \frac{v_A}{1000}$$

b) Load line:

KVL:

$$3.5V - i_T\,(1000) - v_T = 0$$

$$i_T = \frac{3.5 - v_T}{1000}$$

Operating point occurs at intersection, and we find that

$$i_T = 2mA$$

ANS:: (b) $i_T = 2$mA

Exercise 4.5 Consider two identical semiconductor diodes, each of which has an $i - v$ relation:

$$i_D = I_S(e^{v_D/V_{TH}} - 1) \tag{4.2}$$

a) Find the relation of i to v for the pair connected in parallel as shown in Figure 4.6a.

(a) (b)

Figure 4.6:

b) Find the relation of i to v for the pair connected in series as shown in Figure 4.6b.

Solution:

a) The currents add, so the i-v graphs may be vertically added - so if the two devices are identical, the output is merely twice the output of each individual device, since we would replace the vertical coordinate i with $\frac{i}{2}$.

$$i = i_{D1} + i_{D2} = 2 \cdot \ I_s \left(e^{q \cdot V_D / KT} - 1 \right)$$

b) Here, the two devices are in series, so the voltages add. Since the two devices are identical, the horizontal addition is the same as replacing the original v coordinate with $\frac{v}{2}$.

$$i = I_s \left(e^{q \cdot V_D / 2KT} - 1 \right)$$

ANS:: (a) $i = 2 \cdot \ I_s \left(e^{q \cdot V_D / KT} - 1 \right)$, (b) $i = I_s \left(e^{q \cdot V_D / 2KT} - 1 \right)$

Exercise 4.6 For the circuit in Figure 4.7, find the input characteristic, i versus v, and the transfer characteristic i_2 versus v. I is fixed and positive. Express your results in graphs, labeling all slopes, intercepts, and coordinates of any break points.

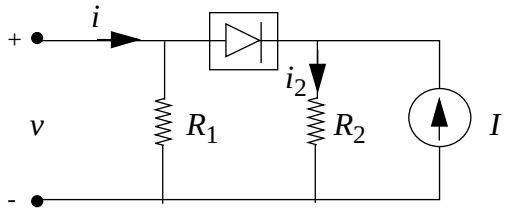


Figure 4.7:

Solution:

Note: when diode is on,

$$i_2 = (I + i) \frac{R_1}{R_1 + R_2}$$

But

$$i = \frac{V \ (R_1 + R_2)}{R_1 \ R_2}$$

$$i_2 = \frac{I \cdot \ R_1}{R_1 + R_2} + \frac{V (R_1 + R_2) R_1}{(R_1 + R_2) R_1 \ R_2}$$

$$i_2 = \frac{V}{R_2} + \frac{I \cdot \ R_1}{R_1 + R_2}$$

as graph shows.

ANS:: $i_2 = \frac{V}{R_2} + \frac{I \cdot \ R_1}{R_1 + R_2}$

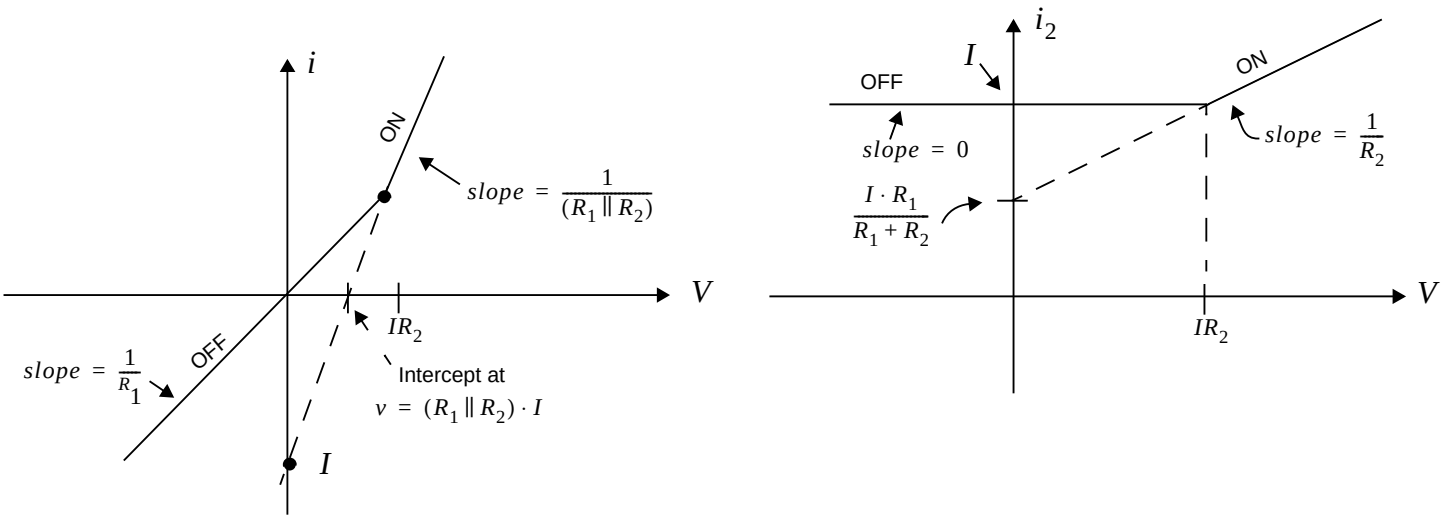


Figure 4.8:

Exercise 4.7 For the circuit in Figure 4.9 and the values shown below, sketch the waveform of $i(t)$. On your sketch, show when the ideal diode is on and when it is off.

$v_i = 10 \sin t \quad V_0 = 5V \quad R = 1\Omega$

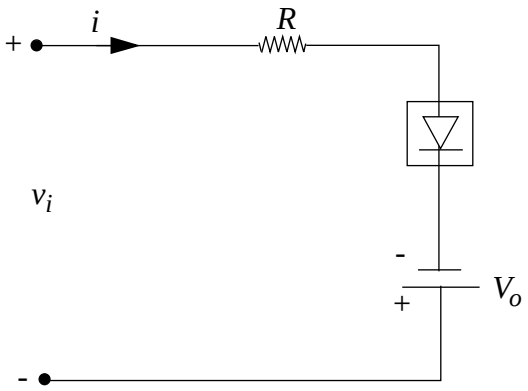


Figure 4.9:

Solution:

Diode on:

$$i(t) = (V_1(t) + 5V)/R$$

Diode off:

$$i(t) = 0$$

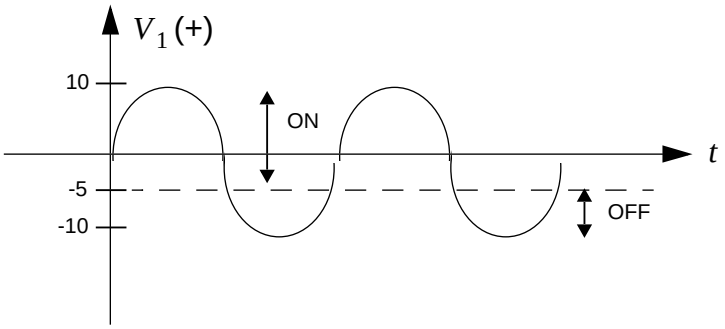


Figure 4.10:

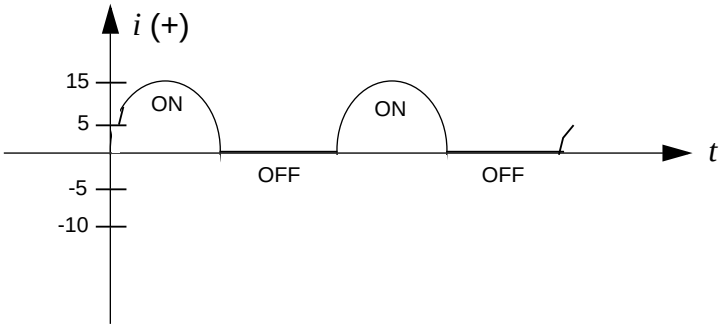


Figure 4.11:

ANS:: Diode on: $(i(t) = V_1(t) + 5V)/R$; Diode off: $i(t) = 0$

Problems

Problem 4.1 Consider the circuit containing a nonlinear element N as shown in Figure 4.12. The i-v relation for N is given by:

$$i_A = c_2 v_A^2 + c_1 v_A + c_0 \;\; for \;\; v_A \geq 0, \; and \; i_A = 0 \;\; otherwise$$

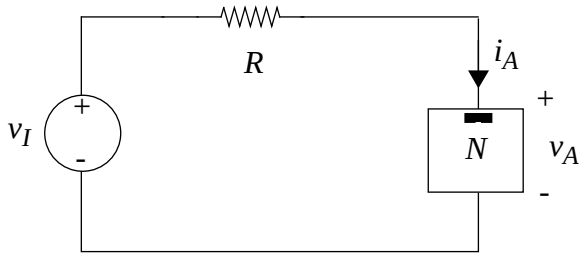


Figure 4.12:

a) Solve for i_A and v_A using the analytical method.

b) Find the operating point values of the nonlinear element's voltage and current for $v_I = V_I$, where V_I is positive.

c) Find the incremental change in i_A (given by i_a) for an incremental change in v_I (given by v_i).

d) Determine the incremental change in the voltage across the resistor R for an incremental change in the input v_I (given by v_i).

e) Find the incremental change in i_A for a 2% increase in the value of R.

f) Find the incremental change in i_A for an incremental change in v_A at the bias point V_A, I_A.

g) Suppose we replace the source v_I with a DC voltage V_I in series with a small time varying voltage $v_i = v_o cos\omega t$. Determine the time varying component of i_A.

h) Suppose we now replace $v_I = V_I + v_i$, where $V_I = 10$ volts and $v_i = 1$ volt.

i) Find the bias point DC current I_A corresponding to $V_I = 10$ volts.

ii) Find the value of i_a corresponding to $v_i = 1$ volt using small signal analysis.

iii) Find the value of i_A using small signal analysis. (Use $i_A = I_A + i_a$).

iv) Find the value of i_A using the analytical method for $v_I = V_I + v_i = 11$ volts.

v) Now, find the exact value of the i_a using $i_a = i_A - I_A$.

vi) What is the error in the value of i_a computed using the small signal method?

Solution:

a) $v_A = v_I - i_A R$

$v_A = v_I - R(c_2 v_A^2 + c_1 v_A + c_0)$

$Rc_2 v_A^2 + (Rc_1 + 1)v_A + (Rc_0 - v_I) = 0$

$v_A = \frac{-(Rc_1+1) \pm \sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - v_I)}}{2Rc_2}$

$v_A = \frac{\sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - v_I)} - (Rc_1+1)}{2Rc_2}$ for $v_I \geq Rc_0$; $V_A = V_I$ otherwise

$i_A = \frac{2Rc_2 v_I + Rc_1 + 1 - \sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - v_I)}}{2R^2 c_2}$ for $v_I \geq Rc_0$; $i_A = 0$ otherwise

b) $V_A = \frac{\sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - V_I)} - (Rc_1+1)}{2Rc_2}$

$I_A = \frac{2Rc_2 V_I + Rc_1 + 1 - \sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - V_I)}}{2R^2 c_2}$

c) $\frac{\triangle i_a}{\triangle v_i} = \frac{1}{R}\left(1 - \frac{1}{\sqrt{(Rc_1+1)^2 + 4R^2 c_0 c_2 + 4Rc_2 V_I}}\right)$

d) $v_r = i_a R$

$\frac{\triangle v_r}{\triangle v_i} = R\left(\frac{\triangle i_a}{\triangle v_i}\right) = 1 - \frac{1}{\sqrt{(Rc_1+1)^2 + 4R^2 c_0 c_2 + 4Rc_2 V_I}}$

e) $\triangle i_A = \frac{1}{1.02R}\left(v_I - \frac{\sqrt{(1.02Rc_1+1)^2 - 4.08Rc_2(1.02Rc_0 - v_I)} - (1.02Rc_1+1)}{2c_2(1.02R)^2}\right) - \frac{1}{R}\left(v_I - \frac{\sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - v_I)} - (Rc_1+1)}{2c_2 R^2}\right)$

f) $\frac{di_A}{dv_A} = 2c_2 V_A + c_1$; $V_A \geq 0$

g) Incremental model of N is a resistor r_N

$r_N = \left(\frac{di_A}{dv_A}\right)^{-1} = \frac{1}{2c_2 V_A + c_1}$

$i_a = \frac{v_i}{R + r_N} = \frac{\frac{v_0 \cos \omega t}{R}}{R + \frac{1}{\sqrt{(Rc_1+1)^2 - 4Rc_2(Rc_0 - V_I) - 1}}}$

h) i) $I_A = \frac{20Rc_2+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2}$

ii) $i_a = \frac{\frac{1}{R}}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)-1}}}$

iii) $i_A = \frac{20Rc_2+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2} + \frac{\frac{1}{R}}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)-1}}} = I_A + i_a =$

iv) $i_A = \frac{22Rc_2+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-11)}}{2R^2c_2}$

v) $i_a = \frac{2Rc_2-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-11)}+\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2}$

vi) error is: $\frac{\frac{1}{R}}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)-1}}} - \frac{2Rc_2-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-11)}+\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2}$

ANS:: (a)$i_A = \frac{2Rc_2v_I+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-v_I)}}{2R^2c_2}$ for $v_I \geq Rc_0; i_A = 0$ otherwise, $v_A = \frac{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-v_I)}-(Rc_1+1)}{2Rc_2}$ for $v_I \geq Rc_0, V_A = V_I$ otherwise (b) $V_A = \frac{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-V_I)}-(Rc_1+1)}{2Rc_2}$, $I_A = \frac{2Rc_2V_I+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-V_I)}}{2R^2c_2}$ (c) $\frac{\triangle i_a}{\triangle v_i} = \frac{1}{R}(1 - \frac{1}{\sqrt{(Rc_1+1)^2+4R^2c_0c_2+4Rc_2V_I}})$ (d) $1 - \frac{1}{\sqrt{(Rc_1+1)^2+4R^2c_0c_2+4Rc_2V_I}}$ (e) $\triangle i_A = \frac{1}{1.02R}(v_I - \frac{\sqrt{(1.02Rc_1+1)^2-4.08Rc_2(1.02Rc_0-v_I)}-(1.02Rc_1+1)}{2c_2(1.02R)^2}) - \frac{1}{R}(v_I - \frac{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-v_I)}-(Rc_1+1)}{2c_2R^2})$ (f) $\frac{di_A}{dv_A} = 2c_2V_A + c_1;\ V_A \geq 0$ (g) $r_N = \frac{1}{2c_2V_A+c_1}$, $i_a = \frac{v_0 \cos \omega t}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-V_I)-1}}}$ (h) (i) $I_A = \frac{20Rc_2+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2}$ (ii) $i_a = \frac{\frac{1}{R}}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)-1}}}$ (iii) $i_A = \frac{20Rc_2+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2} + \frac{\frac{1}{R}}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)-1}}}$ (iv) $i_A = \frac{22Rc_2+Rc_1+1-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-11)}}{2R^2c_2}$ (v) $i_a = \frac{2Rc_2-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-11)}+\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2}$ (vi) $\frac{\frac{1}{R}}{R+\frac{1}{\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)-1}}} - \frac{2Rc_2-\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-11)}+\sqrt{(Rc_1+1)^2-4Rc_2(Rc_0-10)}}{2R^2c_2}$

Problem 4.2 The circuit shown in Figure 4.13 contains two nonlinear devices and a current source. The characteristics of the two devices are given. Determine the voltage, v, for (a) $i_S = 1$ amp, (b) $i_S = 10$ amps, (c) $i_S = 1\ cos\ t$ (in amperes).

Solution:

(See Figure 4.14)

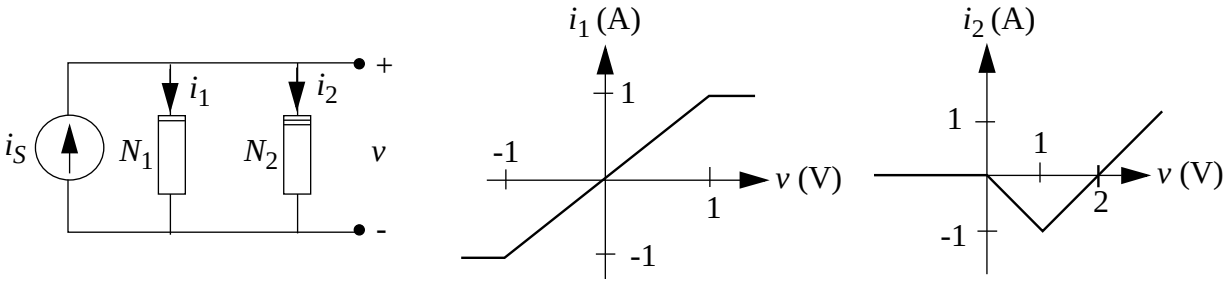


Figure 4.13:

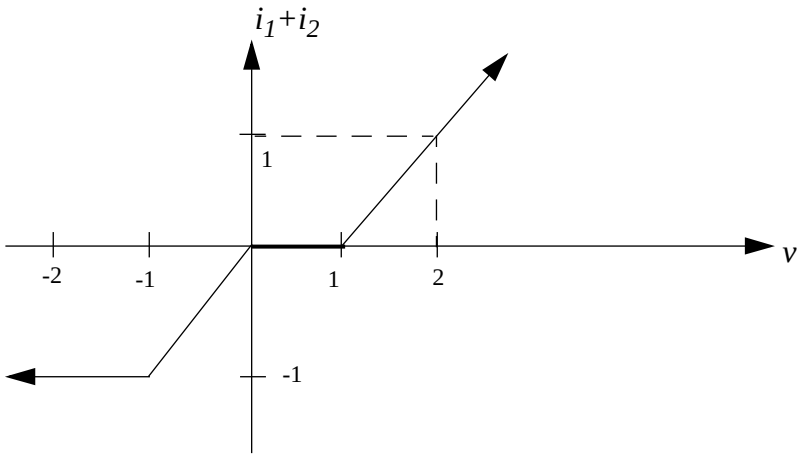


Figure 4.14:

a) 2

b) 11

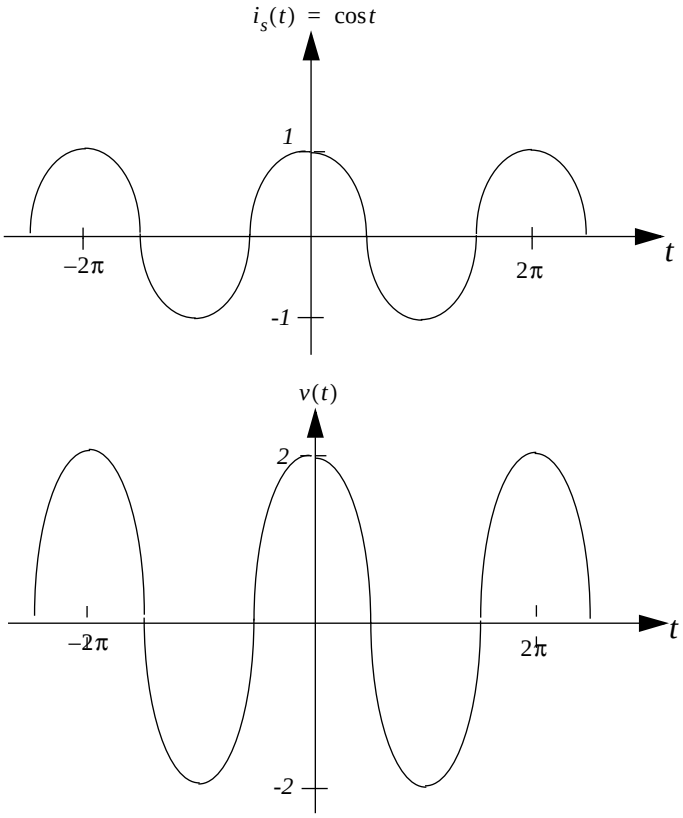


Figure 4.15:

c) See Figure 4.15.

ANS:: (a) 2 (b) 11

Problem 4.3 A plot (hypothetical) of the v-i characteristics, (terminal voltage as a function of the current drawn *out*, and *NOT* its associated variables) for a battery is shown in Figure 4.16(a).

a) If a 2 ohm resistor is connected across the battery terminals, find the terminal voltage of the battery and the current through the resistor.

b) A light bulb is a nonlinear resistance because of self-heating effects. A hypothetical i-v plot is shown in Figure 4.16(b). Find the bulb current and bulb voltage if the lamp is connected to the battery.

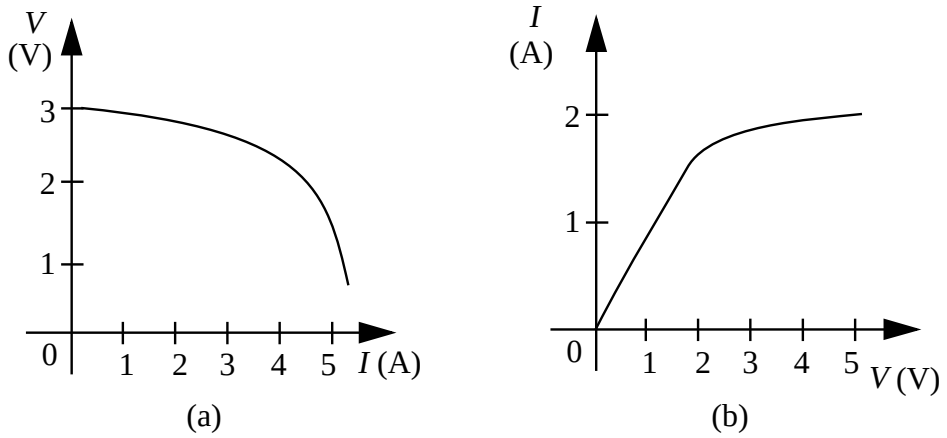


Figure 4.16:

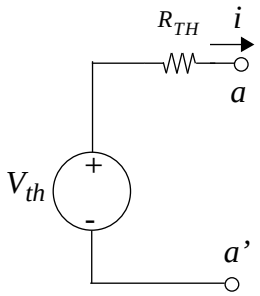
c) Devise a piecewise-linear model for the battery which is reasonably accurate over the current range 0-2 amp.

d) Use this piecewise-linear battery model to find the battery voltage and bulb current if the bulb and 2 ohm resistor are connected in series to the battery.

Solution:

a) $i \approx 1.4$ amps; $v \approx 2.8$ volts

b) $i \approx 1.9$ amps; $v \approx 2.9$ volts



V_{th} = 3 V
R_{th} = 0.1 ohms
$0 \le i \le 2$ amps

Figure 4.17:

c) see Figure 4.17. $V_{TH} = 3$ volts; $R_{TH} = 0.1\Omega$

d) $i \approx 1$ amp; $v \approx 3$ volts

ANS:: (a) $i \approx 1.4$ amps; $v \approx 2.8$ volts (b) $i \approx 1.9$ amps; $v \approx 2.9$ volts (d) $i \approx 1$ amp; $v \approx 3$ volts

Problem 4.4

a) Assuming the diode can be modeled as an ideal diode, and $R_1 = R_2$, plot the waveform $v_o(t)$ for the circuit in Figure 4.18, assuming a triangle wave input. Write an expression for $v_o(t)$ in terms of v_i, R_1 and R_2.

b) If the triangle wave has a peak amplitude of only 2 volts, and $R_1 = R_2$, a more accurate diode model must be used. Plot and write an expression for v_o assuming that the diode is modeled using an ideal diode in series with a 0.6 volt source. Draw the transfer curve v_o versus v_i.

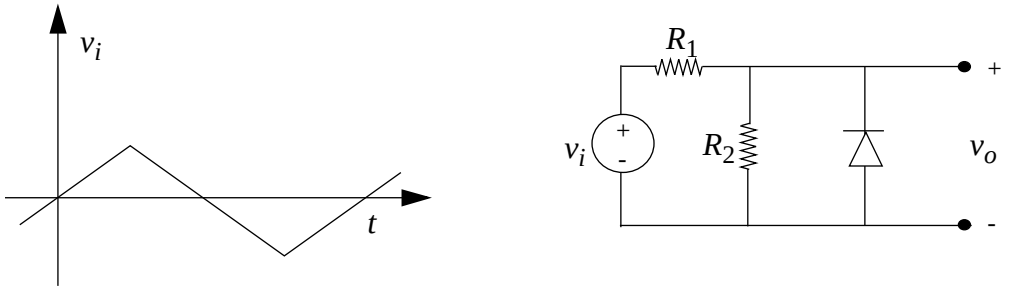


Figure 4.18:

Solution:

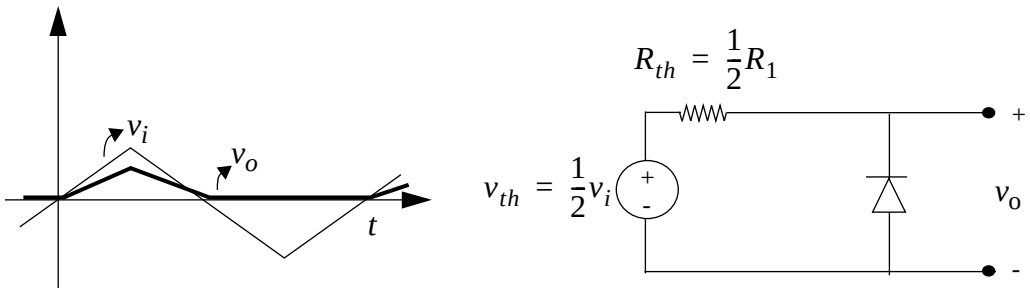


Figure 4.19:

a) see Figure 4.19. $v_o = \frac{1}{2}v_i$ for $v_i > 0$, and $v_o = 0$ otherwise

b) See Figure 4.20. $v_o = \frac{1}{2}v_i$ for $v_i > -1.2$, and $v_o = -0.6$ otherwise

ANS:: (a) $v_o = \frac{1}{2}v_i$ for $v_i > 0$, and $v_o = 0$ otherwise (b) $v_o = \frac{1}{2}v_i$ for $v_i > -1.2$, and $v_o = -0.6$

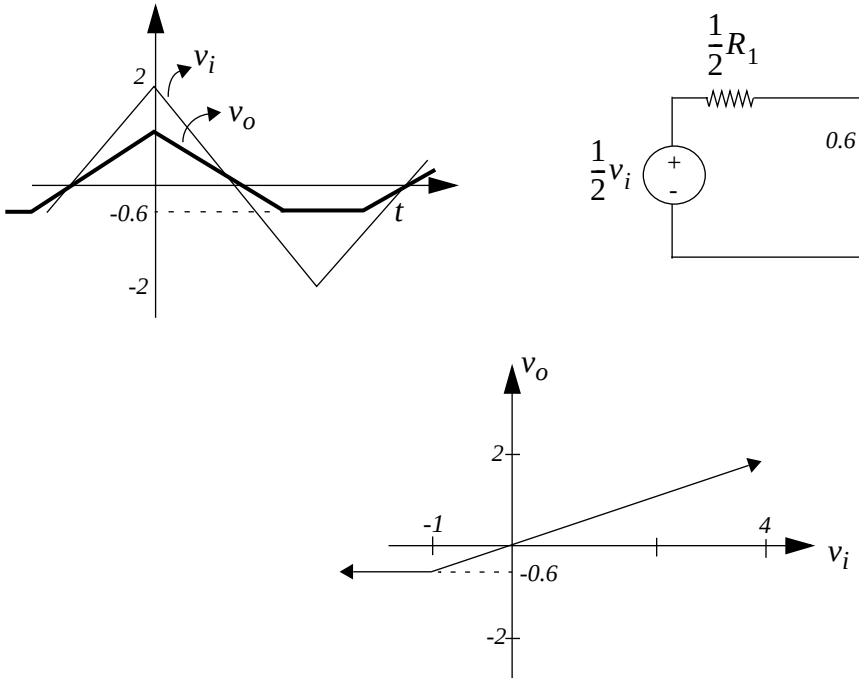


Figure 4.20:

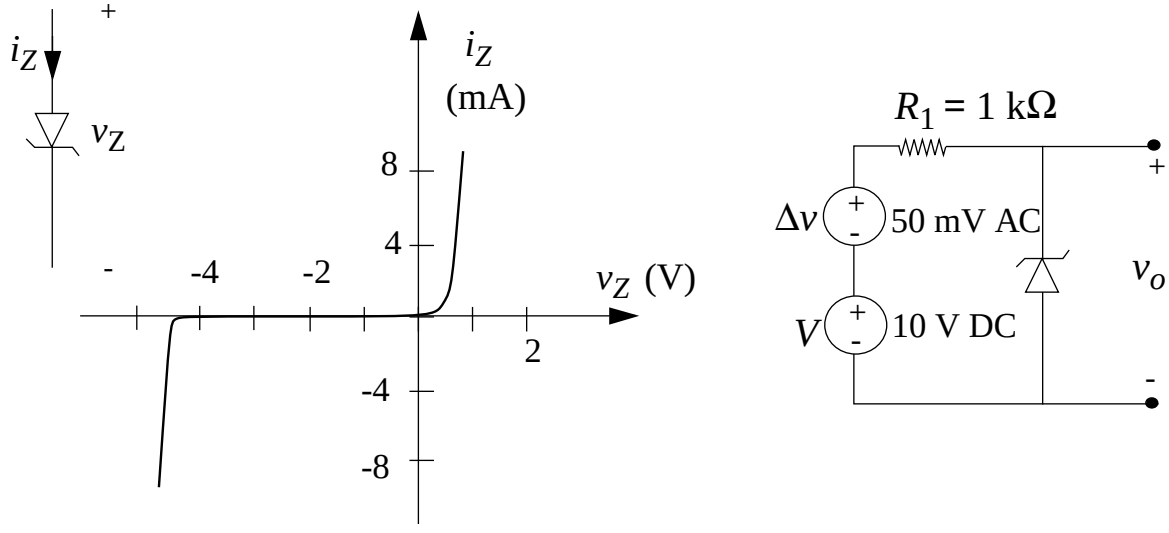


Figure 4.21:

Problem 4.5 Figure 4.21 is an illustration of a crude Zener-diode regulator circuit.

a) Using incremental analysis, estimate from the graph an analytical expression for v_o in terms of V and Δv.

b) Calculate the amount of DC and the amount of AC in the output voltage using the Zener diode characteristic to find model values. Numbers, please.

c) What is the Theévenin output resistance of the power supply, that is, the Thévenin resistance seen looking in at the v_o terminals.

Solution: Assume 20mA/V for forward bias, 40mA/V for reverse breakdown.

a) $v_o = 0.024 \triangle v$

b) DC: 4.5 V AC: 1.2 mV

c) 25Ω

ANS:: (a) $v_o = 0.024 \triangle v$ (b) DC: 4.5 V AC: 1.2 mV (c) 25Ω

Problem 4.6 The terminal voltage-current characteristic of a *single* solar cell is shown in Figure 4.22a. Note that this is a sketch of the terminal voltage as a function of current drawn out (i.e. not the associated variable convention). An array is made by connecting a total of 100 such cells as follows: Ten solar cells are connected in series. Ten sets of these are made. These ten series strips are then connected in parallel (see Figure 4.22b).

If a 3 ohm resistor is connected across this new two-terminal element (the 100 cell array), determine the terminal voltage across and the current through the resistor.

Solution:

The act of combining 10 in series causes the graph to stretch vertically by a factor of 10, and the act of combining 10 in parallel stretches it horizontally by 10. So one intersects this new graph with a line of slope 3, and gets the approximate intersection point of $(1.7, 5.1)$

$V = 5.1$ volts; $I = 1.7$ amps

ANS:: $V = 5.1$ volts; $I = 1.7$ amps

Problem 4.7 The junction field-effect transistor (JFET) with the specific connection shown in Figure 4.23a (gate and source shorted together) behaves as a two-terminal device. The $v_D - i_D$ characteristics of the resulting two-terminal device shown in Figure 4.23b saturates at current I_{DSS} for v_D greater than a voltage V_P, called the pinch-off voltage. In the two-terminal configuration shown, the JFET characteristic is

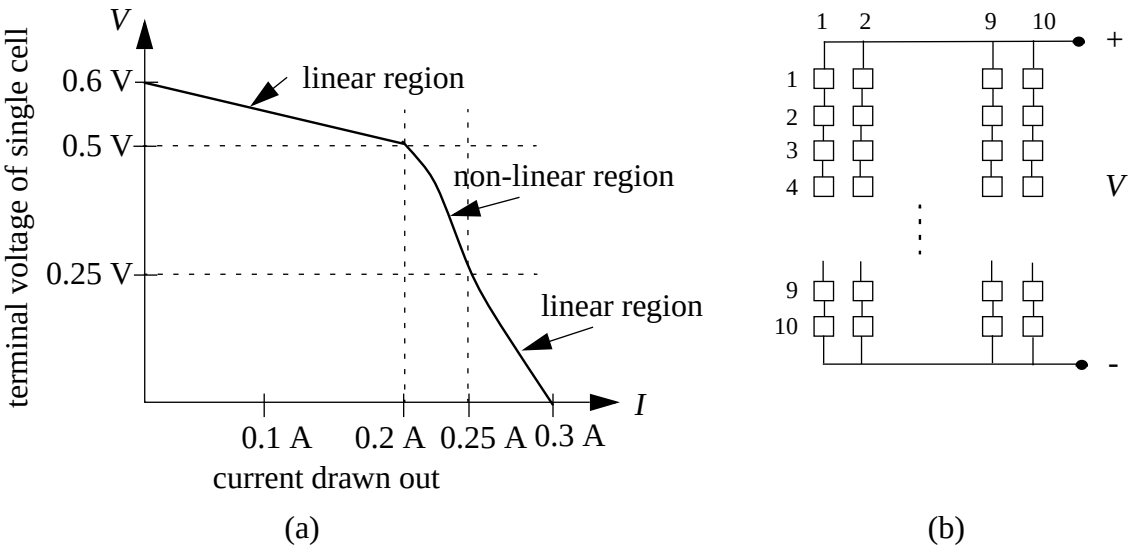


Figure 4.22:

$$i_D = I_{DSS}\left[2(v_D/V_P) - (v_D/V_P)^2\right] \quad \text{for} \;\; v_D \leq V_P$$

and

$$i_D = I_{DSS} \quad \text{for} \;\; v_D > V_P$$

As illustrated in Figure 4.23c, this two-terminal device can be used to make a well-behaved dc current source, even starting with a ripple-containing power supply (depicted as v_S), as would be obtained from ordinary rectifier circuits. Suppose the voltage source v_S has an average value V_S and a 60 Hz "ripple component", $v_r = a\cos\omega t$ as shown in Figure 4.23d.

a) First assume that there is no ripple ($a = 0$). Find the current i through the resistor R as a function of V_S for a value of $R = 1k\Omega$. At what value of V_S does the current stabilize at I_{DSS}? How would this value change if R were doubled in value? Explain.

b) Now assume $a = 0.1V$ and $R = 1k\Omega$. Make reasonable approximations to find the current waveform when $V_S = 5V, V_S = 10V$, and $V_S = 15V$. Determine in each case the average value of the current i and the magnitude and frequency of the largest sinusoidal component of the current.

Solution:

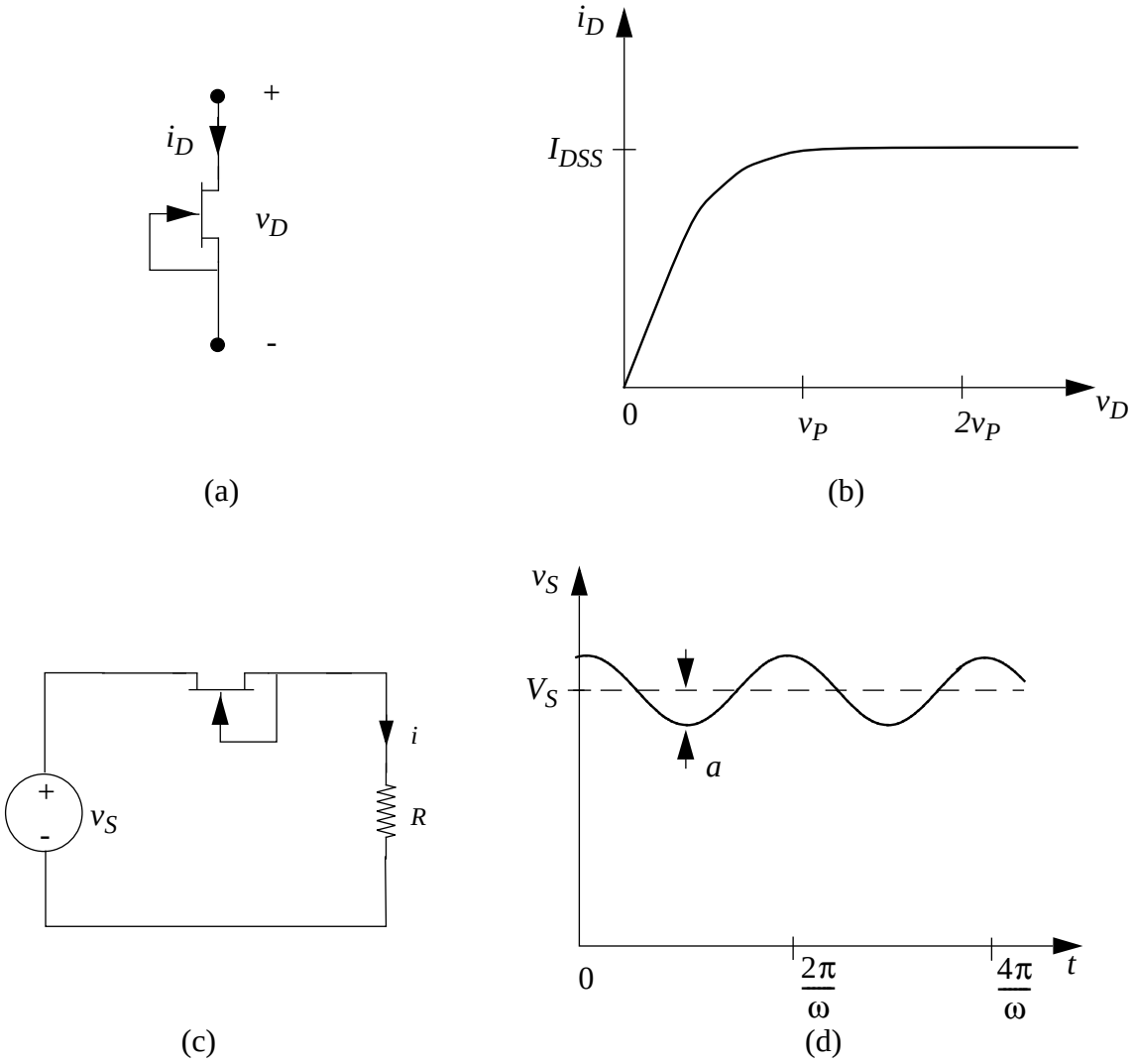

+
i_D
v_D
-
(a)
i_D
I_{DSS}
0
v_P
$2v_P$
v_D
(b)
+
-
v_S
i
R
(c)
v_S
V_S
a
0
$\frac{2\pi}{\omega}$
$\frac{4\pi}{\omega}$
t
(d)

Figure 4.23:

a) $i = \frac{2V_S - (\frac{V_P^2}{RI_{DSS}} + 2V_P) + \sqrt{(\frac{V_P^2}{RI_{DSS}} + 2V_P)^2 - \frac{4V_P^2 V_S}{RI_{DSS}}}}{2R}$ for $V_S < V_P + I_{DSS}R$; The current stabilizes at I_{DSS} when $V_S \geq V_P + I_{DSS}R$

b) $I_{DSS} = 5mA$, $V_P = 5V$

When $V_S = 5V$, $i_{average} = 3.1mA$, largest sinusoidal component has frequency ω, magnitude $0.056mA$

When $V_S = 10V$, $i_{average} = 5mA$, largest sinusoidal component has frequency 2ω, magnitude $0.002mA$

When $V_S = 15V$, $i_{average} = 5mA$, no sinusoidal component present

ANS:: Assume $I_{DSS} = 5mA$ and $V_P = 5V$. (a) $i = \frac{2V_S - (\frac{V_P^2}{RI_{DSS}} + 2V_P) + \sqrt{(\frac{V_P^2}{RI_{DSS}} + 2V_P)^2 - \frac{4V_P^2 V_S}{RI_{DSS}}}}{2R}$ for $V_S < V_P + I_{DSS}R$ (b) $V_S = 5V; i_{average} = 3.1mA$, $V_S = 10V; i_{average} = 5mA$, $V_S = 15V; i_{average} = 5mA$

Problem 4.8 The current-voltage characteristic of a photovoltaic energy converter (solar cell) can be approximated by

$$i = I_1(e^{v/V_{TH}} - 1) - I_2$$

where the first term characterizes the diode in the dark and I_2 is a term that depends on light intensity.

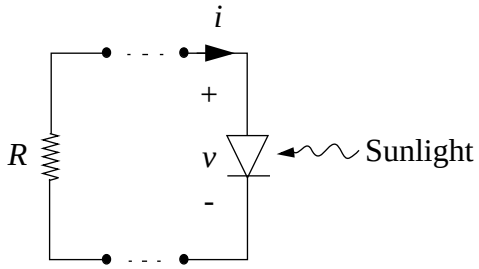


Figure 4.24:

Assume $I_1 = 10^{-9}$ and assume light exposure such that $I_2 = 10^{-3}A$.

a) Plot the i-v characteristic of the solar cell. Be sure to note the values of open-circuit voltage and short-circuit current. (Note, however, that the characteristic is clearly nonlinear. Therefore, Thévenin or Norton equivalents *do not apply*.)

b) If it is desired to maximize the power that the solar cell can deliver to a resistive load, determine the optimum value of the resistor. How much power can this cell deliver?

Solution:

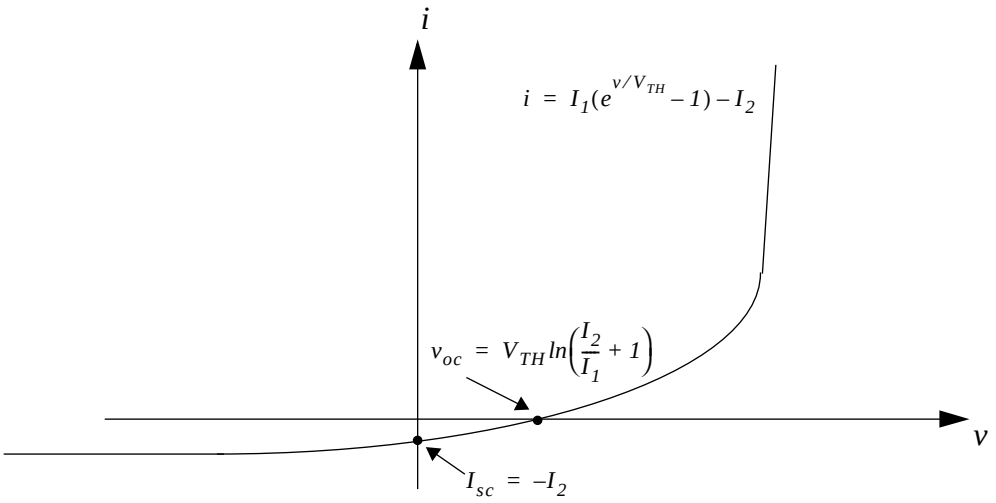


Figure 4.25:

a) See Figure 4.25. $I_{SC} = -I_2$; $V_{OC} = V_{TH} \ln(\frac{I_2}{I_1} + 1)$

b) $R_{OPTIMUM} = 30$ ohms; Maximum power = 2.6 mW

ANS:: (b) $R_{OPTIMUM} = 30$ ohms; Maximum power = $2.6mW$

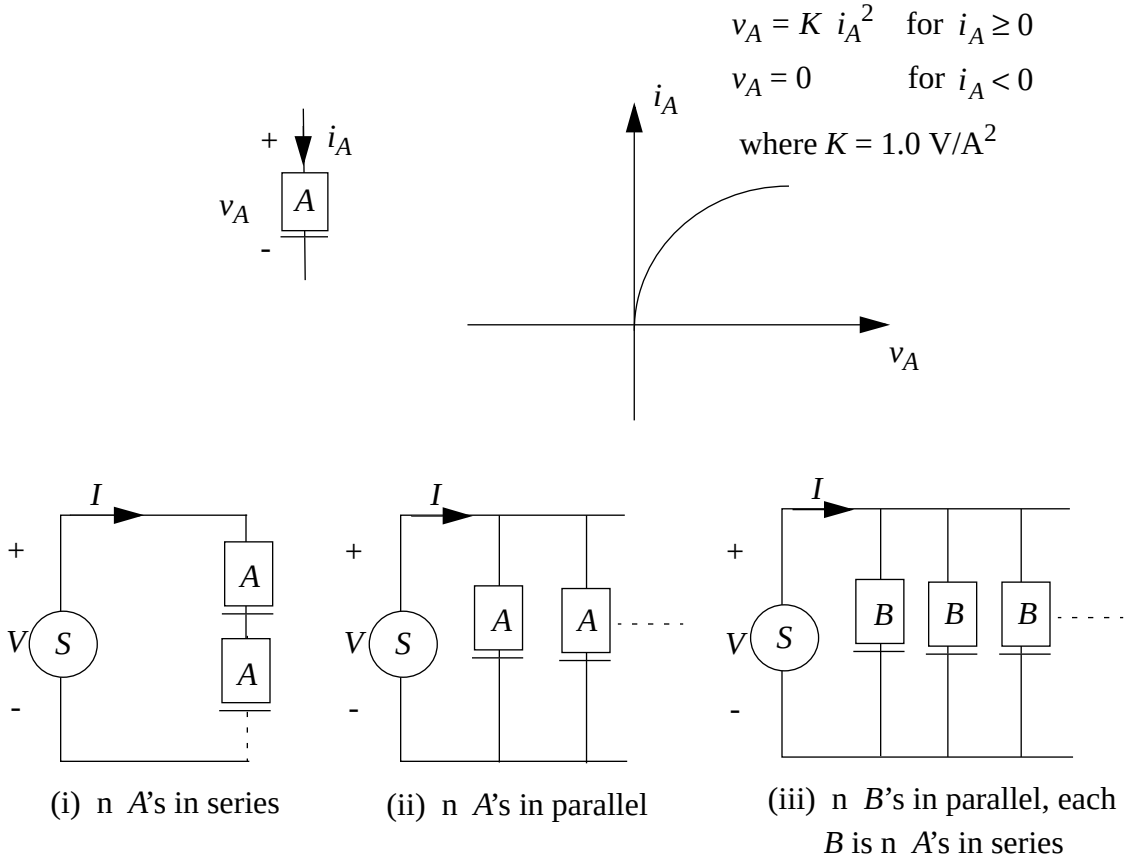
Problem 4.9

a) A nonlinear device has i-v characteristics shown in Figure 4.26. Assuming that S is an ideal voltage source, which connection, (i), (ii) or (iii) consumes most power? What if S is an ideal current source?

b) Another crazy device, C, with v-i characteristics as shown in Figure 4.27, is introduced. If device A and device C are connected in series across an ideal voltage source of 6 volts, what is the current flow in the circuit? (You can either solve it analytically or graphically.)

Solution:

a) ii) consumes the most power. If S is a current source, i) consumes the most power.



(i) n *A*'s in series (ii) n *A*'s in parallel (iii) n *B*'s in parallel, each *B* is n *A*'s in series

Figure 4.26:

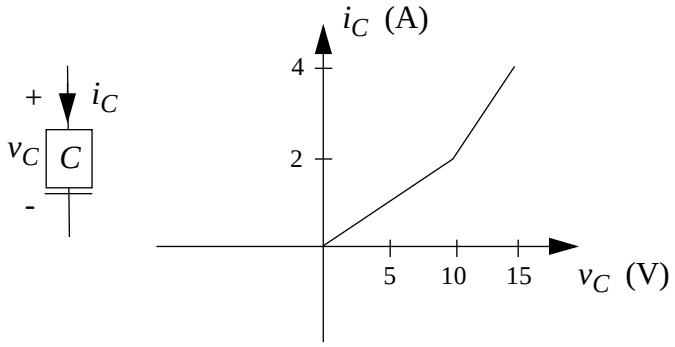


Figure 4.27:

b) 1 Ampere

ANS:: (a) ii; if S current source, i (b) $1 Ampere$

Problem 4.10 In the circuit in Figure 4.28, assume $v_1 = 0.5V$ and $v_2 = A_2 \cos \omega t$, where $A_2 = 0.001V$. Assume further that $V_{TH} = 25$mV.

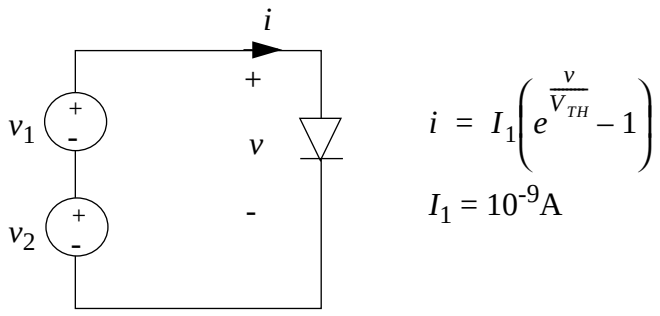


Figure 4.28:

a) Find the current i if only the v_1 source is connected (i.e., with the v_2 source shorted out).

b) Find the current i if only the v_2 source is connected.

c) Find the current i if both sources are connected as shown. Is superposition obeyed? Explain.

d) Based on your answer in c) discuss the dependence of the amplitude of the *sinusoidal component* of the current on the amplitude A_2. How big can A_2 be before significant generation of harmonics will occur?

HINT: Taylor's theorem is relevant to this problem.

Solution:

a) $i = 10^{-9}(\exp(\frac{0.5}{V_{TH}}) - 1)$

b) $i = 10^{-9}(\exp(\frac{0.001 \cos(\omega t)}{V_{TH}}) - 1)$

c) $i = 10^{-9}(\exp(\frac{0.5+0.001 \cos(\omega t)}{V_{TH}}) - 1)$

d) The dependence of the sinusoidal component of the current on the amplitude A_2 is nonlinear. However, for sufficiently small A_2 the relationship approximates a linear dependence. When $A_2 = 0.001$, harmonics make up approximately 2% of the sinusoidal component.

ANS:: (a) $i = 10^{-9}(\exp(\frac{0.5}{V_{TH}}) - 1)$ (b) $i = 10^{-9}(\exp(\frac{0.001\cos(\omega t)}{V_{TH}}) - 1)$ (c) $i = 10^{-9}(\exp(\frac{0.5+0.001\cos(\omega t)}{V_{TH}}) - 1)$ (d) $A_2 = 0.001$

Problem 4.11 This problem concerns the circuit illustrated in Figure 4.29:

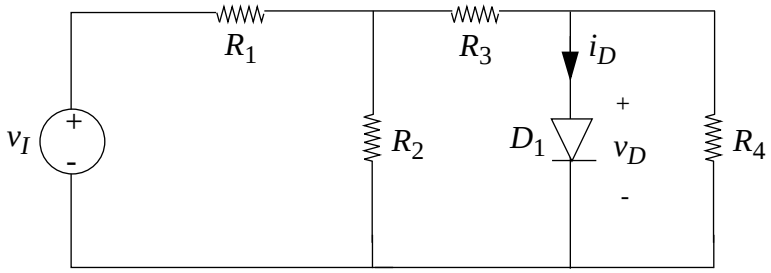


Figure 4.29:

$R_1 = 1.0k\Omega \quad R_2 = 1.0k\Omega \quad R_3 = 0.5k\Omega \quad R_4 = 1k\Omega$

For $D_1 : i_D = I_S(e^{v_D/V_{TH}} - 1)$ with $I_S = 1 \times 10^{-9}A$ and $V_{TH} = 25$mV.

a) Find the Thévenin equivalent circuit for the circuit connected to the diode.

b) Assume that for bias point determination the diode can be modeled by an ideal diode and a 0.6 volt battery. What are v_D and i_D when $v_1 = 4$ volts?

c) Find a linear equivalent model for this diode valid for small signal incremental operation about the bias point determined from part b.

d) Use your model of part c) to find $v_d(t)$ if $v_I = 4 + 0.004\ \cos\omega t$ volts.

Solution:

a) $R_{TH} = 0.5$ kΩ $V_{OC} = \frac{1}{4}v_I$

b) $v_D = 0.6$V, $i_D = 0.8$mA

c) $r_d = \frac{V_{TH}}{I_S}\exp(\frac{-V_D}{V_{TH}}) = 9.44 \times 10^{-4}\Omega$

d) $v_d = 7.55 \times 10^{-9}\ \cos\omega t$

ANS:: (a) $R_{TH} = 0.5k\Omega, V_{OC} = \frac{1}{4}v_I$ (b) $v_D = 0.6V, i_D = 0.8mA$ (c) $r_d = \frac{V_{TH}}{I_S}\exp(\frac{-V_D}{V_{TH}}) = 9.44 \times 10^{-4}\Omega$ (d) $v_d = 7.55 \times 10^{-9}\ \cos\omega t$

Problem 4.12 Consider the circuit in Figure 4.30. The voltage source and the current source are the sum of a dc-level and an ac-perturbation:

$$v = V + \Delta v$$
$$i = I + \Delta i$$

such that $V = 30V$ (dc), $I = 10A$ (dc), $\Delta v = 100mV$ (ac), $\Delta i = 50mA$ (ac).

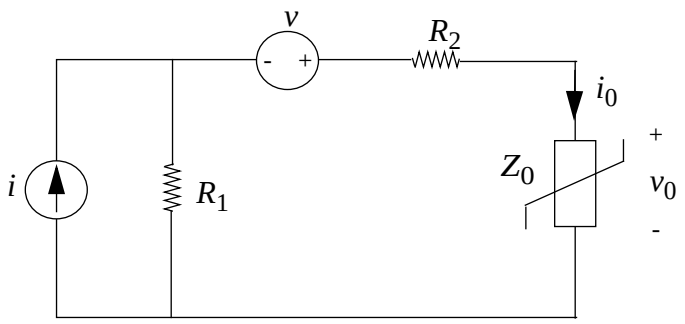


Figure 4.30:

The resistors have the following values: $R_1 = R_2 = 1/2$ ohm. The nonlinear element Z_0 has the characteristic:

$$i_0 = v_0 + v_0^2$$

Find, by incremental analysis, the DC and AC components of the output voltage v_0.

Remark: You can assume in your analysis that the nonlinear element is behaving as a passive element, i.e., is consuming power.

Solution: DC component: $5V$

AC component from current source: $0.002V$

AC component from voltage source: $0.008V$

ANS:: DC:$5V$, AC from current:$0.002V$, AC from voltage: $0.008V$

Problem 4.13 The circuit shown in Figure 4.31 contains a nonlinear element with the following properties:

$$\begin{aligned} i_N &= 10^{-4} v_N^2 \quad when \;\; v_N > 0 \\ i_N &= 0 \qquad\quad when \;\; v_N < 0 \end{aligned}$$

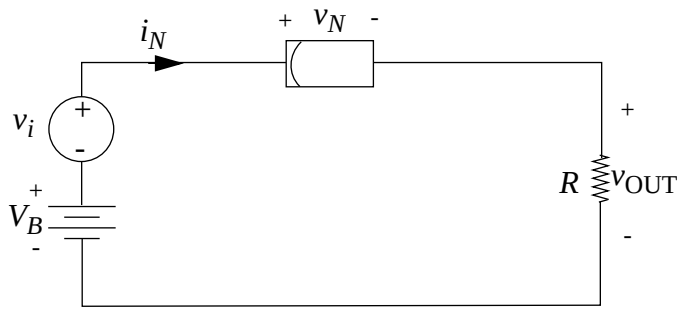


Figure 4.31:

where i_N is in amps, and v_N is in volts.

The output voltage, v_{OUT}, may be written approximately as the sum of the two terms:

$$v_{OUT} \simeq V_{OUT} + v_{out} \tag{4.3}$$

Where V_{OUT} is a dc voltage produced by V_B and v_{out} is the incremental voltage produced by the incremental voltage source v_i.

Assuming that $v_i = 10^{-3} sin\ \omega t$ volts and V_B is such that the nonlinear element operates with $V_N = 10$ volts, determine the incremental output voltage v_{out}.

Solution:

(note: must label resistor value)

$v_{out} = \frac{R}{R+500} 10^{-3} \sin(\omega t)$

ANS:: $v_{out} = \frac{R}{R+500} 10^{-3} \sin(\omega t)$

Problem 4.14 Consider the diode network shown below.

For purposes of this problem, the $i_D - v_D$ characteristics of all of the diodes can be accurately represented as

$$i_D = I_S e^{(v_D/25mV)} \quad \text{where} \quad I_S = 1mA/e^{25}$$

Do not use a piecewise-linear model.

a) First assume that $\Delta i = 0$. (Thus $\Delta v_i = \Delta v_2 = 0$). What are the operating-point values of voltages V_1 and V_2?

b) Now assume that Δi is non zero, but small enough so that incremental analysis can be used to determine Δv_1 and Δv_2. What is the ratio $\Delta v_1 / \Delta v_2$?

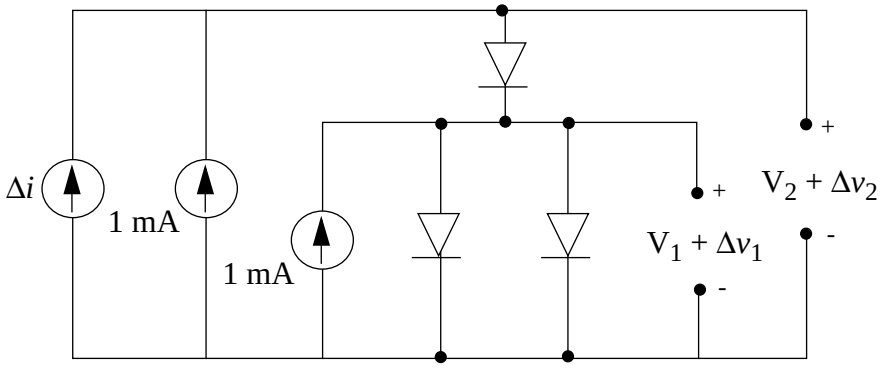


Figure 4.32:

Solution:

a) $V_1 = 625mV$; $V_2 = 1.25V$

b) $\frac{1}{3}$

ANS:: (a) $V_1 = 625mV; V_2 = 1.25V$, (b) $\frac{1}{3}$.

Chapter 5

The Digital Abstraction

Exercises

Exercise 5.1 Write a Boolean expression for the following statement: "Z is TRUE if either X or Y is FALSE, otherwise Z is FALSE". Write a truth table for this expression.

Solution:

$$Z = \overline{X} + \overline{Y}$$

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

ANS:: $Z = \overline{X} + \overline{Y}$

Exercise 5.2 Write a Boolean expression for the following statement: "Z is FALSE if either X or Y is FALSE, otherwise Z is TRUE". Write a truth table for this expression.

Solution:

$$\overline{Z} = \overline{X} + \overline{Y}$$
$$Z = \overline{\overline{X} + \overline{Y}} = XY$$

ANS:: $Z = XY$

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

Exercise 5.3 Write a Boolean expression for the following statement: "Z is TRUE if no more than two of W, X, and Y are TRUE, otherwise Z is FALSE".

Solution:

In this case, "no more than 2" = "not all 3", so:

$$Z = \overline{WXY}$$

ANS:: $Z = \overline{WXY}$

Exercise 5.4 Consider the statement: "Z is TRUE if at least two of W, X, and Y are TRUE, otherwise Z is FALSE".

a) Write a Boolean expression for the above statement.

b) Write a truth table for the function Z.

c) Implement Z using only AND, OR, and NOT gates. The inputs W, X, and Y are available. Each gate may have an arbitrary number of inputs. (Hint: A sum-of-products representation of the Boolean expression will facilitate this implementation.)

d) Implement Z using only AND, OR, and NOT gates. Each gate may have no more than two inputs. As before, the inputs W, X, and Y are available.

e) Implement Z using only NAND and NOR gates. (Hint: a NAND gate or a NOR gate with its inputs tied together behaves like an inverter).

f) Implement Z using only NAND gates. (Hint: Use De Morgan's laws.)

g) Implement Z using only NOR gates. (Hint: Use De Morgan's laws.)

h) Repeat part (d) and attempt to minimize the number of gates used.

i) Repeat part (d) and attempt to minimize the number of gates used, assuming that the inputs are available both in their true and complement forms. In other words, assume that in addition to W, X, and Y, the inputs $\overline{W}$, $\overline{X}$, and $\overline{Y}$, are also available.

Solution:

a)

$$Z = WX + WY + XY + WXY$$

W	X	Y	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

b)

c) See Figure 5.1 for logic diagram.

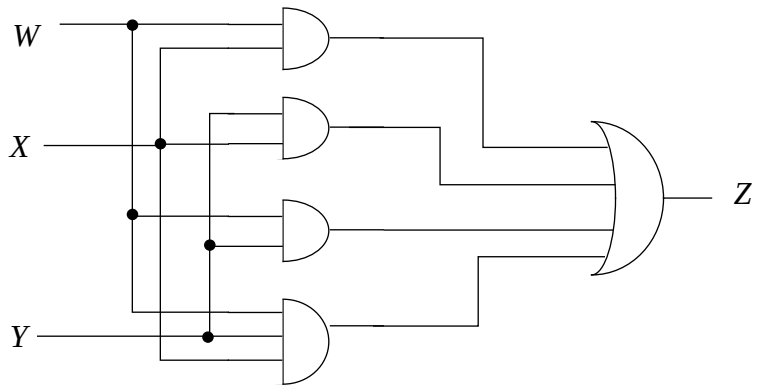


Figure 5.1:

d) See Figure 5.2 for logic diagram.

e) See Figure 5.3 for logic diagram.

f) Only NAND:

$$Z = \overline{(\overline{WX})(\overline{WY})(\overline{XY})(\overline{WXY})}$$

See Figure 5.4 for logic diagram.

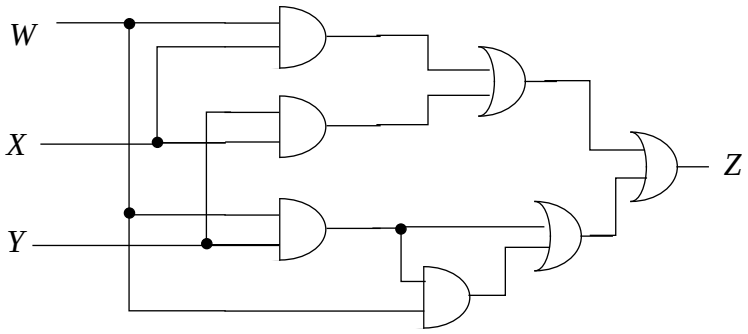


Figure 5.2:

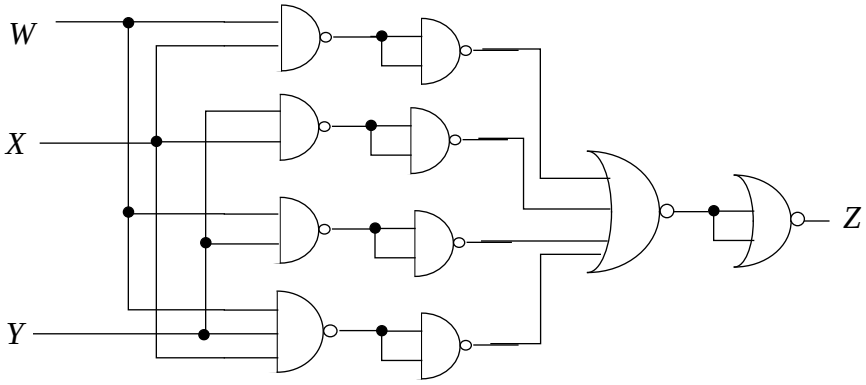


Figure 5.3:

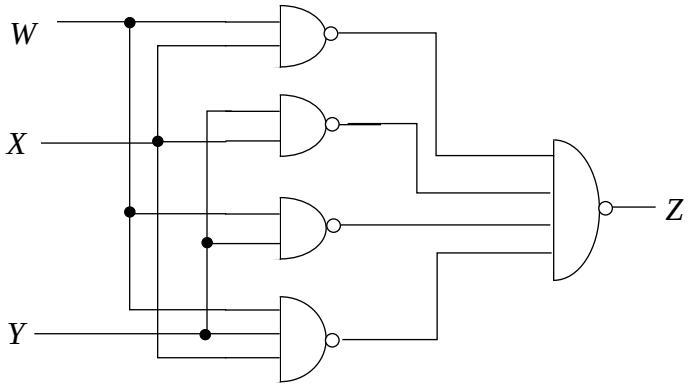


Figure 5.4:

g) Only NOR:

$$Z = \overline{\overline{(\overline{W} + \overline{X})} + \overline{(\overline{W} + \overline{Y})} + \overline{(\overline{Y} + \overline{X})} + \overline{(\overline{W} + \overline{X} + \overline{Y})}}$$

See Figure 5.5 for logic diagram.

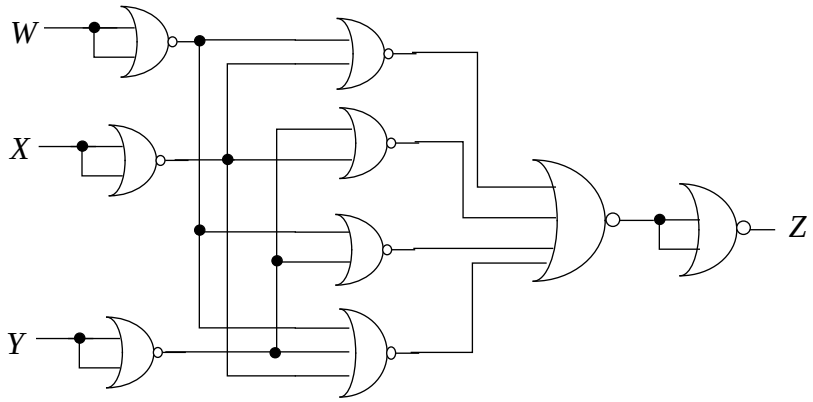


Figure 5.5:

h)

$$\begin{aligned} Z &= WX + WY + XY + WXY \\ &= WX(1+Y) + WY + XY \\ &= WX + WY + XY \\ Z &= W(X+Y) + XY \end{aligned}$$

See Figure 5.6 for logic diagram.

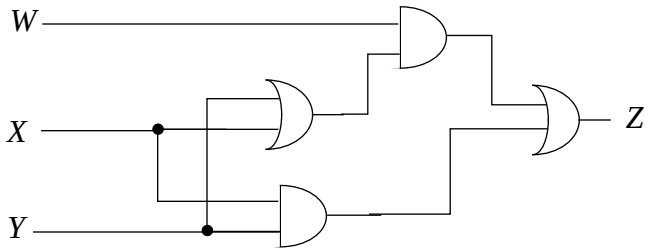


Figure 5.6:

i) Solution: same as (h)

ANS:: (a) $Z = WX + WY + XY + WXY$

Exercise 5.5 Represent the decimal number 4 as an unsigned, three-bit binary number and as an unsigned, four-bit binary number. Unsigned numbers do not include a sign bit. For example, 11110 is the unsigned, binary representation of the decimal number 30.

Solution:

Unsigned 3-bit: 100

Unsigned 4-bit: 0100

ANS:: 100, 0100

Exercise 5.6 Consider the functions $F(A, B, C)$ and $G(A, B, C)$ specified in the truth table given in Table 5.1.

A	B	C	$F(A, B, C)$	$G(A, B, C)$
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

Table 5.1: Truth table for Exercise 5.6

a) Write a logic expression corresponding to the functions $F(A, B, C)$ and $G(A, B, C)$.

b) Implement $F(A, B, C)$ with logic gates.

c) Implement $F(A, B, C)$ using only 2-input gates.

d) Implement $F(A, B, C)$ using only 2-input NAND gates. Hint: Use De Morgan's laws.

e) Repeat parts b) through d) for the function $G(A, B, C)$.

Solution:

a)

$$F = \overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot C + A \cdot B \cdot C$$

If we simplify F, combining the first pair and the second pair,

$$F = \overline{B} \cdot \overline{C} + A \cdot C$$

and

$$G = \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + A \cdot B \cdot C$$

We can combine the first and last terms,

$$G = A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + B \cdot C$$

b) See Figure 5.7 for logic diagram.

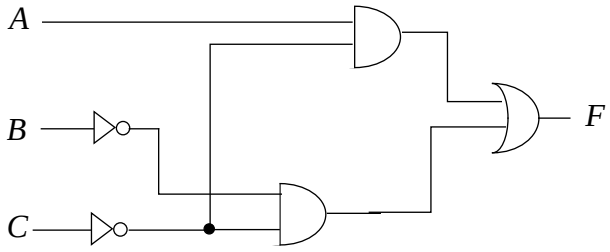


Figure 5.7:

c) Same as part (b)

d) Using our simplified version of F, De Morgan's laws, and the fact that a NAND gate with logical signal X tied into both inputs produces $\overline{X}$,

$$F = \overline{\overline{(\overline{B} \cdot \overline{C})} \cdot \overline{(A \cdot C)}}$$

See Figure 5.8

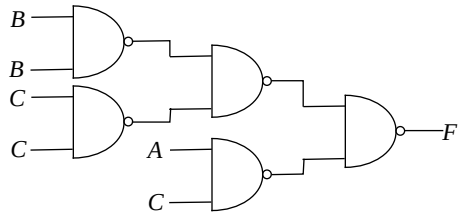


Figure 5.8:

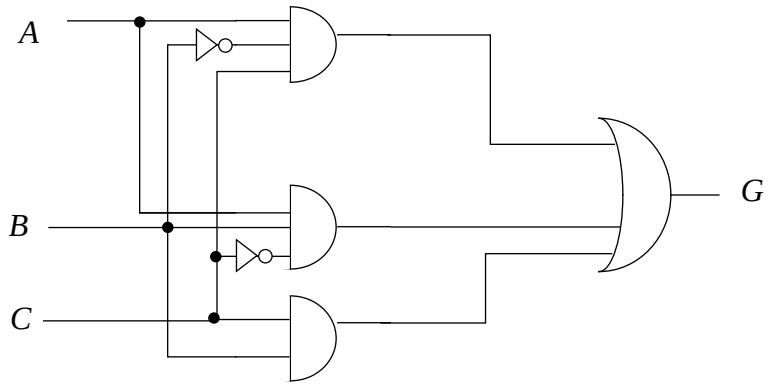


Figure 5.9:

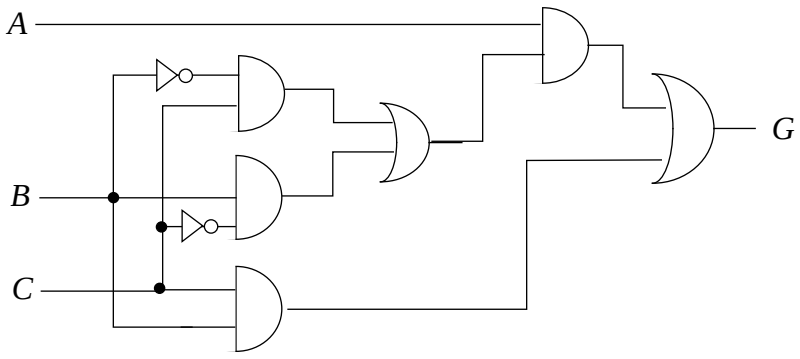


Figure 5.10:

e) Implement $G(A, B, C)$ with logic gates. See Figure 5.9

Implement $G(A, B, C)$ using only 2-input gates. See Figure 5.10

Implement $G(A, B, C)$ using only 2-input NAND gates.

$$G = \overline{\overline{(\overline{BC})}\,\overline{(A(\overline{\overline{(\overline{BC})}}\,(\overline{BC})))}}$$

See Figure 5.11

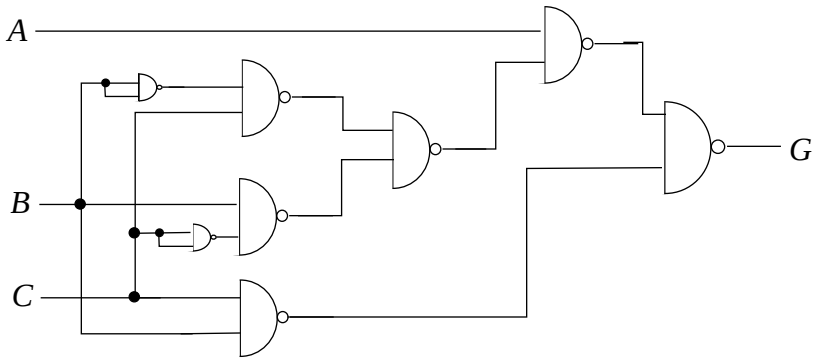


Figure 5.11:

ANS:: (a) $F = \overline{B} \cdot \overline{C} + A \cdot C$, $A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + B \cdot C$

Exercise 5.7 Consider the four logic expressions below.

1. $(A + \overline{B})(\overline{A} \cdot \overline{B} + C) + \overline{C \cdot D}$
2. $(A \cdot \overline{C} + \overline{B \cdot D})(\overline{D + \overline{B} + A})$
3. $A + \overline{\overline{B} \cdot D} + A \cdot C \cdot \overline{D}$
4. $\overline{(\overline{(A + \overline{C})} + B + \overline{D}) + A \cdot \overline{C} \cdot D}$

a) Give an implementation using gates for each of the logic expressions above.

b) Write the truth table for each of the four expressions.

c) Suppose you know that $A = 0$. Simplify the four expressions under this constraint.

d) Simplify the four expressions assuming that A and B are related as $A = \overline{B}$.

Solution:

a) 1. A simplification of the expression would be

$$F = \overline{(\overline{A} \cdot B \cdot C \cdot D)}$$

See Figure 5.12(1)

2. Using De Morgan's laws, the fact that X $\cdot$ $\overline{X}$ = 0, the fact that X $\cdot$ X = X, and the distributive law,

$$F = (A \cdot \overline{C} + \overline{B} + \overline{D})(\overline{D} \cdot B \cdot \overline{A})$$

$$F = \overline{D} \cdot B \cdot \overline{A}$$

See Figure 5.12(2)

3. Using the fact that X + X $\cdot$ Y = X and De Morgan's,

$$F = A + B + \overline{D}$$

See Figure 5.12(3)

4. Using the fact that $\overline{X}$ + X $\cdot$ Y = $\overline{X}$ + Y and De Morgan's,

$$F = \overline{\overline{A} \cdot C + B + \overline{D} + A \cdot \overline{C}}$$

See Figure 5.12(4)

b) See Table 5.2

•

c) 1) $\overline{BCD}$

2) $B\overline{D}$

3) $B + \overline{D}$

4) $\overline{B}\,\overline{C}D$

d)

1) $\overline{BCD}$

2) 0

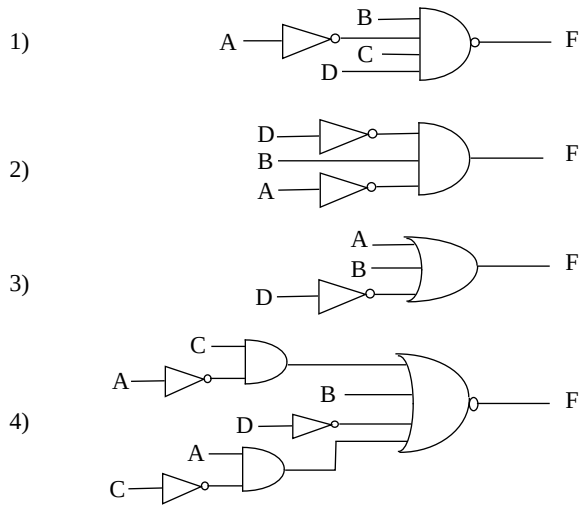


Figure 5.12:

Table 5.2:

A	B	C	D	F_1	F_2	F_3	F_4
0	0	0	0	1	0	1	0
0	0	0	1	1	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	1	0	0	0
0	1	0	0	1	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	0
1	1	1	1	1	0	1	0

3) 1

4) $\overline{B}CD$

ANS:: (c) $\overline{BCD}$, $B\overline{D}$, $B + \overline{D}$, $\overline{B}\ \overline{C}D$ (d) $\overline{BCD}$, 0, 1, $\overline{B}CD$

Exercise 5.8 A logic gate obeys a static discipline with the following voltage levels: $V_{IH} = 3.5V$, $V_{OH} = 4.3V$, $V_{IL} = 1.5V$ and $V_{OL} = 0.9V$. (a) What range of voltages will be treated as invalid under this discipline? (b) What are its noise margins?

Solution:

(a)

Devices must produce output voltages within the following ranges:

Valid range for low outputs:

$$V_{OL} \leq v \Rightarrow 0.9 \leq v$$

Valid range for high outputs:

$$V_{OH} \geq v \Rightarrow 4.3 \geq v$$

Devices must interpret correctly input voltages within the following ranges:

Valid range for low inputs:

$$V_{IL} \leq v \Rightarrow 1.5 \leq v$$

Valid range for high inputs:

$$V_{IH} \geq v \Rightarrow 3.5 \geq v$$

(b)

$$NM_0 = V_{IL} - V_{OL} = 1.5 - 0.9 = 0.6$$

$$NM_1 = V_{OH} - V_{IH} = 4.3 - 3.5 = 0.8$$

ANS:: (a) "0" outputs: $0.9 \leq v$, "1" outputs: $4.3 \geq v$, "0" inputs: $1.5 \leq v$, "1" inputs: $3.5 \geq v$, (b) $NM_0 = 0.6$ and $NM_1 = 0.8$

Exercise 5.9 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{IL} = 1.5$ V, $V_{OL} = 0.5$ V, $V_{IH} = 3.5$ V, and $V_{OH} = 4.4$ V.

a) Graph an input-output voltage transfer function of a buffer satisfying the voltage thresholds given above.

b) Graph an input-output voltage transfer function of an inverter satisfying the voltage thresholds given above.

c) What is the highest voltage that can be output by an inverter for a logical 0 output?

d) What is the lowest voltage that can be output by an inverter for a logical 1 output?

e) What is the highest voltage that must be interpreted by a receiver as a logical 0?

f) What is the lowest voltage that must be interpreted by a receiver as a logical 1?

g) Does this choice of voltage thresholds offer any immunity to noise? If so, determine the noise margins.

Solution:

a) See Figure 5.13

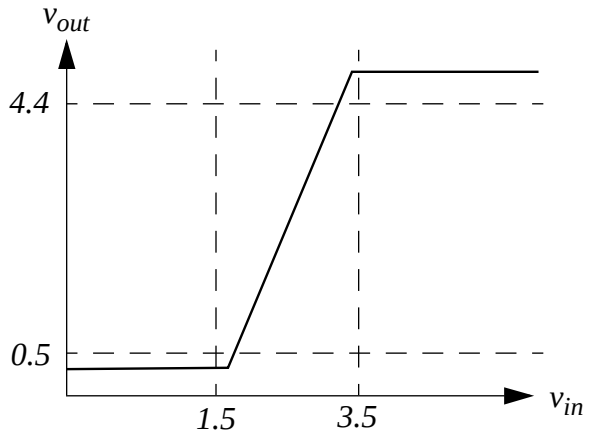


Figure 5.13:

b) See Figure 5.14

c) $V_{OL} = 0.5V$

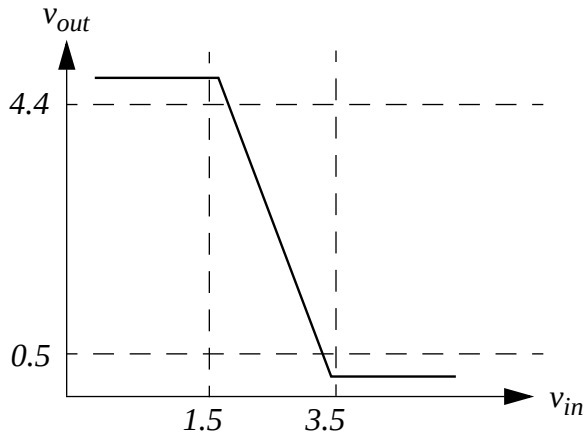


Figure 5.14:

d) $V_{OH} = 4.4V$

e) $V_{IL} = 1.5V$

f) $V_{IH} = 3.5V$

g) Yes. The noise margins are given by:

$$NM_0 = V_{IL} - V_{OL} = 1.5 - 0.5 = 1V$$

$$NM_1 = V_{OH} - V_{IH} = 4.4 - 3.5 = 0.9V$$

ANS:: (c) 0.5V (d) 4.4V (e) 1.5V (f) 3.5V (g) Yes. $NM_0 = 1V$ and $NM_1 = 0.9V$

Exercise 5.10 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{IL} = V_{OL} = 0.5$ V and $V_{IH} = V_{OH} = 4.4$ V.

a) Graph an input-output voltage transfer function of a buffer satisfying the voltage thresholds given above.

b) Graph an input-output voltage transfer function of an inverter satisfying the voltage thresholds given above.

c) What is the highest voltage that can be output by an inverter for a logical 0 output?

d) What is the lowest voltage that can be output by an inverter for a logical 1 output?

e) What is the highest voltage that must be interpreted by a receiver as a logical 0?

f) What is the lowest voltage that must be interpreted by a receiver as a logical 1?

g) Does this choice of voltage thresholds offer any immunity to noise?

Solution:

a) See Figure 5.15

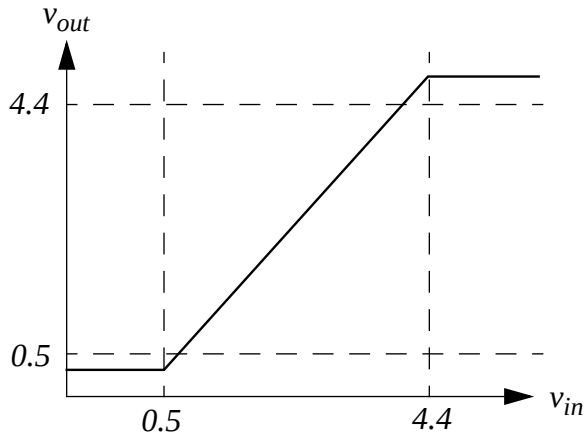


Figure 5.15:

b) See Figure 5.16

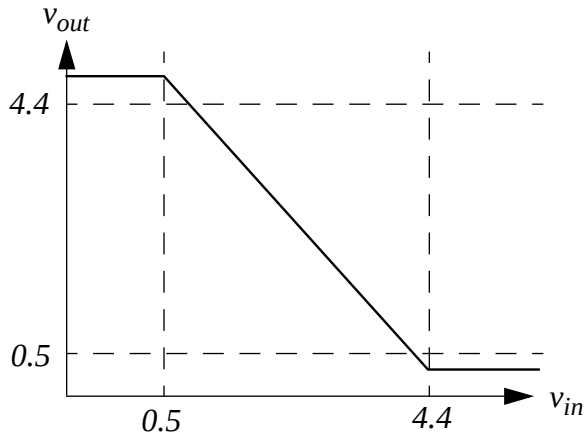


Figure 5.16:

c) $V_{OL} = 0.5V$

d) $V_{OH} = 4.4V$

e) $V_{IL} = 0.5V$

f) $V_{IH} = 4.4V$

g) No.

ANS:: (c) 0.5V (d) 4.4V (e) 0.5V (f) 4.4V (g) No

Problems

Problem 5.1 Derive a truth table and a Boolean expression that describes the operation of each digital circuit shown in Figure 5.17.

Solution:

For truth tables, see Table 5.1 (parts a-b), and Table 5.1 (parts c-f).

A	B	C	D	Z_a	Z_b
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	0

a) $\overline{\overline{AB} \cdot \overline{CD}} = \overline{\overline{AB}} + \overline{\overline{CD}} = AB + CD$

b) $\overline{\overline{A\overline{B}} \cdot \overline{\overline{C}D}} = \overline{\overline{A\overline{B}}} + \overline{\overline{\overline{C}D}} = A\overline{B} + \overline{C}D$

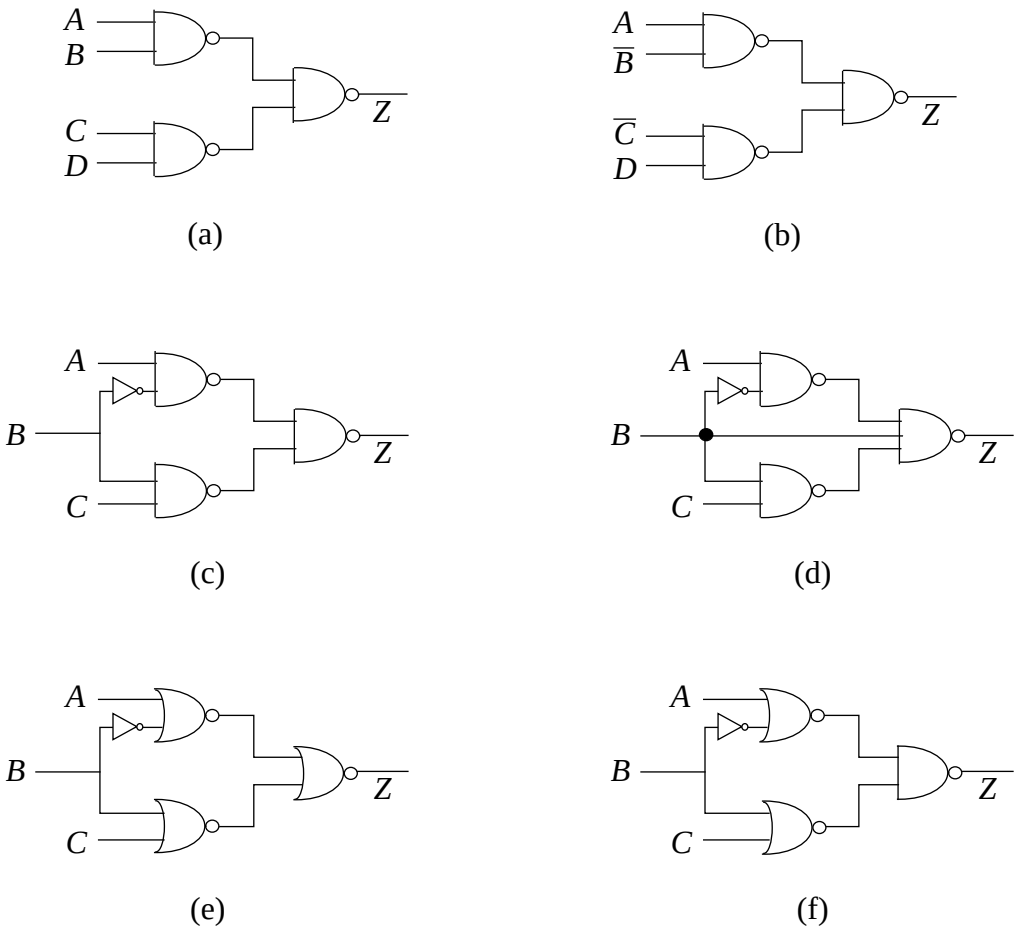


Figure 5.17:

A	B	C	Z_c	Z_d	Z_e	Z_f
0	0	0	0	1	0	0
0	0	1	0	1	1	1
0	1	0	0	0	0	0
0	1	1	1	1	0	1
1	0	0	1	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	1	1	1	1	1

c) $\overline{\overline{A\overline{B}} \cdot \overline{BC}} = A\overline{B} + BC$

d) $\overline{\overline{A\overline{B}} \cdot B \cdot \overline{BC}} = A\overline{B} + \overline{B} + BC = \overline{B} + C$

e) $\overline{\overline{A + \overline{B}} + \overline{B + C}} = (A+\overline{B}) \cdot (B+C) = AB + AC + \overline{B}B + \overline{B}C = AB + AC + \overline{B}C$

f) $\overline{\overline{A + \overline{B}} \cdot \overline{B + C}} = 1$

ANS:: (a) $AB + CD$ (b) $A\overline{B} + \overline{C}D$ (c) $A\overline{B} + BC$ (d) $\overline{B} + C$ (e) $AB + AC + \overline{B}C$ (f) 1

Problem 5.2 Draw an output voltage waveform for the circuit in Figure 5.17c in response to the input voltage waveforms shown in Figure 5.18. Assume that the gates in the circuit obey the static discipline with $V_{\mathrm{OH}} = 4$V, $V_{\mathrm{IH}} = 3$V, $V_{\mathrm{OL}} = 1$V, and $V_{\mathrm{IL}} = 2$V.

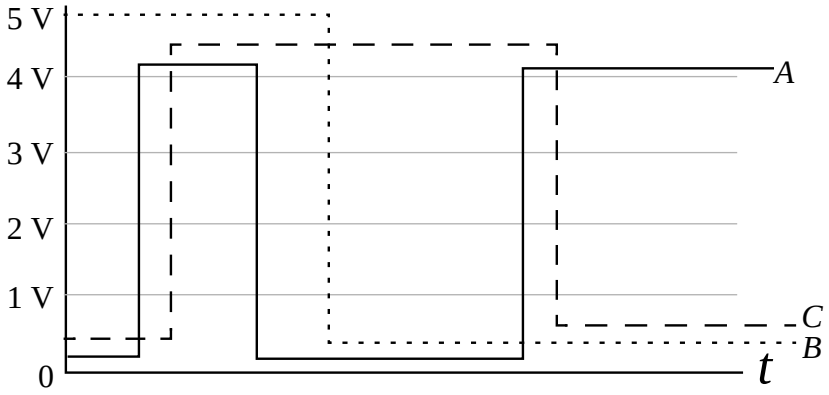


Figure 5.18:

Solution:

For Circuit 5.17c, the output is given by

$$Z = A\overline{B} + BC$$

There are 7 different states, where a state transition occurs when one of the three inputs changes by itself. For example, the first state is when A and C are low and B is high, the second state is when A and B are high, and C is low, and so on. The output in the first, second and fifth states is low (below 1V), while the output in the remaining states is high (above 4V).

Problem 5.3 The truth table for a "ones count" circuit is given in Table 5.3. This circuit has four inputs: A, B, C, and D, and three outputs OUT_0, OUT_1, and OUT_2. Together, the signals OUT_0, OUT_1, and OUT_2 represent a 3-bit positive integer $OUT_2OUT_1OUT_0$. The output integer $OUT_2OUT_1OUT_0$ reflects the number of ones in the input. Using only NAND, NOR and NOT gates, design an implementation for the circuit. Each gate may have an arbitrary number of inputs.

A	B	C	D	OUT_2	OUT_1	OUT_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	0	1	0
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	1	0	0

Table 5.3:

Solution:

See Figure 5.19 for logic diagram.

Using sum-of-products,

$OUT_2 = ABCD$

$OUT_1 = \overline{A} \cdot \overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + \overline{A}BCD + A\overline{B} \cdot \overline{C}D + A\overline{B}C\overline{D} + A\overline{B}CD + AB\overline{C} \cdot \overline{D} + AB\overline{C}D + ABC\overline{D} = \overline{A}CD + B\overline{C}D + BC\overline{D} + A\overline{B}C + A\overline{B} \cdot \overline{C}D + AB\overline{C} \cdot \overline{D}$

$OUT_0 = \overline{A} \cdot \overline{B} \cdot \overline{C}D + \overline{A} \cdot \overline{B}C\overline{D} + \overline{A}B\overline{C} \cdot \overline{D} + \overline{A}BCD + A\overline{B} \cdot \overline{C} \cdot \overline{D} + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$

ANS:: $OUT_2 = ABCD$, $OUT_1 = \overline{A}CD + B\overline{C}D + BC\overline{D} + A\overline{B}C + A\overline{B} \cdot \overline{C}D + AB\overline{C} \cdot \overline{D}$, $OUT_0 = \overline{A} \cdot \overline{B} \cdot \overline{C}D + \overline{A} \cdot \overline{B}C\overline{D} + \overline{A}B\overline{C} \cdot \overline{D} + \overline{A}BCD + A\overline{B} \cdot \overline{C} \cdot \overline{D} + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$

Problem 5.4 A four-input multiplexer module is shown in Figure 5.20. The multiplexer

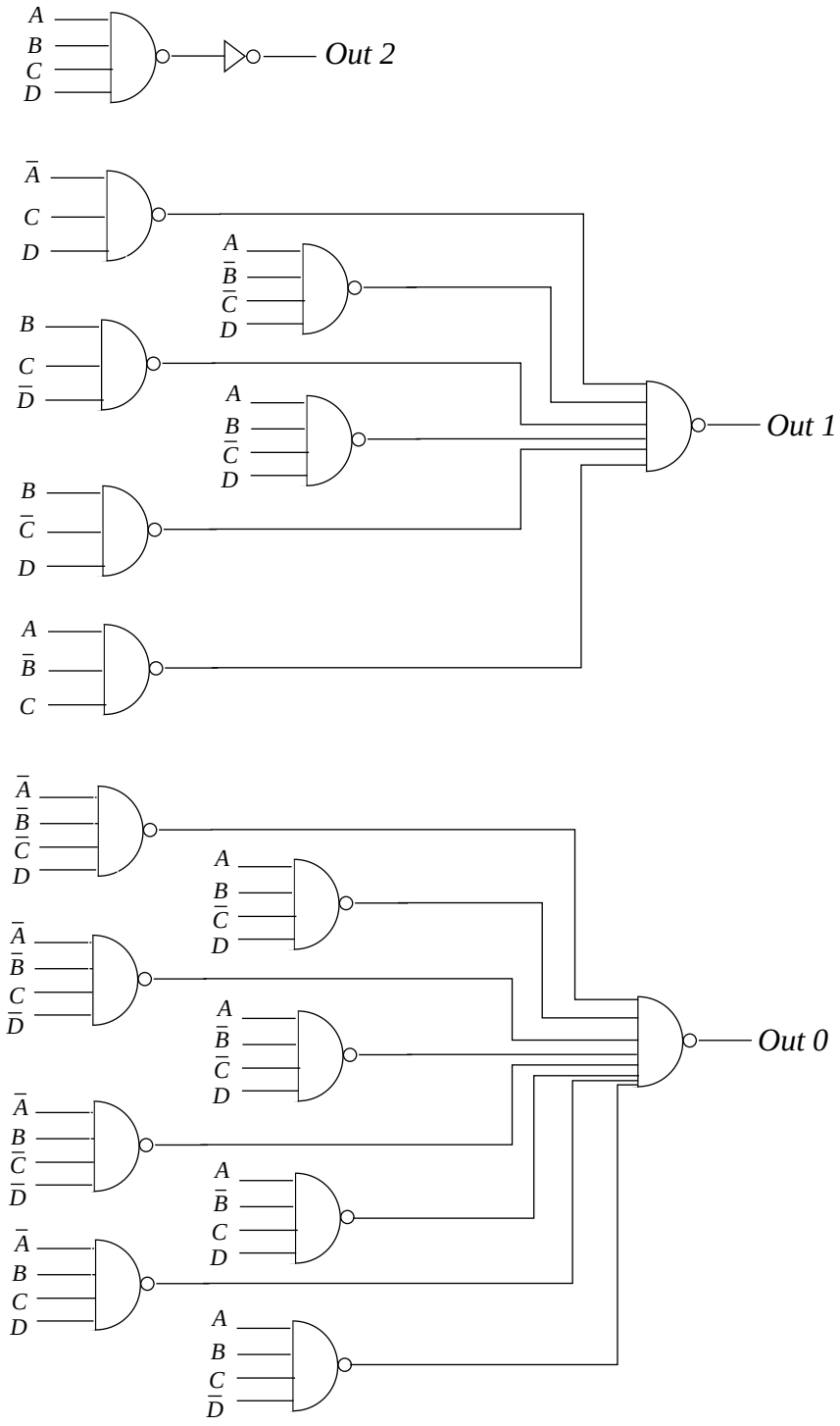

A
B
C
D
Out 2
$\overline{A}$
C
D
A
$\overline{B}$
$\overline{C}$
D
B
C
$\overline{D}$
A
B
$\overline{C}$
D
Out 1
B
$\overline{C}$
D
A
$\overline{B}$
C
$\overline{A}$
$\overline{B}$
$\overline{C}$
D
A
B
$\overline{C}$
D
$\overline{A}$
$\overline{B}$
C
$\overline{D}$
A
B
$\overline{C}$
D
Out 0
$\overline{A}$
B
$\overline{C}$
$\overline{D}$
A
$\overline{B}$
C
D
$\overline{A}$
B
C
D
A
B
C
$\overline{D}$

Figure 5.19:

has two select signals S_1 and S_0. The value on the select signals determines which of the inputs A, B, C, and D appears at the output. As illustrated in the figure, A is selected if S_1S_0 is 00, B if S_1S_0 is 01, C if S_1S_0 is 10, and D if S_1S_0 is 11. Write a boolean expression for Z in terms of S_1S_0, A, B, C, and D. Implement the multiplexer using only NAND gates.

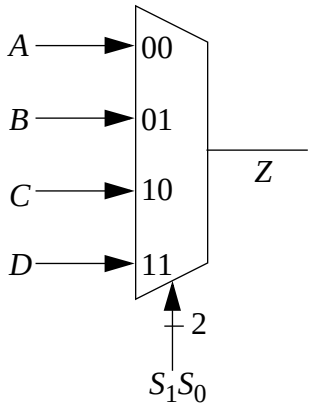


Figure 5.20: A four-input multiplexer module. The "2" beside the wire corresponding to the select signals is a short-hand notation indicating there are two wires present.

Solution:

Boolean expression:

$$Z = A\overline{S_1} \cdot \overline{S_0} + B\overline{S_1}S_0 + CS_1\overline{S_0} + DS_1S_0$$

See Figure 5.21 for logic diagram.

ANS:: $Z = A\overline{S_1} \cdot \overline{S_0} + B\overline{S_1}S_0 + CS_1\overline{S_0} + DS_1S_0$

Problem 5.5 A four-input demultiplexer module is shown in Figure 5.22. The demultiplexer has two select signals S_1 and S_0. The select signals determines on which of the outputs (OUT0, OUT1, OUT2, or OUT3) the input IN appears. As illustrated in the figure, IN appears at output OUT0 if S_1S_0 is 00, at OUT1 if S_1S_0 is 01, at OUT2 if S_1S_0 is 10, and at OUT3 if S_1S_0 is 11. An output is 0 if it is not selected. Write a boolean expression for each of the outputs in terms of S_1S_0 and IN. Implement the demultiplexer using only NAND gates.

Solution:

See Figure 5.23 for logic diagrams.

Boolean expressions:

$$OUT0 = IN \cdot \overline{S_1} \cdot \overline{S_2}$$

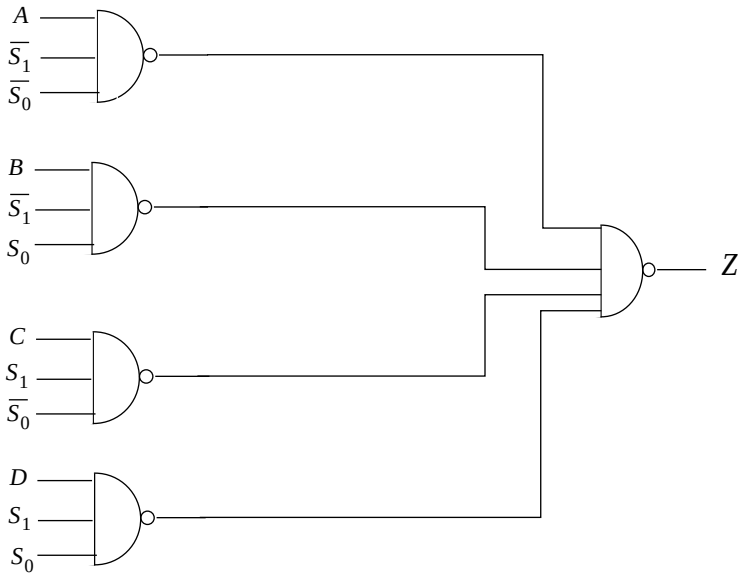


Figure 5.21:

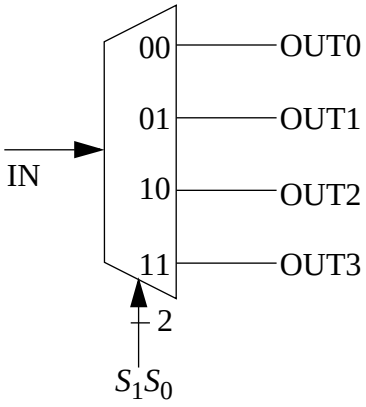


Figure 5.22:

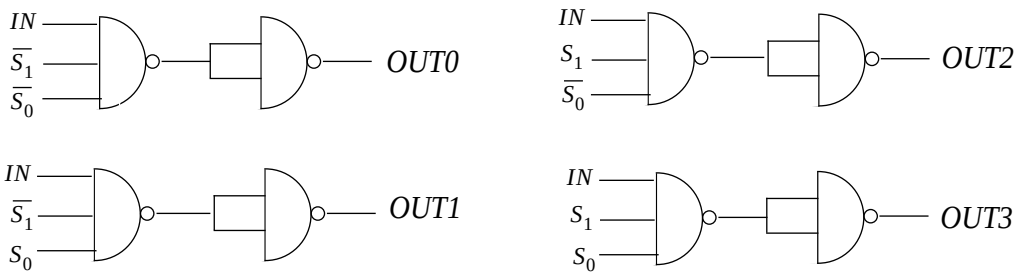


Figure 5.23:

$$OUT1 = IN \cdot \overline{S_1} \cdot S_0$$

$$OUT2 = IN \cdot S_1 \cdot \overline{S_0}$$

$$OUT3 = IN \cdot S_1 \cdot S0$$

ANS:: $OUT0 = IN \cdot \overline{S_1} \cdot \overline{S_2}$, $OUT1 = IN \cdot \overline{S_1} \cdot S_0$, $OUT2 = IN \cdot S_1 \cdot \overline{S_0}$, $OUT3 = IN \cdot S_1 \cdot S0$

Problem 5.6 Implement the "greater-than" circuit depicted in Figure 5.24 using NAND gates. A and B represent one-bit positive integers. The output Z is 1 if A is greater than B, otherwise Z is 0.

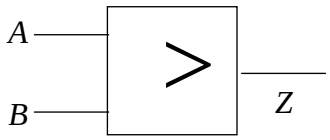


Figure 5.24:

Solution:

Z is 1 only if A is 1 and B is 0. The resulting expression is then:

$$Z = A\overline{B}$$

See Figure 5.25 for logic diagram.

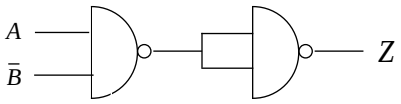


Figure 5.25:

ANS:: $Z = A\overline{B}$

Problem 5.7 Implement the 4-input "odd" or "odd parity" circuit depicted in Figure 5.26 using NOR gates. In this circuit, the output Z is high if an odd number of the inputs are high, otherwise the output Z is low. How would you use the 4-input "odd" circuit module shown in Figure 5.26 to implement a 3-input "odd" circuit. If this cannot be done, discuss why not.

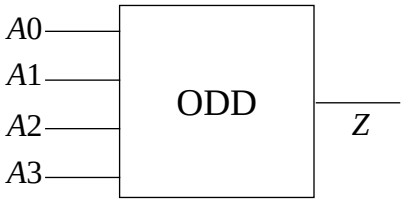


Figure 5.26:

$A1$	$A2$	$A3$	$A4$	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Solution:

Boolean expression:

$Z = \overline{A3} \cdot \overline{A2} \cdot \overline{A1} \cdot A0 + \overline{A3} \cdot \overline{A2} \cdot A1 \cdot \overline{A0} + \overline{A3} \cdot A2 \cdot \overline{A1} \cdot \overline{A0} + \overline{A3} \cdot A2 \cdot A1 \cdot A0 + A3 \cdot \overline{A2} \cdot \overline{A1} \cdot \overline{A0} + A3 \cdot \overline{A2} \cdot A1 \cdot A0 + A3 \cdot A2 \cdot \overline{A1} \cdot A0 + A3 \cdot A2 \cdot A1 \cdot \overline{A0}$

This circuit can be implemented in the same way as the previous problems, using sum of products and NAND gates. This same circuit module can be used to implement a 3-input "odd" circuit by tying one of the A inputs to ground. Incidentally, you could also make a 3-input "even" circuit by tying one of the A inputs to hi.

ANS:: $Z = \overline{A3} \cdot \overline{A2} \cdot \overline{A1} \cdot A0 + \overline{A3} \cdot \overline{A2} \cdot A1 \cdot \overline{A0} + \overline{A3} \cdot A2 \cdot \overline{A1} \cdot \overline{A0} + \overline{A3} \cdot A2 \cdot A1 \cdot A0 + A3 \cdot \overline{A2} \cdot \overline{A1} \cdot \overline{A0} + A3 \cdot \overline{A2} \cdot A1 \cdot A0 + A3 \cdot A2 \cdot \overline{A1} \cdot A0 + A3 \cdot A2 \cdot A1 \cdot \overline{A0}$

Problem 5.8 Figure 5.27 depicts a 4-input majority circuit module. The output Z of this circuit module is high if a majority of the inputs are high. Write a boolean expression for Z in terms of A0, A1, A2, and A3. How would you use the 4-input majority circuit module shown in Figure 5.27 to implement a 3-input majority circuit and a 2-input majority circuit. If either of these cannot be done, discuss why not.

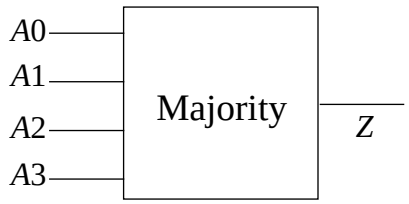


Figure 5.27:

Solution:

Boolean expression:

$Z = A0 \cdot A1 \cdot A2 \cdot \overline{A3} + A0 \cdot A1 \cdot \overline{A2} \cdot A3 + A0 \cdot \overline{A1} \cdot A2 \cdot A3 + A1 \cdot A2 \cdot A3$

Use NAND gates and sum-of-products to implement the Boolean expression. A 3-input majority circuit can be implemented by tying one input to HI. A 2-input majority circuit can be implemented by tying one input to ground and another input to HI.

ANS:: $Z = A0 \cdot A1 \cdot A2 \cdot \overline{A3} + A0 \cdot A1 \cdot \overline{A2} \cdot A3 + A0 \cdot \overline{A1} \cdot A2 \cdot A3 + A1 \cdot A2 \cdot A3$

Problem 5.9 Figure 5.28 illustrates a two-bit grey code converter. Its outputs OUT0, OUT1, are equal to the inputs when the IN0, IN1 are 00 or 01. However, when the inputs IN0, IN1 are 10 and 11 the outputs OUT0, OUT1 are 11 and 10 respectively. Implement the grey code converter using 2-input NAND gates.

$A1$	$A2$	$A3$	$A4$	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

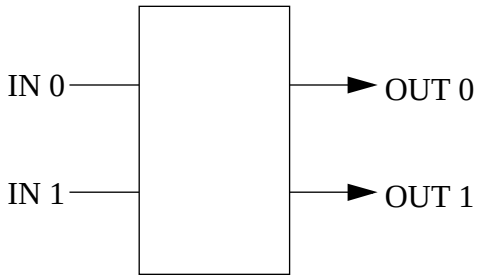


Figure 5.28:

$IN0$	$IN1$	$OUT0$	$OUT1$
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Solution:

Boolean expressions:

$$OUT0 = IN0$$

$$OUT1 = \overline{IN0}IN1 + IN0\overline{IN1}$$

ANS:: $OUT0 = IN0, OUT1 = \overline{IN0}\ IN1 + IN0\ \overline{IN1}$

Problem 5.10 Figure 5.29 illustrates input-output voltage transfer functions for several one-input one-output devices. For the voltage thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} as shown, which of the devices can serve as valid inverters?

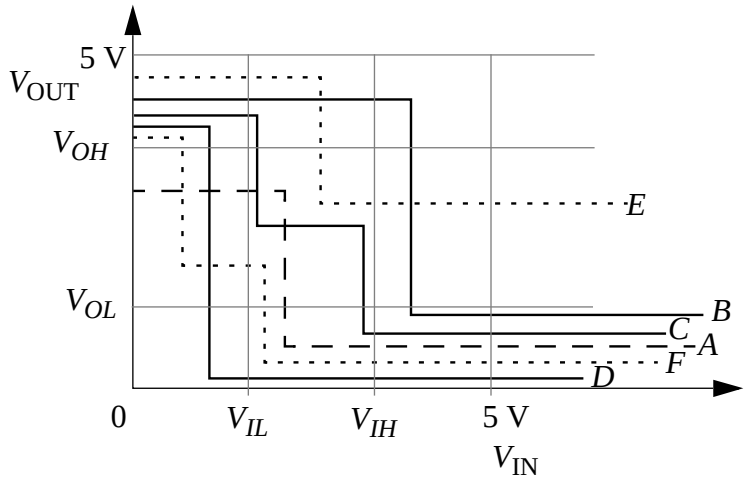


Figure 5.29:

Solution:

Only C is valid according to the static discipline.

Problem 5.11 Suppose we wish to build a two-bit adder circuit (Figure 5.30) that takes as input a pair of two-bit positive integers A_1A_0 and B_1B_0 and produces a two-bit sum output S_1S_0 and a carry out bit C_1. Write a truth table and a boolean expression for the carry out bit in terms of the inputs.

Now, suppose we wish to build a two-bit adder circuit (Figure 5.31) that takes as input a pair of two-bit positive integers A_1A_0 and B_1B_0, and a carry-in bit C_0, and produces a two-bit sum output S_1S_0 and a carry out bit C_1. Write a truth table and a boolean expression for the carry out bit in terms of the inputs.

Solution:

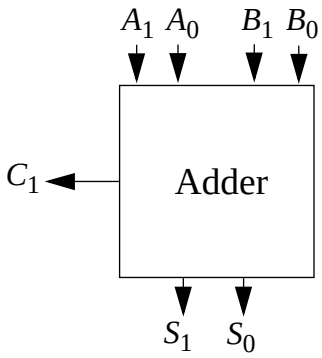


Figure 5.30:

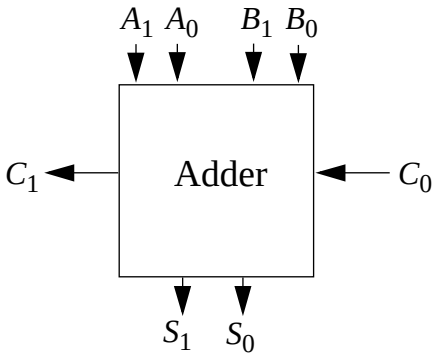


Figure 5.31:

A_1	A_0	B_1	B_0	C_1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

A_1	A_0	B_1	B_0	C_0	C_1
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

$$C_1 = \overline{A_1}A_0B_1B_0 + A_1A_0\overline{B_1}B_0 + A_1B_1$$

$$C_1 = \overline{A_1}A_0B_1B_0 + A_1A_0\overline{B_1}B_0 + A_1B_1 + B_1B_0C_0 + A_1A_0C_0 + A_1B_0C_0 + A_0B_1C_0$$

ANS:: $C_1 = \overline{A_1}A_0B_1B_0 + A_1A_0\overline{B_1}B_0 + A_1B_1 + B_1B_0C_0 + A_1A_0C_0 + A_1B_0C_0 + A_0B_1C_0$

Problem 5.12 Suppose we have two logic families named NTL and YTL. The NTL family of logic gates operates under the static discipline with the following voltage thresholds: $V_{IL} = 1.5$V, $V_{OL} = 1.0$V, $V_{IH} = 3.5$V, and $V_{OH} = 4$V. The YTL family, on the other hand, is characterized by the voltage thresholds: $V_{IL} = 0.8$V, $V_{OL} = 0.3$V, $V_{IH} = 3.0$V, and $V_{OH} = 4.5$V. Will a YTL inverter driving the input of an NTL inverter operate correctly? Explain. Will a NTL inverter driving the input of an YTL inverter operate correctly? Explain.

Solution:

A YTL inverter driving an NTL inverter will operate correctly because all valid outputs of the YTL are valid inputs for the NTL.

On the other hand, an NTL inverter driving a YTL inverter will not operate correctly since a valid low output of the NTL between 0.8V - 1V would fall into the forbidden region (0.8V - 3V) of the YTL.

Problem 5.13 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{\mathrm{OL}} = 0.5$ V, $V_{\mathrm{IL}} = 1.6$ V, $V_{\mathrm{OH}} = 4.4$ V and $V_{\mathrm{IH}} = 3.2$ V.

a) Graph an input-output voltage transfer function of a buffer satisfying the voltage thresholds given above.

b) Graph an input-output voltage transfer function of an inverter satisfying the voltage thresholds given above.

c) What is the highest voltage that can be output by an inverter for a logical 0 output?

d) What is the lowest voltage that can be output by an inverter for a logical 1 output?

e) What is the highest voltage that must be interpreted by a receiver as a logical 0?

f) What is the lowest voltage that must be interpreted by a receiver as a logical 1?

g) When transmitting information over a noisy wire, buffers can be used to minimize transmission errors by restoring signal values. Consider the transmission of data over a noisy wire which picks up a maximum of 80 mV symmetric peak-to-peak noise per centimeter. How many buffers are needed to transmit a signal over a distance of 2 meters in this noisy environment?

h) How large are the 0 and 1 noise margins for a buffer in this logic family? Now consider three buffers connected in series and behaving as a single buffer. What are the noise margins for this new buffer?

Solution:

a) Any input below V_{IL} must produce an output less than or equal to V_{OL} and any input above V_{IH} must produce an output greater than or equal to V_{OH}.

See Figure 5.32 for graph.

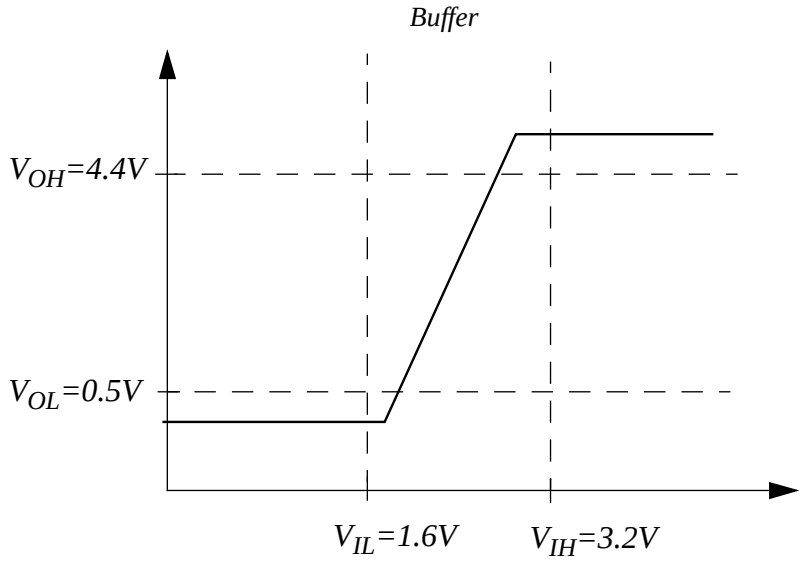


Figure 5.32:

b) See Figure 5.33 for graph.

c) $0.5V$

d) $4.4V$

e) $1.6V$

f) $3.2V$

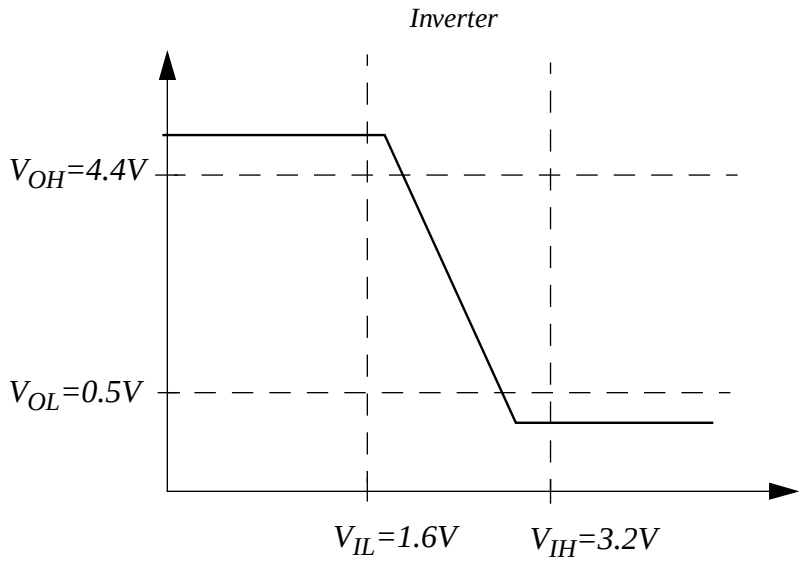


Figure 5.33:

g) 2 meters = 200 cm which translates into 16V of noise peak-to-peak centered at 0, meaning our signal could be plus or minus 8 volts from the desired. The smaller noise margin is NM_0 which equals 1.1 volts. $\frac{8V}{1.1V}$ is 7 something so we need 8 buffers in between the sender and receiver.

h)

$$NM_0 = V_{IL} - V_{OL} = 1.1V$$

$$NM_1 = V_{OH} - V_{IH} = 1.2V$$

If we look at what happens with a triple-buffer at the sender side and at the receiver side, we realize that the noise margins stay the same. Basically this means we are not allowed any more noise during transmission than with a single buffer. If we look at the low noise margin, the minimum voltage the triple-buffer is guaranteed to output for a "low" is still V_{OL} = 0.5V (any logic gate under this static discipline) and likewise, the maximum voltage the receiving triple-buffer is guaranteed to interpret as a "low" is still V_{IL} = 1.6V giving us a 0 noise margin of 1.1V

ANS:: (c) $0.5V$ (d) $4.4V$ (e) $1.6V$ (f) $3.2V$ (g) 8 (f) $NM_0 = 1.1V$, $NM_1 = 1.2V$, unchanged

Problem 5.14 Many manufacturing flaws in digital circuits can be modeled as *stuck-at faults*. The output of a gate is said to suffer from a *stuck-at 1* fault if the output is a 1 irrespective of its input values. Similarly, a *stuck-at 0* fault at an output causes the output to produce a 0 at all times.

a) Consider the circuits shown in Figure 5.34 with one or more faults. Write an expression for each of the outputs in terms of the input variables for the given faults. (Hint: As an example, the output of the faulty circuit in Figure 5.34a will be independent of the input variable C).

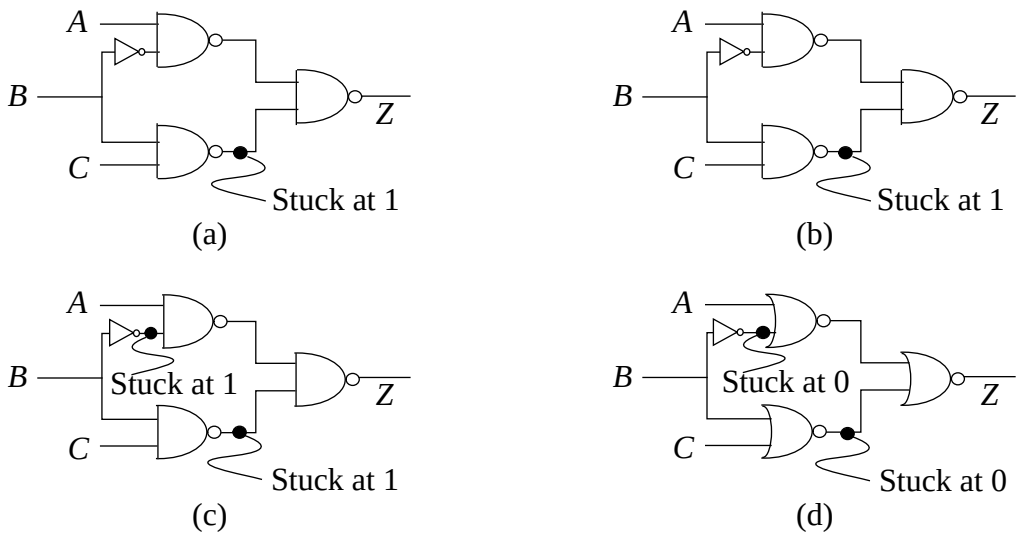


Figure 5.34:

b) Suppose we are given the faulty circuit in Figure 5.35a where the output of NAND gate N2 is known to have a stuck-at fault. However, we do not know whether it is a stuck-at 1 fault or a stuck-at 0 fault. Further, as illustrated in Figure 5.35b, suppose that we have access only to the inputs A, B, and C, and the output Z. In other words, we are unable to directly observe the output X of the faulty NAND gate N2. How would you go about determining whether N2 suffers from a stuck-at 1 fault or a stuck-at 0 fault.

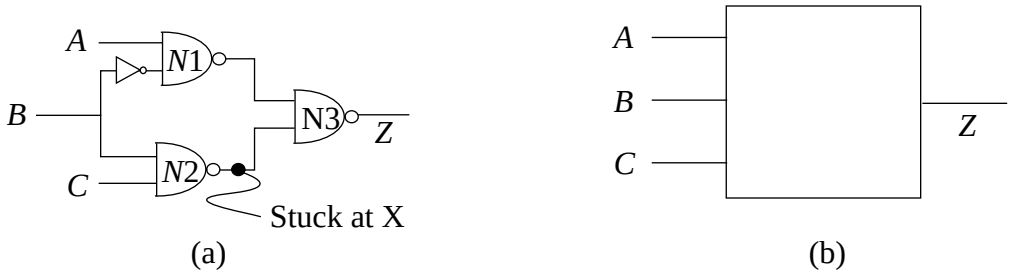


Figure 5.35:

Solution:

a) a) $Z = A\overline{B}$

b) $Z = 1$

c) $Z = A$

d) $Z = A$

b) The boolean for a stuck at 1 is $Z = A\overline{B}$. The boolean for a stuck at 0 is $Z = 1$ One possible test is A = 1 , B = 1. If the output Z = 1 , then it is a stuck at 0 fault. If the output Z = 0, then it is a stuck at 1 fault.

ANS:: (a) $Z = A\overline{B}$ (b) $Z = 1$ (c) $Z = A$ (d) $Z = A$

Chapter 6

The MOSFET Switch

Exercises

Exercise 6.1 Give a resistor-MOSFET implementation of the following logic functions. Use the S model of the MOSFET for this exercise (in other words, you may assume that the on-state resistance of the MOSFETs is 0).

1. $(A + B) \cdot (C + D)$
2. $\overline{A} \cdot \overline{B} \cdot C \cdot D$
3. $(\overline{Y \cdot W})(\overline{X \cdot W})(\overline{\overline{X} \cdot Y \cdot \overline{W}})$

Solution:

1. $(A + B) \cdot (C + D)$
2. $\overline{A} \cdot \overline{B} \cdot C \cdot D$

   Using DeMorgan's laws, we can transform the expression into

$$\overline{A + B + \overline{C \cdot D}}$$

   See Figure 6.1

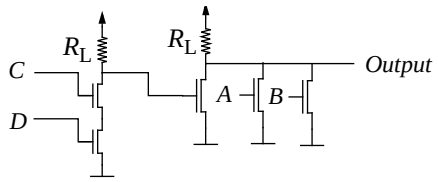


Figure 6.1:

3. $(\overline{Y \cdot W})(\overline{X \cdot W})(\overline{\overline{X} \cdot Y \cdot \overline{W}})$

   Solution:

   Using DeMorgan's laws, we can transform the expression into

$$\overline{Y \cdot W + X \cdot W + \overline{X + W + \overline{Y}}}$$

   See Figure 6.2

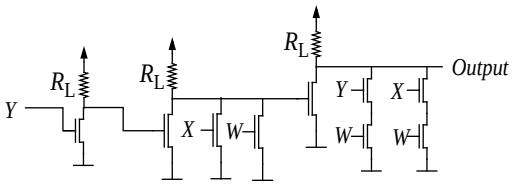


Figure 6.2:

Exercise 6.2 Write a boolean expression that describes the function of each of the circuits in Figure 6.3.

Solution:

a) $OUT = A$

b) $OUT = \overline{\overline{A} + \overline{B}} = A \cdot B$

c) $OUT = \overline{A \cdot (B + \overline{C})}$

d) $OUT = \overline{(A + B + C) \cdot EN}$

ANS:: (a) $OUT = A$ (b) $OUT = A \cdot B$ (c) $OUT = \overline{A \cdot (B + \overline{C})}$ (d) $OUT = \overline{(A + B + C) \cdot EN}$

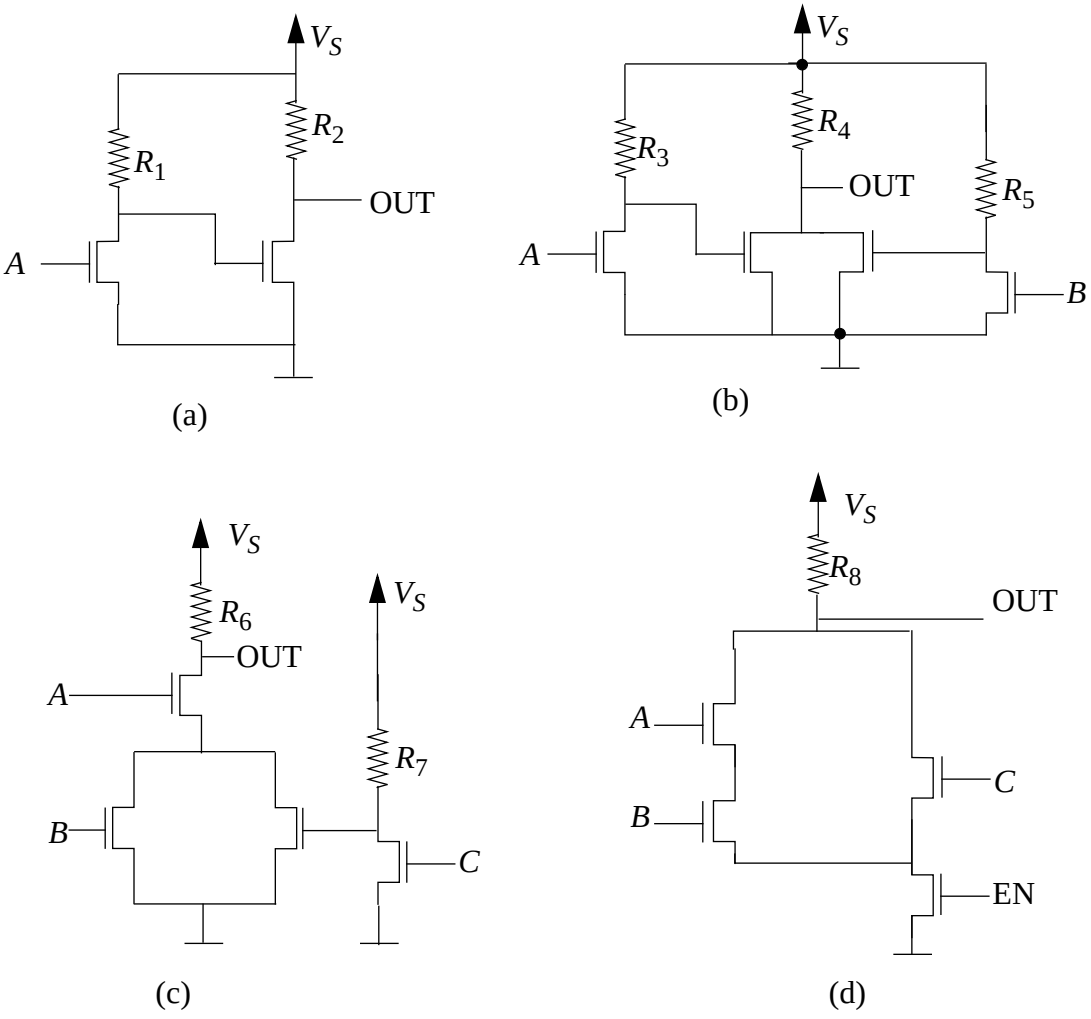

V_S
R_1
R_2
OUT
A
(a)
V_S
R_3
R_4
R_5
OUT
A
B
(b)
V_S
R_6
OUT
A
V_S
R_7
B
C
(c)
V_S
R_8
OUT
A
B
C
EN
(d)

Figure 6.3:

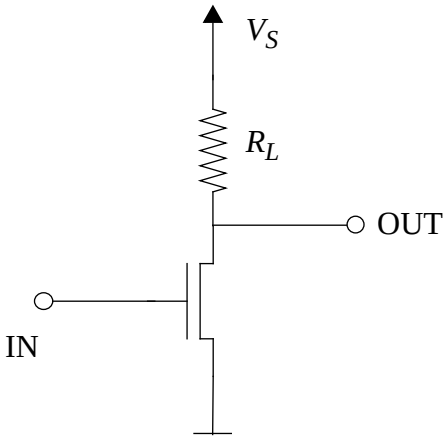


Figure 6.4:

Exercise 6.3 Figure 6.4 shows an inverter circuit using a MOSFET and a resistor. The MOSFET has a threshold voltage $V_T = 2V$. Assume that $V_S = 5V$ and $R_L = 10k$. For this exercise, model the MOSFET using its switch model. In other words, assume that the on-state resistance of the MOSFET is 0.

a) Draw the input versus output voltage transfer curve for the inverter.

b) Does the inverter satisfy the static discipline for the voltage thresholds $V_{OL} = 1V$, $V_{IL} = 1.5V$, $V_{OH} = 4V$ and $V_{IH} = 3V$? Explain. (Hint: To satisfy the static discipline, the inverter must interpret correctly input values that are valid logic signals. Furthermore, given valid logic inputs, the inverter must also output valid logic signals. Valid logic 0 input signals are represented by voltages less than V_{IL}, valid logic 1 input signals are represented by voltages greater than V_{IH}, valid logic 0 output signals are represented by voltages less than V_{OL}, and valid logic 1 output signals are represented by voltages greater than V_{OH}.)

c) Does the inverter satisfy the static discipline if the V_{IL} specification was changed to $V_{IL} = 2.5V$? Explain.

d) What is the maximum value of V_{IL} for which the inverter will satisfy the static discipline?

e) What is the minimum value of V_{IH} for which the inverter will satisfy the static discipline?

Solution:

a) See Figure 6.5 for transfer curve.

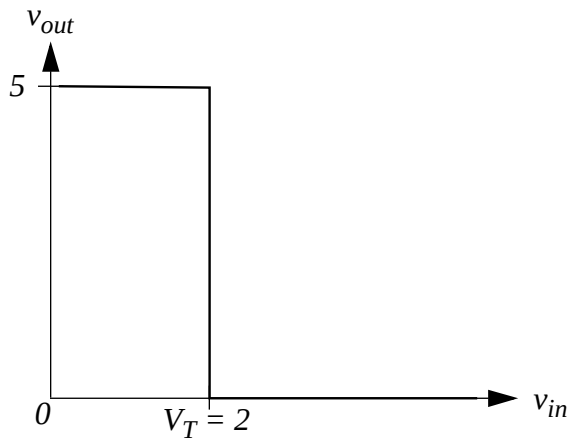


Figure 6.5:

b) Yes, the inverter satisfies the static discipline, as illustrated in Figure 6.6. If the input is less than V_{IL}, then output is always greater than V_{OH}. Similarly, if the input is greater than V_{IH}, then the output is always less than V_{OL}.

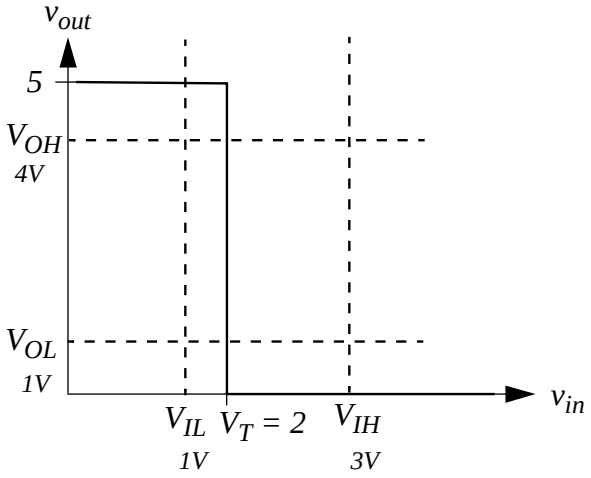


Figure 6.6:

c) No. A case where this would not work is in the input voltage range: $2 < v_{in} < 2.5$. Under the new voltage threshold, input voltages in this range should be interpreted as a logical 0. However, since V_T is at 2V, these would result in $v_{out} = 0$, which is also a logical 0, thereby breaking the static discipline for an inverter.

d) The maximum value of V_{IL} is the threshold voltage V_T. So $V_{IL} < 2$.

e) The minimum value of V_{IH} is also the threshold voltage V_T, because voltages greater than or equal to V_T will be interpreted as a logical 1. So $V_{IH} \geq 2$.

ANS:: (b) yes (c) no (d) 2 (e) 2

Exercise 6.4 Consider, again, the inverter circuit shown in Figure 6.4. The MOSFET has a threshold voltage $V_T = 2V$. Assume that $V_S = 5V$ and $R_L = 10k$. For this exercise, model the MOSFET using its switch-resistor model. Assume that the on-state resistance of the MOSFET is $R_{ON} = 8k$.

a) Does the inverter satisfy the static discipline which has voltage thresholds given by $V_{OL} = V_{IL} = 1V$ and $V_{OH} = V_{IH} = 4V$? Explain.

b) Does the inverter satisfy the static discipline for the voltage thresholds $V_{OL} = V_{IL} = 2.5V$ and $V_{OH} = V_{IH} = 3V$? Explain.

c) Draw the input versus output voltage transfer curve for the inverter.

d) Is there any value of V_{IL} for which the inverter will satisfy the static discipline? Explain.

e) Now assume that $R_{ON} = 1k$ and repeat parts (a), (b), and (c).

Solution:

a) First find the relevant threshold output and input values for the inverter:

The output high voltage is 5.

The output low voltage is

$$V_S \cdot \frac{R_{ON}}{R_{ON} + R_L} = 5 \cdot \frac{8}{18} = 2.2$$

The lowest input voltage recognized as a logical 1 is

$$V_T = 2V$$

The highest input voltage recognized as a logical 0 is less than $2V$.

With $V_{OL} = V_{IL} = 1V$ and $V_{OH} = V_{IH} = 4V$:

No, the static discipline is not satisfied. A failure case is for an input voltage which is greater than $V_{OH} = 4V$ (i.e., a valid 1). Since this high input voltage is greater than the threshold, the inverter output voltage is 2.2V, which is greater than $V_{OL} = 1V$. But this is not a valid 0. Valid 0 outputs would be outputs that are less than 1V.

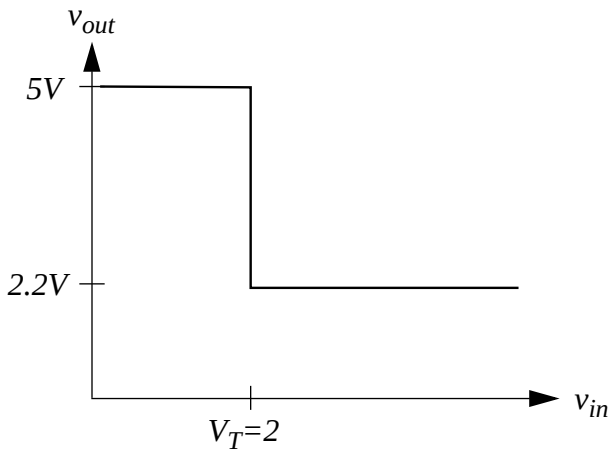


Figure 6.7:

b) With $V_{OL} = V_{IL} = 2.5V$ and $V_{OH} = V_{IH} = 3V$:

No. Now we have a failure case when the input is, say, 2.3V (i.e., a valid 0). But since $2.3 > V_T$, the output will be 2.2V. For a valid inverter the output should have been a valid 1. Thus, this violates the inverter's static discipline.

c) See Figure 6.7 for transfer curve.

d) No. The lowest value the inverter output ever reaches is 2.2V, which is still higher than 2V. Thus the inverter output can never turn the MOSFET in a receiving inverter off. This implies that we will never be able to satisfy the discipline.

e) a) $R_{ON} = 1k$

$$V_{OL} = V_S \cdot (\frac{R_{ON}}{R_{ON} + R_L}) = 5 \cdot \frac{1}{11} = 0.45$$

With $V_{OL} = V_{IL} = 1V$ and $V_{OH} = V_{IH} = 4V$:

Yes, we satisfy the static discipline. For valid 0 input ($< V_{IL}$), then output is always a valid 1 ($> V_{OH}$). For valid 1 input ($> V_{IH}$), the output is always a valid 0 ($< V_{OL}$).

b) With $V_{OL} = V_{IL} = 2.5V$ and $V_{OH} = V_{IH} = 3V$:

No. Counter case is if the input is 2.3V which is $< V_{IL}$ (valid 0), then it will produce an output 0 as well (i.e., $< V_{OL}$).

c) See Figure 6.8 for transfer curve.

ANS:: (a) no (b) no (d) no (e-a) yes (e-b) no

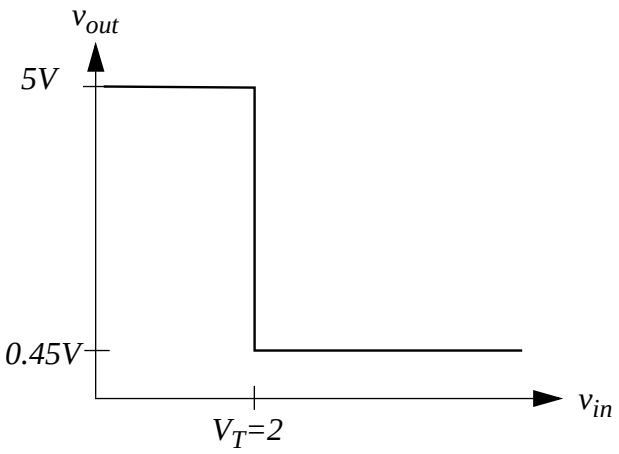


Figure 6.8:

Exercise 6.5 Compute the worst-case power consumed by the inverter shown in Figure 6.4. The MOSFET has a threshold voltage $V_T = 2V$. Assume that $V_S = 5V$ and $R_L = 10k$. Model the MOSFET using its switch-resistor model, and assume that the on-state resistance of the MOSFET is $R_{ON} = 1k$.

Solution:

Power dissipated:

$$\begin{aligned} Power = V_S I &= \frac{V_S^2}{R_L + R_{ON}} \\ &= 5^2 \cdot (\frac{1}{(10+1)10^3}) \\ &= 2.27mW \end{aligned}$$

ANS:: 2.27 mW

Exercise 6.6 Consider again the circuits in Figure 6.3. Using the switch-resistor model of the MOSFET, choose minimum values for the various resistors in Figure 6.3 so each circuit satisfies the static discipline with voltage thresholds given by $V_{IL} = V_{OL} = V_S/10$ and $V_{IH} = V_{OH} = 4V_S/5$. Assume the on-state resistance of the MOSFET is R_{ON} and that its turn-on threshold voltage $V_T = V_S/9$.

Solution:

There are two critical constraints.

First, the valid low input and output voltage thresholds must be less than V_T. The given parameters satisfy this constraint irrespective of the resistor values.

Second, the output low voltage produced by the inverter must be lower than V_{OL}. Let us check this second constraint for each circuit.

a) For this circuit, the following constraint must be satisfied

$$V_{OL} > V_S \cdot \frac{R_{ON}}{R_{ON} + R_1}$$

With $V_{OL} = \frac{V_S}{10}$,

$$\frac{1}{10} > \frac{R_{ON}}{R_{ON} + R_1}$$

$$10R_{ON} < R_{ON} + R_1$$

$$R_1 > 9R_{ON}$$

Similarly,

$$R_2 > 9R_{ON}$$

b) Similarly to part (a),

$$R_3 > 9R_{ON}$$

$$R_5 > 9R_{ON}$$

$$R_4 > 9R_{ON}$$

The same constraint applies to R_4 because the relevant worst case scenario in one in which only one of the MOSFETs associated with R_4 is on.

c) Similarly to part (b),

$$R_7 > 9R_{ON}$$

For R_6, the worst case scenario is when two ON MOSFETs appear in series with resistor R_6, and the third MOSFET is off.

$$R_6 > 9R_{ON,eff}$$

where

$$R_{ON,eff} = R_{ON} + R_{ON} = 2R_{ON}$$

$$R_6 > 18R_{ON}$$

d) Similar to part (c), in the worst case scenario, there are three ON MOSFETs (those with input signals A, B, and EN:

$$R_8 > 9R_{ON,eff}$$
$$R_{ON,eff} = R_{ON} + R_{ON} + R_{ON} = 3R_{ON}$$
$$R_8 > 27R_{ON}$$

ANS:: (a) $R_1 > 9R_{ON}$, $R_2 > 9R_{ON}$ (b) $R_3 > 9R_{ON}$, $R_4 > 9R_{ON}$, $R_5 > 9R_{ON}$ (c) $R_6 > 18R_{ON}$, $R_7 > 9R_{ON}$ (d) $R_8 > 27R_{ON}$

Exercise 6.7 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{\mathrm{OL}} = 0.5$ V, $V_{\mathrm{IL}} = 1.6$ V, $V_{\mathrm{OH}} = 4.4$ V and $V_{\mathrm{IH}} = 3.2$ V.

a) Graph an input-output voltage transfer function of a buffer satisfying the voltage thresholds given above.

b) What is the highest voltage that can be output by an inverter for a logical 0 output?

c) What is the lowest voltage that can be output by an inverter for a logical 1 output?

d) What is the highest voltage that must be interpreted by a receiver as a logical 0?

e) What is the lowest voltage that must be interpreted by a receiver as a logical 1?

f) What is the 0 noise margin provided by this logic family?

g) What is the 1 noise margin provided by this logic family?

h) What is the minimum voltage gain the buffer must provide in the forbidden region?

Solution:

a)
$$V_{OL} = 0.5, V_{IL} = 1.6, V_{OH} = 4.4, V_{IH} = 3.2$$
See Figure 6.9 for transfer function.

b) highest for logical 0: $V_{OL} = 0.5V$

c) lowest for logical 1: $V_{OH} = 4.4V$

d) highest interpreted as logical 0: $V_{IL} = 1.6V$

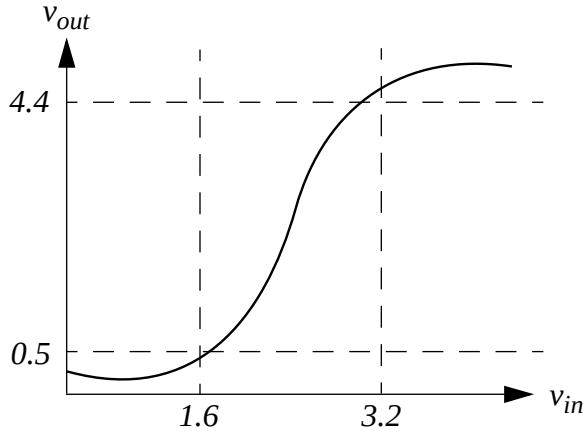


Figure 6.9:

e) lowest interpreted as logical 1: $V_{IH} = 3.2V$

f)
$$NM_0 = V_{IL} - V_{OL} = 1.6 - 0.5 = 1.1V$$

g)
$$NM_1 = V_{OH} - V_{IH} = 4.4 - 3.2 = 1.2V$$

h) Minimum gain: enough to go $V_{OL} \Rightarrow V_{OH}$ at the output for an input transition $V_{IL} \Rightarrow V_{IH}$. In other words,

$$\frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} = \frac{4.4 - 0.5}{3.2 - 1.6} = 2.4$$

ANS:: (b) 0.5 (c) 4.4 (d) 1.6 (e) 3.2 (f) 1.1 (g) 1.2 (h) 2.4

Problems

Problem 6.1

a) Write a truth table and a boolean equation relating the output Z to A, $\overline{A}$, B, and C, when these are input to the circuit shown in Figure 6.10.

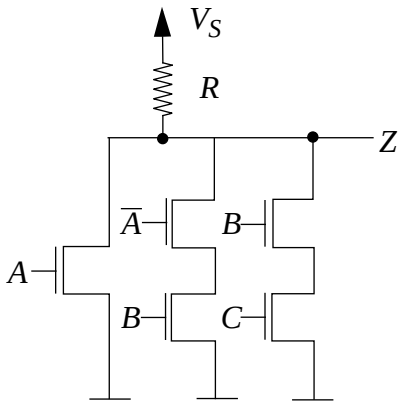


Figure 6.10:

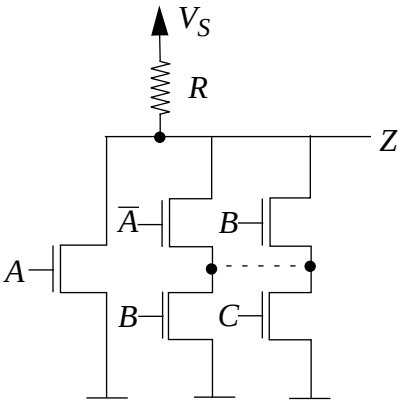


Figure 6.11:

b) Suppose the circuit in Figure 6.10 suffers a manufacturing error which results in a short between the pair of wires depicted in Figure 6.11. Write a truth table and a boolean equation relating the output Z to A, $\overline{A}$, B, and C, for the resulting circuit.

Solution:

a) See table.

A	$\overline{A}$	B	C	Z
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0

A	$\overline{A}$	B	C	Z
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0

b)

ANS:: (a) $Z = \overline{A + B}$ (b) $Z = \overline{A}BC$

Problem 6.2 A specific type of MOSFET has $V_T = -1V$. The MOSFET is in the ON state (a short exists between its drain and source) when $v_{GS} \geq V_T$. The MOSFET is in the OFF state (an open circuit exists between its drain and source) when $v_{GS} < V_T$. (a) Graph the i_{DS} versus v_{GS} characteristics of this MOSFET. (b) Graph the i_{DS} versus v_{DS} characteristics this of the MOSFET for $v_{GS} \geq V_T$ and $v_{GS} < V_T$.

Solution:

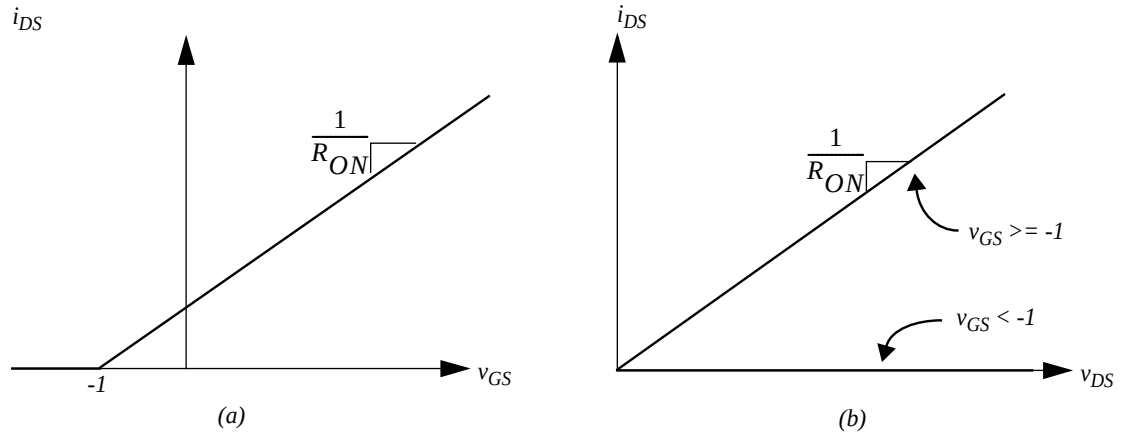


Figure 6.12:

a) See Figure 6.12(a)

Graph of i_{DS} versus v_{GS}: $i_{DS} = 0$ for $v_{GS} < -1$ and $i_{DS} = v_{DS}/R_{on}$ for $v_{GS} > -1$.

b) See Figure 6.12(b)

Graph of i_{DS} versus v_{DS} in an ideal MOSFET: For $v_{GS} < V_T$, i_{DS} versus v_{DS} is zero for all v_{DS}. For $v_{GS} > V_T$, i_{DS} is zero until $v_{DS} > 0$, when i_{DS} increases linearly with a slope of $1/R_{on}$

Problem 6.3 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{OL} = 1$ V, $V_{IL} = 1.3$ V, $V_{OH} = 4$ V, and $V_{IH} = 3$ V. Consider the N-input NAND gate design shown in Figure 6.13. In the design $R = 100k$ and R_{ON} for the MOSFETs is given to be $1k$. V_T for the MOSFETs is 1.5V. What is the maximum value of N for which the NAND gate will satisfy the static discipline? What is the maximum power dissipated by the NAND gate for this value of N?

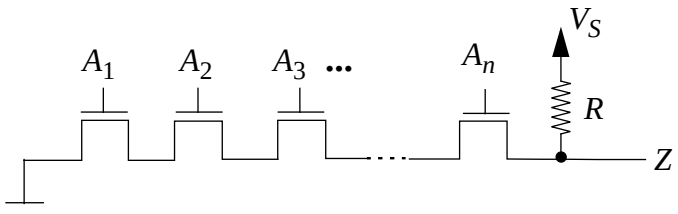


Figure 6.13:

Solution:

Voltage value at Z will equal V_S during a logical 1. During a logical 0, V_S is divided between N R_{ON} and R. Therefore, we require

$V_{Z=0} \leq V_{OL}$

$V_{Z=0} = V_S * \frac{N*R_{ON}}{N*R_{ON}+100k} \leq 1V$

$(V_S - 1)NR_{ON} \leq 100k$

$N \leq \frac{100k}{(V_S-1)R_{ON}}$

Maximum power dissipation when all switches on.

$P_{MAX} = \frac{V_S^2}{100k+NR_{ON}}$

ANS:: $N = \frac{100k}{(V_S-1)R_{ON}}$, $P_{MAX} = \frac{V_S^2}{100k+NR_{ON}}$

Problem 6.4 Consider the N-input NOR gate shown in Figure 6.14. Assume that the on-state resistance of each of the MOSFETs is R_{ON}. For what set of inputs does this gate consume the maximum amount of power? Compute this worst-case power.

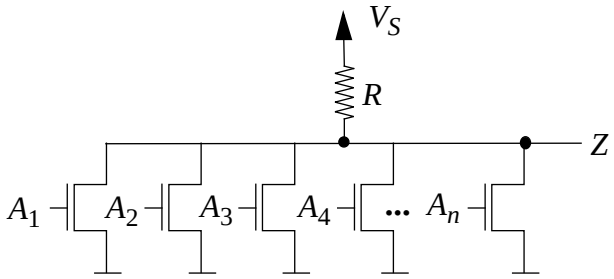


Figure 6.14:

Solution:

Maximum power is consumed when all inputs are high. The equivalent on parallel on resistances decreases to zero for higher N. $P_{MAX} = \frac{V_S^2}{R}$

ANS:: $P_{MAX} = \frac{V_S^2}{R}$

Problem 6.5 Consider the circuit shown in Figure 6.15. We wish to design the circuit so it operates under a static discipline with voltage thresholds V_{OL}, V_{IL}, V_{OH} and V_{IH}. Assume that the on-state resistance of each of the MOSFETs is R_{ON} and that the MOSFET threshold voltage is V_T. Assume that the given values satisfy the constraints $V_S \geq V_{OH}$ and $V_{IL} < V_T$. For what values of n and m does this gate operate under the static discipline? What is the worst case power consumed by this circuit?

Solution:

We can assume that $V_S \geq V_{OH}$ and $V_{IL} < V_T$.

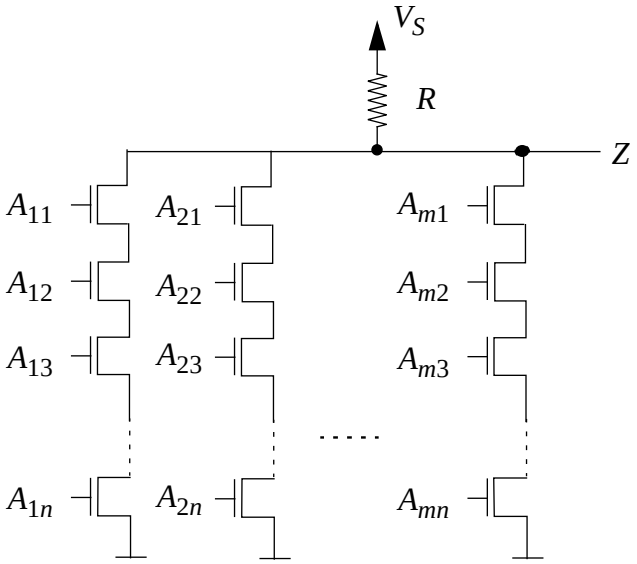


Figure 6.15:

To satisfy the static discipline,

$$V_{OL} \leq \frac{V_S n R_{ON}}{n R_{ON} + R}$$

$$n \leq \frac{V_{OL} R}{(V_S - V_{OL}) R_{ON}}$$

Value m may be any value greater than 0 under the static discipline because each parallel branch contributes only parallel resistances when on.

Worst case power is when all n MOSFET's are ON. Equivalent pull-down resistance approaches zero as m increases. $P_{MAX} = \frac{V_S^2}{R}$

ANS:: $n \leq \frac{V_{OL} R}{(V_S - V_{OL}) R_{ON}}$, m:any value, $P_{MAX} = \frac{V_S^2}{R}$ as m becomes large

Problem 6.6 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{OL} = 0.5V$, $V_{IL} = 1V$, $V_{OH} = 4.5V$, and $V_{IH} = 4.0V$.

a) Graph an input-output voltage transfer function of an inverter satisfying the voltage thresholds given above.

b) Using the switch-resistor MOSFET model, design an inverter satisfying the static discipline for the above voltage thresholds using an n-channel MOSFET and a resistor. The MOSFET has $R_{\mathrm{n}} = 1\,\mathrm{k}\Omega$ and $V_{\mathrm{T}} = 1.8\,V$. Recall, $R_{\mathrm{ON}} = R_{\mathrm{n}}(L/W)$.

Assume $V_S = 5\,V$ and $R_\square$ for a resistor is $500\,\Omega$. Further assume that the area of the inverter is given by the sum of the areas of the MOSFET and the resistor. Assume that the area of a device is $L \times W$. The inverter should take as little area as possible with minimum size for L or W being $0.5\,\mu\text{m}$. Graph the input-output transfer function of the inverter. What is the total area of the inverter? What is its maximum static power dissipation?

Solution:

a) See Figure 6.16.

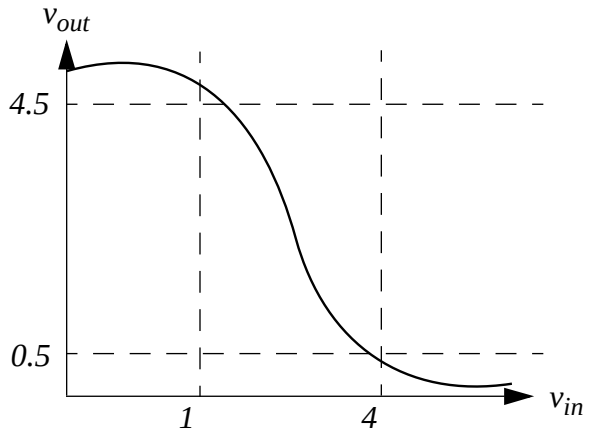


Figure 6.16:

b) The relevant issue in the design is to ensure that the output low voltage produced by the inverter is lower than or equal to V_{OL}.

Therefore, to find the respective (L/W) ratios:

$V_{OL} = V_S \times \frac{R_{ON}}{R_{ON}+R_{PU}}$

$0.5 = 5 \times \frac{R_n(\frac{L_{pd}}{W_{pd}})}{R_n(\frac{L_{pd}}{W_{pd}})+R_\square(\frac{L_{pu}}{W_{pu}})}$

$18(\frac{L_{pd}}{W_{pd}}) = \frac{L_{pu}}{W_{pu}}$

To minimize area, $L_{pd} = 0.5\,\mu\text{m}$ and $W_{pu} = 0.5\,\mu\text{m}$

Use the last equation to minimize the Area equation.

$Area = L_{pd}W_{pd} + L_{pu}W_{pu}$

$L_{pu} = W_{pd} = \frac{3}{\sqrt{2}}\,\mu\text{m}$

ANS:: (b) $Totalarea = \frac{3}{\sqrt{2}}\,\mu\text{m}^2$ and $Power = V_S^2/(R_{ON} + R_{PU})$

Problem 6.7 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{OL} = 0.5V$, $V_{IL} = 0.9V$, $V_{OH} = 4.5V$ and $V_{\text{IH}} = 4V$. Using the switch-resistor MOSFET model, design a 2-input NAND gate satisfying the static discipline for the above voltage thresholds using three n-channel MOSFETs as illustrated in Figure 6.17 (the MOSFET with its gate connected to a voltage V_A and drain connected to the power supply V_S serves as the pull-up). V_A is chosen such that $V_A > V_S + V_T$. The MOSFETs have $R_{\text{n}} = 1\,\text{k}\Omega$ and $V_{\text{T}} = 1.8\,V$. Recall, $R_{\text{ON}} = R_{\text{n}}(L/W)$. Assume $V_S = 5\,V$. Further assume that the area of the NAND gate is given by the sum of the areas of the three MOSFETs. Assume that the area of a device is $L \times W$. The NAND gate should take as little area as possible with minimum size for L or W being $0.5\,\mu\text{m}$. What is the total area of the NAND gate?

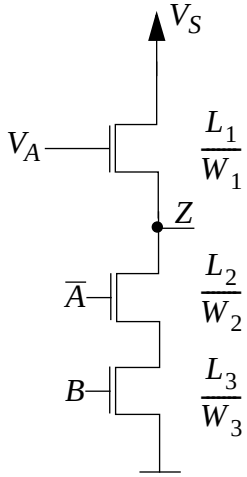


Figure 6.17:

Solution:

Using the same steps as in the previous problem:

The relevant issue in the design is to ensure that the output low voltage produced by the inverter is lower than or equal to V_{OL}.

Therefore, to find the respective (L/W) ratios:

$V_{OL} = V_S \times \frac{R_{ON}}{R_{ON}+R_{PU}}$

$0.5 = 5 \times \frac{R_n(\frac{L_{pd}}{W_{pd}})}{R_n(\frac{L_{pd}}{W_{pd}})+R_{\square}(\frac{L_{pu}}{W_{pu}})}$

$18(\frac{L_2}{W_2} + \frac{L_3}{W_3}) = \frac{L_1}{W_1}$

$18(\frac{L_2W_3+L_3W_2}{W_2W_3}) = \frac{L_1}{W_1}$

The ratios remain the same:

$W_1 = 0.5, L_1 = 3/\sqrt{2}$

$L_2 = L_3 = 0.5, W_2 = W_3 = 1/12\sqrt{2}$

ANS:: $Area = \frac{1}{12\sqrt{2}} + \frac{3}{2\sqrt{2}}$

Problem 6.8 Remember that a NAND gate can be implemented as a circuit with two n-channel MOSFETs and a pull-up resistor $R_{\rm L}$. Let us call it the NAND circuit shown in Figure 6.18. These NAND circuits are used by Penny-Wise Computer Corporation in their computer boards. In one ill-fated shipment of computer boards, the outputs of a pair of NAND circuits get shorted accidentally resulting in the effective Circuit X shown in Figure 6.18.

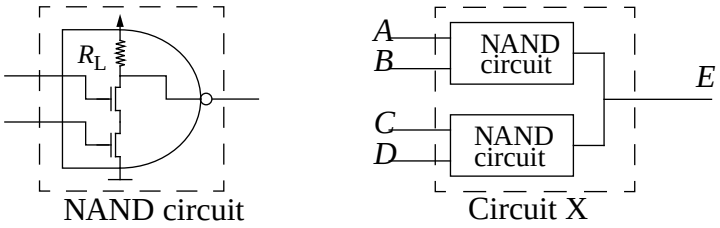


Figure 6.18:

a) What logic function does Circuit X implement? Construct its truth table.

b) If we connect n identical NAND circuits together in parallel forming Circuit Y as shown in Figure 6.19, what is the general form of the logic function it implements?

c) If for each MOSFET, $R_{\rm on} = 500\,\Omega$, $R_{\rm L} = 100\,{\rm k}\Omega$, and $V_{\rm T} = 1.8V$, how many NAND circuits can we connect in parallel and still satisfy the static discipline for the voltage thresholds given by: $V_{\rm IL} = V_{\rm OL}0.5$ V and $V_{\rm IH} = V_{\rm OH} = 4.5$ V.

d) We now connect 10 identical NAND circuits together and have the resulting Circuit Y satisfy the static discipline for the voltage thresholds in Part c) with $R_{\rm L} = 500\,\Omega$. Give specifications on the dimensions of the MOSFETs such that total MOSFET area is minimized. As before, assume that the area of a device is $L \times W$. Assume that $R_{\rm n} = 1\,{\rm k}\Omega$ and no resistor dimension or MOSFET gate dimension should be smaller than $0.5\,\mu{\rm m}$. For what inputs does Circuit Y dissipate maximum static power, and what is that power?

e) Now, suppose choose a static discipline with voltage thresholds given by: $V_{\rm OL} = 0.5$ V, $V_{\rm IL} = 1.6$ V, $V_{\rm OH} = 4.4$ V and $V_{\rm IH} = 3.2$ V. As before, each MOSFET has

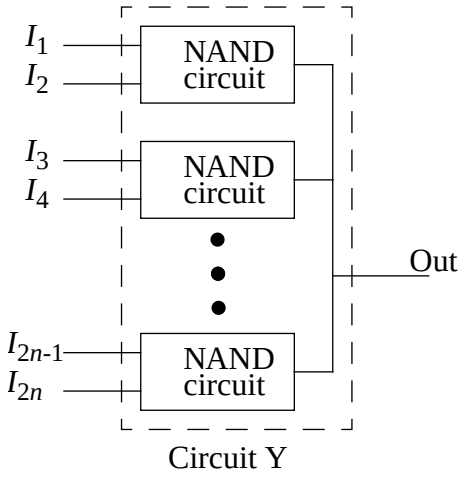


Figure 6.19:

$R_{\text{on}} = 500\,\Omega$, $R_{\text{L}} = 100\,\text{k}\Omega$, and $V_{\text{T}} = 1.8V$. How many NAND circuits can we connect in parallel and still satisfy this static discipline?

f) Repeat part (d) assuming the voltage thresholds given in part (e).

Solution:

a) Shorting the two NAND circuits is like putting two R_L's in parallel above the output line and two pairs of MOSFETS in parallel where each pair is in series.

Circuit X should implement the following logic function

$$\overline{A \cdot B + C \cdot D}$$

b) The logic function has the following form

$$\overline{I_1 \cdot I_2 + I_3 \cdot I_4 + ... + I_{2n-1} \cdot I_{2n}}$$

c) The only relevant threshold that we have to consider is V_{OL}. Thus, taking just one NAND gate on, the following must be satisfied

$$V_{OL} \geq \frac{R_{eq}}{R_L + R_{eq}} V_S$$

We now have two MOSFETs in series giving us an R_{eq} of 1kΩ. Our worst case with n circuits would have only 1 of n NAND gates on but we can't change the fact that

A	B	C	D	$F(A,B,C,D)$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

there are n R_L's in parallel giving an equivalent of R_L/n resulting in the following equation.

$$V_{OL} \geq \frac{R_{eq}}{R_L/n + R_{eq}} V_S$$

Plugging in the values, we see this equation is satisfied for $n \leq 11.11$ so n = 11

d) Again looking at one NAND circuit, it must satisfy the following equation where R_{eq} = $2R_{on}$ = 2k$\Omega \cdot \frac{L}{W}$ since there are two MOSFETs in series

$$V_{OL} \geq \frac{R_{eq}}{R_L + R_{eq}} V_S$$

Substituting the values, we get that $\frac{W}{L} \geq 360$

$$L = 0.5\,\mu\text{m} \qquad and \qquad W = 180\,\mu\text{m}$$

$$R_{on} = \frac{1000}{360} = \frac{25}{9}$$

To maximize the static power, we want the equivalent R_{on} and R_L to be as small as possible since

$$Power \;\; Dissipation = \frac{V_S^2}{R_{on} + R_L}$$

If we turn all inputs on, the equivalent R_{on} has 10 pairs of MOSFETs in parallel which gives 0.56Ω and the 10 R_L resistors in parallel gives 50Ω.

$$Power \;\; Dissipation = 0.49W$$

ANS:: (a) $\overline{A \cdot B + C \cdot D}$ (b) $\overline{I_1 \cdot I_2 + I_3 \cdot I_4 + ... + I_{2n-1} \cdot I_{2n}}$ (c) 11 (d) $L = 0.5\,\mu$m and $W = 180\,\mu$m. $Power = 0.49W$

Problem 6.9 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{\rm OL} = 0.5$ V, $V_{\rm IL} = 1.6$ V, $V_{\rm OH} = 4.4$ V and $V_{\rm IH} = 3.2$ V.

a) Graph an input-output voltage transfer function of an inverter satisfying the voltage thresholds given above.

b) Using the switch-resistor MOSFET model, design an inverter satisfying the static discipline for the above voltage thresholds using an n-channel MOSFET with $R_{\rm n} = 1\,{\rm k}\Omega$ and $V_{\rm T} = 1.8\,V$. Recall, $R_{\rm on} = R_{\rm n}(L/W)$. Assume $V_S = 5\,V$ and $R_\square$ for a resistor is $500\,\Omega$. Further assume that the area of the inverter is given by the sum of the areas of the MOSFET and the resistor. Assume that the area of a device is $L \times W$. The inverter should take as little area as possible with minimum size for L or W being $0.5\,\mu$m. Graph the input-output transfer function of the inverter. What is the total area of the inverter? What is its static power dissipation?

Solution:

a) See Figure 6.20

b) Basically, we need to sift through the given information to see what is important. When the MOSFET is off, there is no current flowing, thus the power dissipated is zero, and the output is just V_S. When the MOSFET turns on, the output must become less than or equal to V_{OL}. A voltage divider relationship results in the following equations

$$V_{OL} \geq \frac{R_{on}}{R_L + R_{on}} V_S$$

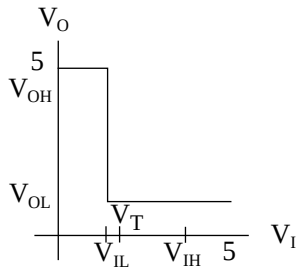


Figure 6.20:

Substituting,

$$0.5 \geq \frac{1000\frac{L}{W}}{1000\frac{L}{W} + 500\frac{L_R}{W_R}}5$$

After lots of algebra,

$$\frac{L_R}{W_R} \cdot \frac{W}{L} \geq 18$$

If we make each ratio a bit above $\sqrt{18}$ or about 4.25 and use the minimum dimension of $0.5\,\mu$m, we get the following values for our design

$$MOSFET \qquad L = 0.5\,\mu\text{m} \;\; and \;\; W = 2.125\,\mu\text{m}$$

$$Resistor \qquad L = 2.125\,\mu\text{m} \;\; and \;\; W = 0.5\,\mu\text{m}$$

$$Total \;\; Area = 2.125\,\mu\text{m}^2$$

$$R_{on} = 235\Omega$$

$$R_L = 2.125k\Omega$$

$$Maximum \;\; Static \;\; Power \;\; Dissipation = \frac{V_S^2}{R_{on} + R_L} = 10.6mW$$

Chapter 7

The MOS Amplifier

Exercises

Exercise 7.1 Determine the voltage v_O across the voltage-dependent current source shown in the circuit in Figure 7.1 when

$$i = f(v) = \frac{K}{v^2}$$

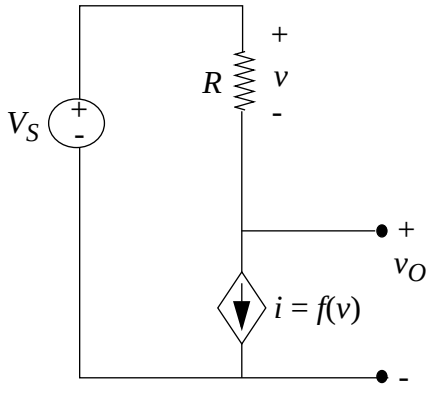


Figure 7.1:

Solution:

$V_S = v + v_O$

$v = Ri = Rf(v) = \frac{RK}{v^2}$

$v^3 = RK$

$v = (RK)^{\frac{1}{3}}$

$v_O = V_S - (RK)^{\frac{1}{3}}$

ANS:: $v_O = V_S - (RK)^{\frac{1}{3}}$

Exercise 7.2 Consider the circuit containing the dependent current source shown in Figure 7.2.

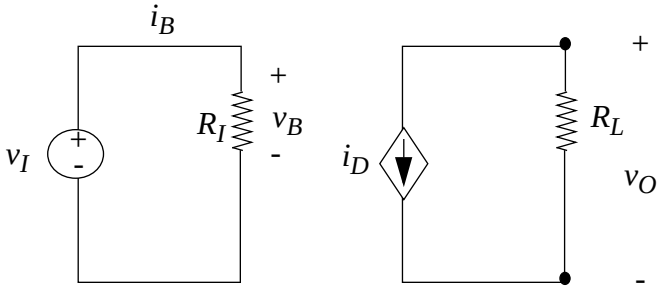


Figure 7.2:

a) Determine v_O in terms of v_I if $i_D = K_1 v_B$. What are the units of K_1?

b) Determine v_O in terms of v_I if $i_D = K_2 i_B$. What are the units of K_2?

c) Determine v_O in terms of v_I if $i_D = K_3 v_B^2$. What are the units of K_3?

d) Determine v_O in terms of v_I if $i_D = K_4 i_B^2$. What are the units of K_4?

Solution:

a) $v_O = -R_L K_1 v_I$

K_1 is in units of $\frac{amperes}{volts}$ or Siemens.

b) $v_O = -R_L K_2 i_B$

$v_O = \frac{-R_L K_2 v_I}{R_I}$

K_2 has no units.

c) $v_O = -R_L K_3 v_B^2$

$v_O = -R_L K_3 v_I^2$

K_3 has units of $\frac{amperes}{volts^2}$

d) $v_O = -R_L K_4 i_B^2 = -R_L K_4 (\frac{v_I}{R_I})^2$

$v_O = \frac{-R_L K_4 v_I^2}{R_I^2}$

K_4 has units of $\frac{1}{amperes}$

ANS:: (a) $v_O = -R_L K_1 v_I$, units: $\frac{amperes}{volts}$ or $\frac{1}{ohms}$ (b) $v_O = \frac{-R_L K_2 v_I}{R_I}$, units: none (c) $v_O = -R_L K_3 v_I^2$, units: $\frac{amperes}{volts^2}$ (d) $v_O = \frac{-R_L K_4 v_I^2}{R_I^2}$, units: $\frac{1}{amperes}$

Exercise 7.3 The resistance R in the circuit shown in Figure 7.3 depends on the voltage across resistor R_B. Determine v_B if

$$R = \frac{K}{v_B}$$

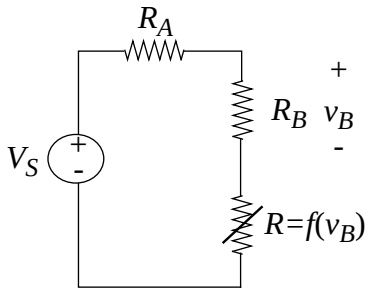


Figure 7.3:

Solution:

$v_B = \frac{R_B V_S}{R_A + R_B + \frac{K}{v_B}}$

$v_B R_A + v_B R_B + K = R_B V_S$

$v_B = \frac{R_B V_S - K}{R_A + R_B}$

ANS:: $v_B = \frac{R_B V_S - K}{R_A + R_B}$

Exercise 7.4 A MOSFET is characterized by the following equation

$$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$$

in its saturation region. A MOSFET operates in the saturation region for

$$v_{DS} \geq v_{GS} - V_T \quad \text{and} \quad v_{GS} \geq V_T$$

Express the $v_{DS} \geq v_{GS} - V_T$ constraint in terms of i_{DS} and v_{DS}.

Solution:

$\frac{2i_{DS}}{K} = (v_{GS} - V_T)^2$

$\sqrt{\frac{2i_{DS}}{K}} = v_{GS} - V_T$

$v_{DS} \geq \sqrt{\frac{2i_{DS}}{K}}$

ANS:: $v_{DS} \geq \sqrt{\frac{2i_{DS}}{K}}$

Exercise 7.5 The MOSFET in Figure 7.4 is characterized by the equation

$$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$$

in its saturation region according to the SCS model. The MOSFET operates in the saturation region for

$$v_{DS} \geq v_{GS} - V_T \quad \text{and} \quad v_{GS} \geq V_T$$

The MOSFET operates in its triode region for

$$v_{DS} < v_{GS} - V_T \quad \text{and} \quad v_{GS} \geq V_T$$

Suppose the MOSFET is characterized by the SR model in its triode region. In other words,

$$i_{DS} = \frac{v_{DS}}{R_{ON}}$$

in the triode region. Assume that R_{ON} is a constant with respect to i_{DS} and v_{DS}, but its value is some function of v_{GS}. Further suppose that $i_{DS} = 0$ when $v_{GS} < V_T$.

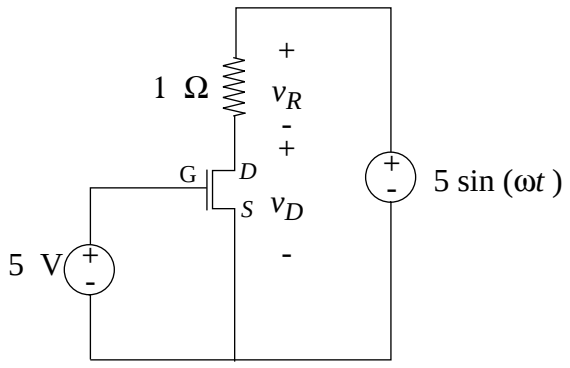


Figure 7.4:

a) For $v_{GS} = 5V$, what value of R_{ON} makes the MOSFET i_{DS} versus v_{DS} characteristic continuous between its triode and saturation regions of operation.

b) Plot v_R versus v_D for the circuit shown in Figure 7.4. This circuit is useful in plotting the MOSFET characteristics. Assume that $K = 1mA/V^2$ and $V_T = 1V$. Use the value of R_{ON} calculated in (a). Use a volt scale for v_D and a millivolt scale for v_R.

Solution:

a) Boundary between triode and saturation regions is when $v_{DS} = v_{GS} - V_T = 5 - V_T$
At this point, $i_{DS} = \frac{K}{2}(5 - V_T)^2$
$R_{ON} = \frac{v_{DS}}{i_{DS}} = \frac{5-V_T}{\frac{K}{2}(5-V_T)^2}$
$R_{ON} = \frac{2}{K(5-V_T)}$

b) $R_{ON} = 500\Omega$
MOSFET is in triode region for $v_D \leq 4volts$. In triode region, $v_R = \frac{v_D}{500}$. In saturation region, $v_R = 8mV$.

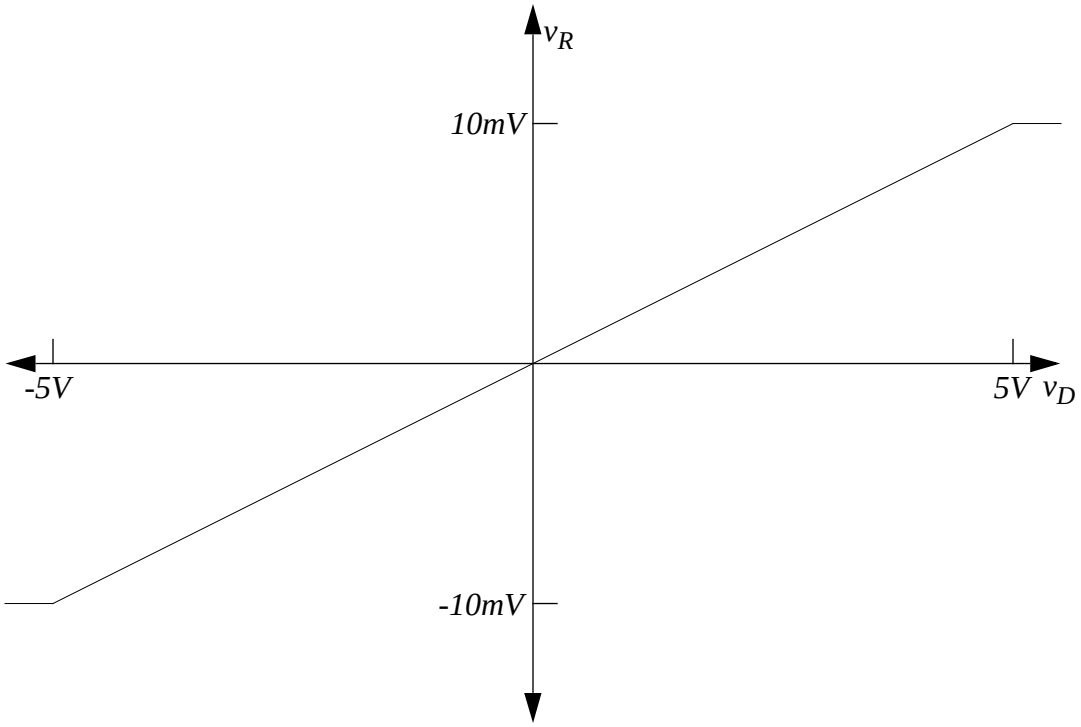


Figure 7.5:

See Figure 7.5.

ANS:: (a) $R_{ON} = \frac{2}{K(5-V_T)}$

Exercise 7.6 Consider the MOSFET amplifier shown in Figure 7.6. Assume that the amplifier is operated under the saturation discipline. In its saturation region, the MOSFET is characterized by the equation

$$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$$

where i_{DS} is the drain-to-source current when a voltage v_{GS} is applied across its gate-to-source terminals.

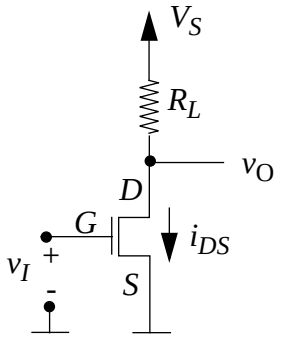


Figure 7.6:

a) Draw the equivalent circuit for the amplifier based on the SCS model of the MOSFET.

b) Write an expression relating v_O to i_{DS}.

c) Write an expression relating i_{DS} to v_I.

d) Write an expression relating v_O to v_I.

e) Suppose that an input voltage V_I results in an output voltage V_O. By what factor must V_I be increased (or decreased) so that the output voltage is doubled.

f) Suppose, again, that an input voltage V_I results in an output voltage V_O. Suppose, further, that we desire an output voltage that is $2V_O$. Assuming that both the input voltage and the MOSFET do not change, what are all the possible ways of accomplishing the desired doubling of the output voltage.

g) The power consumed by the MOSFET amplifier in Figure 7.6 is given by $V_S i_{DS}$, assuming that no current is draw out of the v_O terminal. Which of the alternatives for doubling V_O from parts (e) and (f) will result in the lowest power consumption.

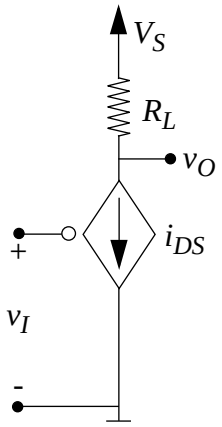


Figure 7.7:

Solution:

a) See Figure 7.7.

b) $v_O = V_S - R_L i_{DS}$

c) $i_{DS} = \frac{K}{2}(v_I - V_T)^2$ for $v_I \geq V_T$; $i_{DS} = 0$ otherwise

d) $v_O = V_S - \frac{R_L K}{2}(v_I - V_T)^2$ for $v_I \geq V_T$; $v_O = V_S$ otherwise

e) $V_O = V_S - \frac{R_L K}{2}(V_I - V_T)^2$

$2V_O = V_S - \frac{R_L K}{2}(NV_I - V_T)^2$

$V_S - 2V_O = \frac{R_L K}{2}(NV_I - V_T)^2$

$\frac{2}{R_L K}(V_S - 2V_O) = (NV_I - V_T)^2$

$NV_I - V_T = \sqrt{\frac{2}{R_L K}(V_S - 2V_O)}$

$N = \frac{\sqrt{\frac{2}{R_L K}(V_S - 2V_O)} + V_T}{V_I}$; $2V_O \leq V_S$

Scale V_I by factor N

f) $V_O = V_S - \frac{K R_L}{2}(V_I - V_T)^2$

This can be accomplished by changing V_S, R_L, or by changing both.

By changing R_L:

$2V_O = V_S - \frac{K R_L N_R}{2}(V_I - V_T)^2$

$N_R = \frac{2V_S - 4V_O}{K R_L (V_I - V_T)^2}$

Scale R_L by factor N_R. This will only work if $2V_O \leq V_S$

By changing V_S:

$2V_O = N_S V_S - \frac{KR_L}{2}(V_I - V_T)^2$

$N_S = \frac{2V_O + \frac{KR_L}{2}(V_I - V_T)^2}{V_S}$

Scale V_S by factor N_S

By changing V_S and R_L:

Scale V_S by factor X and scale R_L by factor Y where

$X = \frac{2V_O + \frac{KR_LY}{2}(V_I - V_T)^2}{V_S}$. This will only work if $2V_O \leq XV_S$

g) The alternative from part e results in the lowest power consumption.

ANS:: (b) $v_O = V_S - R_L i_{DS}$ (c) $i_{DS} = \frac{K}{2}(v_I - V_T)^2$ for $v_I \geq V_T$; $i_{DS} = 0$ otherwise (d) $v_O = V_S - \frac{R_L K}{2}(v_I - V_T)^2$ for $v_I \geq V_T$; $v_O = V_S$ otherwise (e) $N = \frac{\sqrt{\frac{2}{R_L K}(V_S - 2V_O)} + V_T}{V_I}$ (g) e

Exercise 7.7 Consider, again, the MOSFET amplifier shown in Figure 7.6. Assume that the amplifier is operated under the saturation discipline. The MOSFET in doctored so its threshold voltage is 0. In other words, the saturation region of the MOSFET is now characterized by the equation

$$i_{DS} = \frac{K}{2} v_{GS}^2$$

where i_{DS} is the drain-to-source current when a voltage v_{GS} is applied across its gate-to-source terminals. The following questions relate to the large-signal analysis of the amplifier.

a) Derive the relationship between the output voltage v_O and the input voltage v_I.

b) Derive the range of valid input voltages. Under the saturation discipline, valid input voltages are those which result in saturation region operation of the amplifier. Determine the corresponding range of output voltages (v_O) and output currents (i_{DS}).

c) Suppose we wish to amplify an AC input signal v_i. Assume that v_i has a zero DC offset. Draw a circuit showing how a separate DC input voltage V_I can be used to bias the amplifier in a region where saturation region operation is achieved for both positive and negative excursions of v_i. Assuming the v_i has symmetric positive and negative swings, how would you choose the input operating point for the amplifier which allows a maximum peak-to-peak voltage range for v_i. What is the corresponding output operating point (v_O and i_{DS}).

Solution:

a) $v_O = V_S - i_{DS}R_L$

$v_O = V_S - \frac{KR_L v_I^2}{2}$

b) $0 \leq v_I \leq \frac{\sqrt{1+2KR_LV_S}-1}{KR_L}$

$\frac{\sqrt{1+2KR_LV_S}-1}{KR_L} \leq v_O \leq V_S$

$0 \leq i_{DS} \leq \frac{1+KR_LV_S-\sqrt{1+2KR_LV_S}}{KR_L^2}$

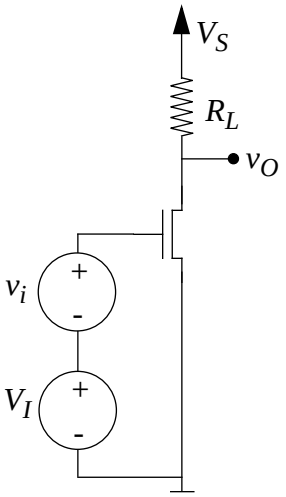


Figure 7.8:

c) See Figure 7.8.

An operating point that is in the middle of the range of valid inputs allows a maximum peak-to-peak voltage range for v_i.

$V_I = \frac{\sqrt{1+2KR_LV_S}-1}{2KR_L}$

$V_O = \frac{3KR_LV_S-1+\sqrt{1+2KR_LV_S}}{4KR_L}$

$I_{DS} = \frac{1+KR_LV_S-\sqrt{1+2KR_LV_S}}{4KR_L^2}$

ANS:: (a) $v_O = V_S - \frac{KR_L v_I^2}{2}$ (b) $0 \leq i_{DS} \leq \frac{1+KR_LV_S-\sqrt{1+2KR_LV_S}}{KR_L^2}$ (c) $V_I = \frac{\sqrt{1+2KR_LV_S}-1}{2KR_L}$, $V_O = \frac{3KR_LV_S-1+\sqrt{1+2KR_LV_S}}{4KR_L}$, $I_{DS} = \frac{1+KR_LV_S-\sqrt{1+2KR_LV_S}}{4KR_L^2}$

Exercise 7.8 The three terminal device shown in Figure 7.9a is called a bipolar junction transistor (BJT). Figure 7.9b shows a piecewise linear model for the device, in which the parameter β is a constant. When

$$i_B > 0$$

and

$$v_{CE} > v_{BE} - 0.4$$

the emitter diode behaves like a short circuit, the collector diode like an open circuit, and the collector current is given by

$$i_C = \beta i_B$$

Under the above constraints, the BJT is said to operate in its active region. For the rest of this exercise, assume that $\beta = 100$.

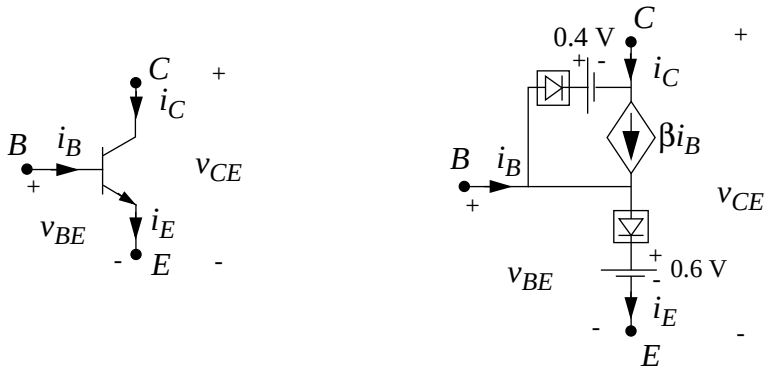


Figure 7.9: (a) A bipolar junction transistor. B stands for base, E for emitter and C for collector. (b) A piecewise linear model for the BJT

a) Determine the collector current i_C for a base current $i_B = 1\mu A$ and $v_{CE} = 2V$ using the model in Figure 7.9b.

b) Sketch a graph of i_C versus v_{CE} for $i_B = 1\mu A$. using the model in Figure 7.9b. In drawing this graph, assume that the current source turns off for

$$v_{CE} \leq v_{BE} - 0.4$$

Solution:

a) Since $i_B > 0$ and $v_{CE} > 0.2V$, the BJT operates in its active region.

$$i_C = \beta i_B = 100\mu A$$

b) The graph of i_C versus v_{CE} will look like this:

For v_{CE} from 0 to 0.2V, $i_C = 0$.

Then, for v_{CE} greater than 0.2V, $i_C = 100\mu A$.

ANS:: (a) $i_C = 100\mu A$

Exercise 7.9 Consider the bipolar junction transistor (BJT) amplifier shown in Figure 7.10. Assume that the BJT is characterized by the large signal model from Exercise 7.8, and that the BJT operates in its active region. Assume further that $V_S = 5V$, $R_L = 10k$, $R_I = 500k$, and $\beta = 100$.

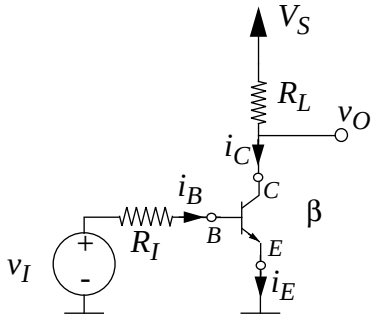


Figure 7.10:

a) Draw the equivalent circuit for the BJT amplifier based on the large signal BJT model from Exercise 7.8.

b) Write an expression relating v_O to i_C.

c) Write an expression relating i_C to v_I.

d) Write an expression relating i_E to i_B.

e) Write an expression relating v_O to v_I.

f) What is the value of v_O for an input voltage $v_I = 0.7$V? What are the corresponding values of i_B, i_C and i_E.

Solution:

a)

b)

$$v_O = V_S - i_C R_L$$

c)

$$i_C = \beta i_B = \beta \frac{v_I - 0.6}{R_I}$$

d)

$$i_E = i_B(\beta + 1)$$

e)

$$v_O = V_S - \frac{v_I - 0.6}{R_I}\beta R_L$$

Or, substituting known values

$$v_O = 6.2 - 2v_I$$

f) $v_O = 4.8V$, $i_B = 0.2\mu A$, $i_C = 20\mu A$, and $i_E = 20.2\mu A$.

ANS:: (b) $v_O = V_S - i_C R_L$ (c) $i_C = \beta \frac{v_I - 0.6}{R_I}$ (d) $i_E = i_B(\beta + 1)$ (e) $v_O = 6.2 - 2v_I$ (f) $v_O = 4.8V$, $i_B = 0.2\mu A$, $i_C = 20\mu A$, and $i_E = 20.2\mu A$.

Exercise 7.10 In this exercise you will perform a large signal analysis of the BJT amplifier shown in Figure 7.10. Assume that the BJT is characterized by the large signal model from Exercise 7.8. Assume further that $V_S = 5V$, $R_L = 10k$, $R_I = 500k$, and $\beta = 100$.

a) Write an expression relating v_O to v_I.

b) What is the lowest value of the input voltage v_I for which the BJT operates in its active region? What are the corresponding values of i_B, i_C, and v_O?

c) What is the highest value of the input voltage v_I for which the BJT operates in its active region? What are the corresponding values of i_B, i_C, and v_O?

d) Sketch a graph of v_O versus v_I for the parameter values given above.

Solution:

a)

$$v_O = V_S - \frac{v_I - 0.6}{R_I}\beta R_L$$

Or, substituting known values

$$v_O = 6.2 - 2v_I$$

b)

$$v_I = 0.6V$$

The BJT goes into cutoff if v_I goes any lower.

The corresponding values of i_B, i_C, and v_O are as follows. $i_B = 0$, $i_C = 0$, and $v_O = 5V$.

c) As v_I increases, the BJT enters saturation when the collector diode gets forward biased. This happens when the base voltage is greater than the collector voltage by 0.4V. In other words, when $v_{CE} = v_{BE} - 0.4$, or when $v_{CE} = v_O$ falls to 0.2V. The corresponding value of v_I is obtained by solving

$$v_O = 0.2 = 6.2 - 2v_I$$

Solving, we get $v_I = 3V$. In other words, when v_I rises to 3V, the output falls to 0.2V, and the BJT goes into saturation.

The corresponding values of i_B, i_C, and v_O are as follows. $i_B = 24/5\mu A$, $i_C = 480\mu A$, and $v_O = 0.2V$.

d) A graph of v_O versus v_I is made up of three straightline segments.

In the first segment, v_O is at 5V for v_I ranging from 0V to 0.6V.

In the second segment, v_O decreases linearly from 5V to 0.2V as v_I increases from 0.6V to 3V. In other words, the second segment follows the equation

$$v_O = 0.2 = 6.2 - 2v_I$$

for $v_I = 0.6V$ to $v_I = 3V$.

In the third segment, v_O stays at 0.2V for v_I greater than 3V.

ANS:: (a) $v_O = 6.2 - 2v_I$ (b) $v_I = 0.6V$, $i_B = 0$, $i_C = 0$, and $v_O = 5V$. (c) $v_I = 3V$, $i_B = 24/5\mu A$, $i_C = 480\mu A$, and $v_O = 0.2V$.

Problems

Problem 7.1 Consider the MOSFET voltage divider circuit shown in Figure 7.11. Assume that both MOSFETs operate in the saturation region. Determine the output voltage V_O as a function of the supply voltage V_S, the gate voltages V_A and V_B, and the MOSFET geometries L_1, W_1 and L_2, W_2. Assume that the MOSFET threshold voltage is V_T, and remember, $K = K_n \frac{W}{L}$.

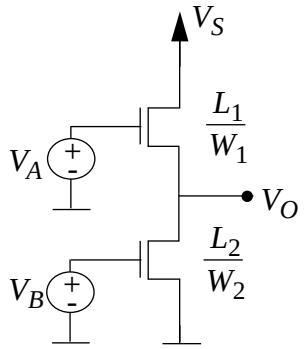


Figure 7.11:

Solution:

Since the current through both MOSFETs must be the same, V_O is forced to a value such that this is the case.

$$\frac{K_n W_2}{2L_2}(V_B - V_T)^2 = \frac{K_n W_1}{2L_1}(V_A - V_O - V_T)^2$$

$$V_O = V_A - V_T - \sqrt{\frac{W_2 L_1}{L_2 W_1}(V_B - V_T)^2}$$

ANS:: $V_O = V_A - V_T - \sqrt{\frac{W_2 L_1}{L_2 W_1}(V_B - V_T)^2}$

Problem 7.2 An inverting MOSFET amplifier is shown in Figure 7.12, together with an $i_{\rm DS}$-$v_{\rm DS}$ characteristic for the MOSFET. This characteristic is simpler than the SCS model presented in this chapter. The characteristic is simply the standard MOSFET characteristic with the triode region compressed onto the Y axis.

Alternatively, this characteristic can be viewed as describing ideal switch behavior that is extended to exhibit a saturating drain-source current. In other words, for $v_{\rm GS} < V_{\rm T}$, the MOSFET behaves like an open switch with $i_{\rm DS} = 0$. For $v_{\rm GS} \geq V_{\rm T}$, the MOSFET behaves like a closed switch with $v_{\rm DS} = 0$ provided that $i_{\rm DS} < \frac{K}{2}(v_{\rm GS} - V_{\rm T})^2$. However, once $i_{\rm DS}$ reaches $\frac{K}{2}(v_{\rm GS} - V_{\rm T})^2$, which is the maximum current the MOSFET can carry for a given $v_{\rm GS}$, MOSFET operation enters a saturation region in which the MOSFET behaves as a current source of value $\frac{K}{2}(v_{\rm GS} - V_{\rm T})^2$. Saturated operation is as described by the saturation model given in Figure 7.12.

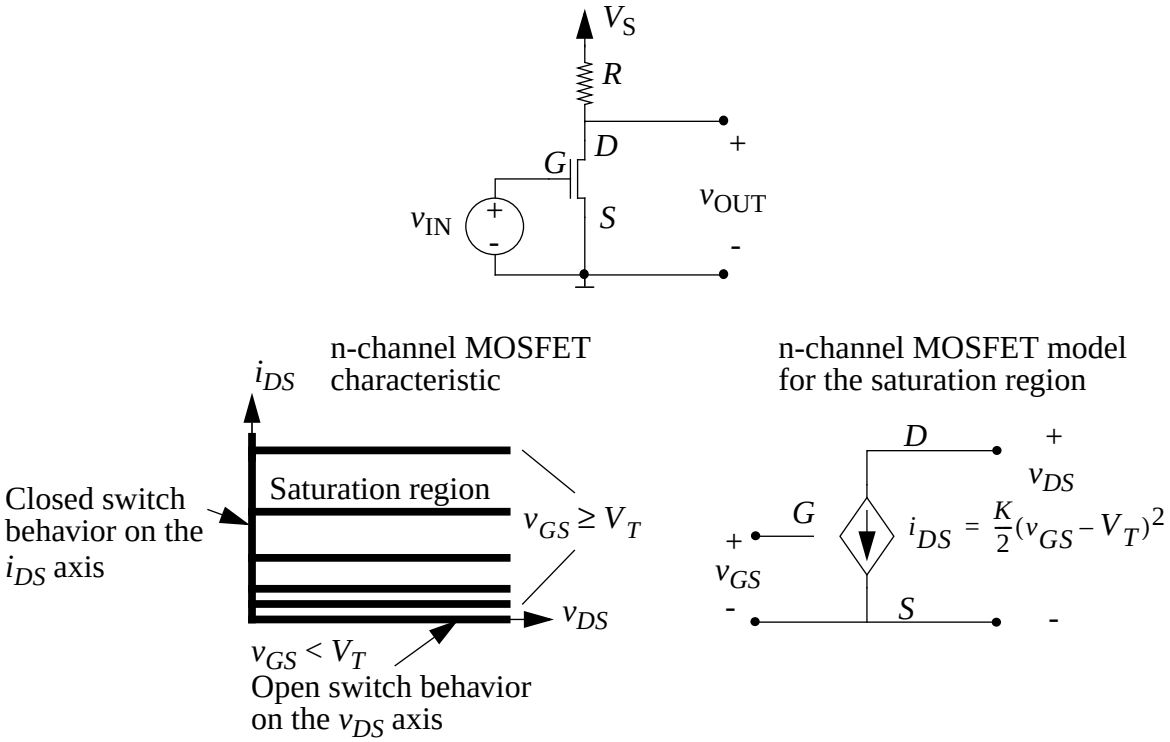


Figure 7.12:

a) Determine $v_{\rm OUT}$ as a function of $v_{\rm IN}$ for $0 \leq v_{\rm IN}$.

b) What is the lowest value of $v_{\rm IN}$ for which $v_{\rm OUT} = 0$?

c) Assume that $V_{\rm S} = 15$ V, $R = 15$ kΩ, $V_{\rm T} = 1$ V and $K = 2$ mA/V^2. Graph $v_{\rm OUT}$ versus $v_{\rm IN}$ for 0 V $\leq v_{\rm IN} \leq$ 3 V.

d) On the input-output graph, identify the regions over which the MOSFET behaves as an open circuit, behaves as a short circuit, and exhibits saturated behavior.

Solution:

a) When there is current going through R, the current is limited by two quantities: either $\frac{V_S}{R}$ or $\frac{K}{2}(v_{GS} - V_T)^2$, whichever is lower. If the limit is V_S/R, then the MOSFET is in the closed-switch region. If the limit is $\frac{K}{2}(v_{GS} - V_T)^2$, then the MOSFET is in the saturation region.

open-switch region For $v_{GS} \leq V_T$, the MOSFET is open, therefore $v_{OUT} = V_S$.

saturation region When v_{GS} begins to exceed V_T, the quantity $v_{GS} - V_T$ is still small, so the current is limited by $\frac{K}{2}(v_{GS} - V_T)^2$. This current determines the output voltage, which is given by $v_{OUT} = V_S - \frac{KR}{2}(v_{IN} - V_T)^2$.

closed-switch region i_{DS} increases until it reaches $\frac{V_S}{R}$ at some gate voltage V_{IN_T}. Now v_{DS} drops to zeros, and both i_{DS} and v_{DS} are no longer affected by the increase in v_{GS}.

In summary,

$$v_{OUT} = \begin{cases} V_S & 0 \leq v_{IN} \leq V_T \\ V_S - \frac{KR}{2}(v_{IN} - V_T)^2 & v_T \leq v_{IN} \leq V_{IN_T} \\ 0 & V_{IN_T} \leq v_{IN} \leq V_{IN_{MAX}} \end{cases}$$

b) The lowest value of v_{IN} for which $v_{OUT} = 0$ occurs when v_{IN} is at the *transition* between the saturation region and the closed-switch region. At this point, the saturation region current limit and the closed-switch region current limit are the same,

$$i_{DS} = \frac{V_S}{R} = \frac{K}{2}(V_{IN_T} - V_T)^2$$

Solving for V_{IN_T} we get

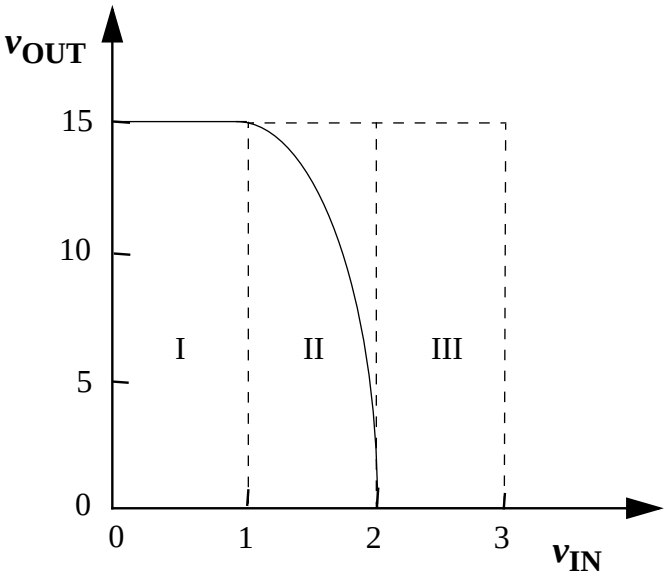
$$V_{IN_T} = \sqrt{\frac{2V_S}{KR}} + V_T$$

c) Combining the results of part (a) and (b), we obtain the following equations.

$$v_{OUT} = \begin{cases} 15 & 0 \leq v_{IN} \leq 1 \\ 15 - 15(v_{IN} - 1)^2 & 1 \leq v_{IN} \leq 2 \\ 0 & 2 \leq v_{IN} \leq 3 \end{cases}$$

The graph is shown in the figure.

d) Region I is the open switch region, where $v_{OUT} = V_S = 15$. Region II is the saturation region, where v_{OUT} drops according to $V_S - \frac{KR}{2}(v_{IN} - V_T)^2$. The MOSFET enters the closed-switch region when $v_{IN} = V_{IN_T} = 2$. In this region, $v_{OUT} = 0$.



ANS:: (b)$V_{\mathrm{IN_T}} = \sqrt{\frac{2V_S}{KR}} + V_T$

Problem 7.3 A two-stage amplifier is shown in Figure 7.13. It is constructed by cascading two one-stage amplifiers of the type seen in Problem 7.2. In analyzing this amplifier, use the MOSFET model described in Problem 7.2 and illustrated in Figure 7.12.

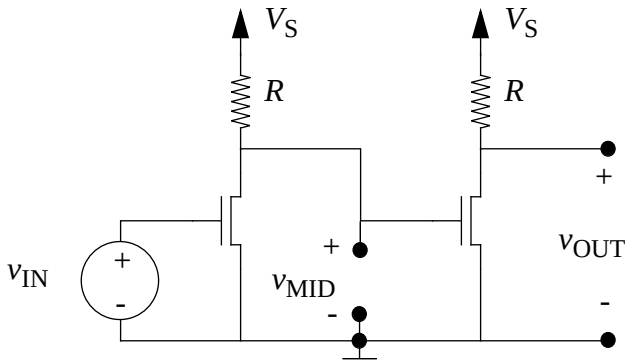


Figure 7.13:

a) The fact that a second amplifier stage is connected to the first amplifier stage does not change the operation of the first stage. That is, the relation between v_{MID} and v_{IN} here is the same as the relation between v_{OUT} and v_{IN} in Problem 7.2. Why? What terminal characteristic of the second MOSFET must change in order for this not to be true?

b) Derive the relation between v_{MID} and v_{IN} for $0 \leq v_{\mathrm{IN}}$, and the relation between v_{OUT} and v_{MID} for $0 \leq v_{\mathrm{MID}} \leq V_{\mathrm{S}}$. Hint: see Problem 7.2.

c) Derive the relation between $v_{\rm OUT}$ and $v_{\rm IN}$ for $0 \leq v_{\rm IN}$.

d) Determine the range of input voltages for which both MOSFETs operate under the saturation discipline. What are the corresponding ranges for $v_{\rm MID}$ and $v_{\rm OUT}$?

e) Using the numerical parameters given in Problem 7.2, graph $v_{\rm OUT}$ versus $v_{\rm IN}$ for $v_{\rm IN}$ for 0 V $\leq v_{\rm IN} \leq$ 3 V. Compare this graph to the input-output graph found in Problem 7.2, and explain the differences.

Solution:

a) The second amplifier does not change the operation of the first because its input draws no current. If the second amplifier drew current from the first, then the output of the first amplifier would be affected by the input resistance of the second amplifier.

b) There are three modes of operation for each amplifier. The cutoff and the saturation modes will be considered, and the triode mode will be ignored for now. In saturation, the equations derived in Problem 8.2 remain valid, as does the threshold voltage. We must also figure out the threshold between the saturation and triode regimes. The MOSFET is in saturation when $V_{\rm DS} \geq V_{\rm GS} - V_{\rm T}$. This implies that $v_{\rm MID} \geq v_{\rm IN} - V_{\rm T}$, or that $V_{\rm S} - \frac{KR}{2}(v_{\rm IN} - V_{\rm T})^2 \geq v_{\rm IN} - V_{\rm T}$. This implies that

$$v_{\rm IN} \leq V_{\rm T} + \frac{-1 + \sqrt{1 + 2KRV_{\rm S}}}{KR}.$$

Let us define $V_{\rm IN_T}$ to be this threshold.

A similar calculation can be made for $v_{\rm OUT}$ vs. $v_{\rm MID}$.

For the first amplifier,

$$v_{\rm MID} = \begin{cases} V_{\rm S} & 0 \leq v_{\rm IN} \leq V_{\rm T} \\ V_{\rm S} - \frac{KR}{2}(v_{\rm IN} - V_{\rm T})^2 & V_{\rm T} \leq v_{\rm IN} \leq V_{\rm IN_T} \\ f(v_{\rm IN}) & V_{\rm IN_T} \leq v_{\rm IN} \leq V_{\rm IN_{MAX}} \end{cases}$$

For the second amplifier,

$$v_{\rm OUT} = \begin{cases} V_{\rm S} & 0 \leq v_{\rm MID} \leq V_{\rm T} \\ V_{\rm S} - \frac{KR}{2}(v_{\rm MID} - V_{\rm T})^2 & V_{\rm T} \leq v_{\rm MID} \leq V_{\rm MID_T} \\ f(v_{\rm MID}) & V_{\rm MID_T} \leq v_{\rm MID} \leq V_{\rm MID_{MAX}} \end{cases}$$

c) This part is trickier.

First of all, if $v_{\rm IN} \leq V_{\rm T}$ then $v_{\rm MID} = V_{\rm T}$, so the second FET will be either in saturation or triode, depending on the value of R. Let us find the condition for saturation.

$$V_{\rm S} \leq V_{\rm T} - \frac{1}{KR} + \sqrt{\frac{1}{K^2R^2} + \frac{2V_{\rm S}}{KR}}.$$

Simplifying this, one gets:

$$KR \leq \frac{2V_{\rm T}}{(V_{\rm S} - V_{\rm T})^2}.$$

Let us assume that R is large enough that if $v_{\rm IN} \leq V_{\rm T}$, the second FET will be in triode. Then, while the first FET is in saturation, we can find the minimum value for which the second FET also enters saturation.

$$v_{\rm MID} \geq V_{\rm T} - \frac{1}{KR} + \sqrt{\frac{1}{K^2R^2} + \frac{2V_{\rm S}}{KR}}.$$

Substituting in for $v_{\rm MID}$ and simplifying, we get that

$$v_{\rm IN} \leq V_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} + \frac{2}{K^2R^2} - \sqrt{\frac{4}{K^4R^4} + \frac{8V_{\rm S}}{K^3R^3}}}.$$

Now, we can prove that the second FET entered saturation before the first FET left it. We prove that the value just derived is less than the boundary condition for the first FET to leave saturation.

This expression:

$$V_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} + \frac{2}{K^2R^2} - \sqrt{\frac{4}{K^4R^4} + \frac{8V_{\rm S}}{K^3R^3}}}.$$

Must be less than this expression:

$$V_{\rm T} - \frac{1}{KR} + \sqrt{\frac{1}{K^2R^2} + \frac{2V_{\rm S}}{KR}}.$$

This simplifies to

$$\frac{-2V_{\rm T}}{KR} \leq 0.$$

This is always true for NFETs, which is what we are using, so we have proven that there will be a range for which both FETs are in saturation. Next, either the first FET will enter triode, or the second will enter cutoff. Since we are not dealing with the triode region, it is easier to assume that the second will enter cutoff while the first is still in saturation. Therefore, we want to have both of the following equations satisfied:

$$v_{\rm IN} \leq V_{\rm T} - \frac{1}{KR} + \sqrt{\frac{1}{K^2R^2} + \frac{2V_{\rm S}}{KR}}$$

$$V_{\rm S} - \frac{KR}{2}(v_{\rm IN} - V_{\rm T})^2 \leq V_{\rm T}.$$

We find the threshold condition for these two inequalities by setting the lower and upper bounds of $v_{\rm IN}$ the same. Simplifying, we get that

$$KR \geq \frac{2(V_{\rm S} - V_{\rm T})}{V_{\rm T}^2}.$$

We now have two conditions on KR that must both be met. For now, assume that $V_{\rm T} = 2{\rm V}$ and $V_{\rm S} = 5{\rm V}$. Therefore, we must make $KR \geq \frac{3}{2}$. We will choose $K = 2 \times 10^{-3}$ and $R = 1{\rm k}\Omega$.

We must now calculate the final branch of our voltage transfer graph, which is when both inverters are in saturation. Substituting previously derived equations, we get that

$$v_{\rm OUT} = f(v_{\rm IN}) = V_{\rm S} - \frac{KR}{2}(V_{\rm S} - \frac{KR}{2}(v_{\rm IN} - V_{\rm T})^2 - V_{\rm T})^2$$

In summary, if

$$V_H = V_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} + \frac{2}{K^2R^2} - \sqrt{\frac{4}{K^4R^4} + \frac{8V_{\rm S}}{K^3R^3}}},$$

$$v_{\rm OUT} = \begin{cases} C & v_{\rm IN} \le V_{\rm T} \\ g(v_{\rm IN}) & V_{\rm T} \le v_{\rm IN} \le V_H \\ f(v_{\rm IN}) & V_H \le v_{\rm IN} \le V_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR}} \\ V_{\rm S} & V_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR}} \le v_{\rm IN} \le V_{\rm T} + \sqrt{\frac{1}{K^2R^2} + \frac{2V_{\rm S}}{KR}} - \frac{1}{KR} \\ V_{\rm S} & V_{\rm T} + \sqrt{\frac{1}{K^2R^2} + \frac{2V_{\rm S}}{KR}} - \frac{1}{KR} \le v_{\rm IN} \end{cases}$$

C is a constant, and g is an undetermined function, since both would require the use of triode equations.

d) This is the third region in the previously calculated transfer function.

$$v_{\rm OUT} = f(v_{\rm IN}) = V_{\rm S} - \frac{KR}{2}(V_{\rm S} - \frac{KR}{2}(v_{\rm IN} - V_{\rm T})^2 - V_{\rm T})^2.$$

This holds when

$$\sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} + \frac{2}{K^2R^2} - \sqrt{\frac{4}{K^4R^4} + \frac{8V_{\rm S}}{K^3R^3}}} \le v_{\rm IN} \le v_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR}}.$$

e) Using the formulas derived in part (c), we find

$$v_{\rm OUT} = \begin{cases} C & 0 \le v_{\rm IN} \le 2 \\ g(v_{\rm IN}) & 2 \le v_{\rm IN} \le 2.43 \\ 15 - \frac{15}{2}(15 - \frac{15}{2}(v_{\rm IN} - 2)^2 - 2)^2. & 2.43 \le v_{\rm IN} \le 2.56 \\ 15 & 2.56 \le v_{\rm IN} \end{cases}$$

This is shown in Figure 7.14.

Note that the transition region of this two-stage amplifier is much narrower than that of the single-stage amplifier earlier. This is because when the second amplifier is saturated, the first amplifier is also saturated. Since $v_{\rm MID}$ is the output of the first stage, its range maps into a much smaller range of $v_{\rm IN}$ values.

ANS:: (d) $\sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} + \frac{2}{K^2R^2} - \sqrt{\frac{4}{K^4R^4} + \frac{8V_{\rm S}}{K^3R^3}}} \le v_{\rm IN} \le v_{\rm T} + \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR}}$

Problem 7.4 Consider again the two-stage amplifier shown in Figure 7.13. Suppose that the MOSFETs are characterized by the following equation in their saturation region:

$$i_{\rm DS} = \frac{K}{2} v_{\rm GS}^2$$

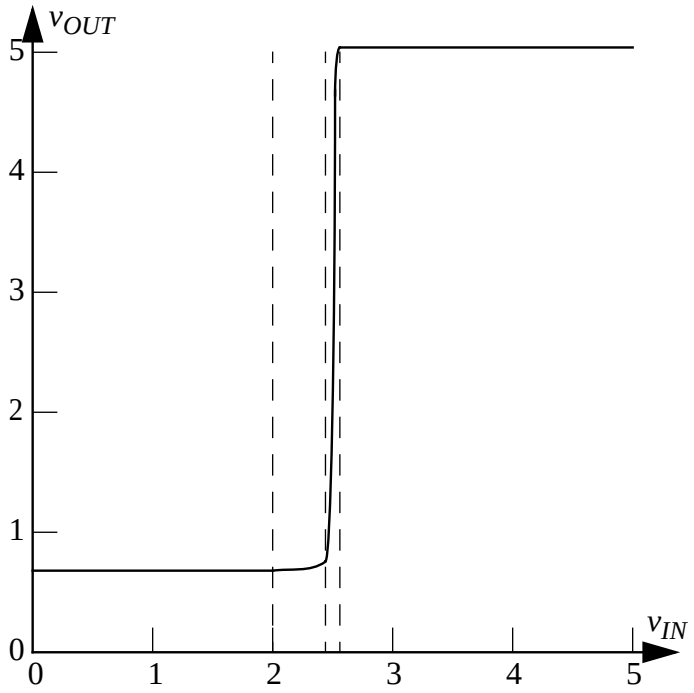


Figure 7.14:

In other words, the threshold voltage $V_{\rm T} = 0$. Furthermore, the MOSFETs operate in their saturation region when

$$v_{\rm DS} \geq v_{\rm GS} \quad \text{and} \quad v_{\rm GS} \geq 0$$

Show that there is only one input voltage for which both stages simultaneously operate under the saturation discipline. What is that input voltage?

Solution:

$$v_{\rm MID} = V_{\rm S} - \frac{KR}{2} v_{\rm IN}^2$$

$$v_{\rm OUT} = V_{\rm S} - \frac{KR}{2} v_{\rm MID}^2$$

For the saturation discipline to hold for both, the following inequalities must all be met: $v_{\rm MID} \geq v_{\rm IN}$, $v_{\rm OUT} \geq v_{\rm MID}$, $v_{\rm IN} \geq 0$, $v_{\rm MID} \geq 0$. Substituting the equations from above,

$$V_{\rm S} - \frac{KR}{2} v_{\rm MID}^2 \geq V_{\rm S} - \frac{KR}{2} v_{\rm IN}^2$$

$$v_{\rm IN}^2 \geq v_{\rm MID}^2$$

Therefore since $v_{\rm MID} \geq 0$, we find that $v_{\rm IN} \geq v_{\rm MID}$ and $v_{\rm MID} \geq v_{\rm IN}$, so $v_{\rm MID}$ must equal $v_{\rm IN}$ for both MOSFETs to both adhere to the saturation discipline. Solving the equation $v_{\rm IN} = V_{\rm S} - \frac{KR}{2} v_{\rm IN}^2$, we find that this occurs when

$$v_{\rm IN} = \frac{-1 + \sqrt{1 + 2KRV_{\rm S}}}{KR}$$

ANS:: $v_{\rm IN} = \frac{-1+\sqrt{1+2KRV_{\rm S}}}{KR}$

Problem 7.5 Consider the "source-follower" or "buffer" circuit shown in Figure 7.15. Use the SCS MOSFET model (with parameters $V_{\rm T}$ and K) to perform a large-signal analysis of this circuit according to the following steps.

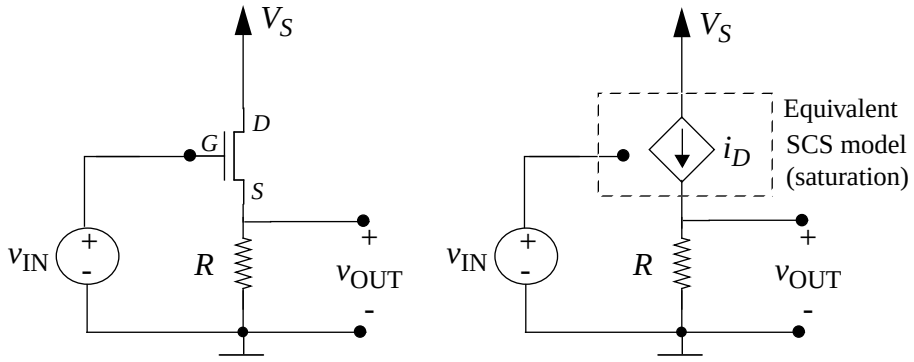


Figure 7.15:

a) Assuming that the MOSFET operates in its saturation region, show that $v_{\rm OUT}$ is related to $v_{\rm IN}$ according to

$$v_{\rm OUT} = \left[\frac{\sqrt{(2/RK) + 4(v_{\rm IN} - V_{\rm T})} - \sqrt{2/RK}}{2} \right]^2 .$$

b) Determine the range of $v_{\rm IN}$ over which the assumption of saturated MOSFET operation holds. What is the corresponding range for $v_{\rm OUT}$?

Solution:

a) By Ohm's law,

$$v_{\rm OUT} = i_{\rm D} R$$

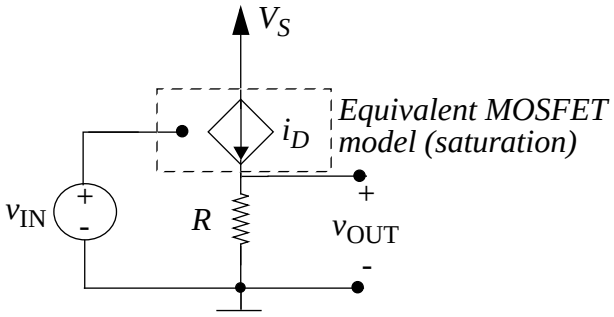


Figure 7.16:

Substitute in the formula for the current source:

$$v_{\rm OUT} = \frac{K}{2}(v_{\rm GS} - V_{\rm T})^2 R$$

Substitute for $v_{\rm GS} = v_{\rm IN} - v_{\rm OUT}$:

$$v_{\rm OUT} = \frac{RK}{2}(v_{\rm IN} - v_{\rm OUT} - V_{\rm T})^2$$

Let $v_{\rm o} = v_{\rm IN} - V_{\rm T}$ and $\alpha = \frac{2}{RK}$:

$$\alpha \cdot v_{\rm OUT} = v_{\rm o}^2 - 2v_{\rm o}v_{\rm OUT} + v_{\rm OUT}^2$$

This can be solved using the quadratic formula to obtain:

$$v_{\rm OUT} = \frac{2v_{\rm o} + \alpha \pm \sqrt{\alpha^2 + 4v_{\rm o}\alpha}}{2}.$$

This simplifies to:

$$v_{\rm OUT} = v_{\rm IN} - V_{\rm T} + \frac{1}{RK} \pm \sqrt{\left(\frac{1}{RK}\right)^2 + (v_{\rm IN} - V_{\rm T})\frac{2}{RK}}$$

We will determine which root to use in part (b).

Check the formula given in the problem by expanding it algebraically:

$$v_{\rm OUT} = \left[\frac{\sqrt{\alpha + 4v_{\rm o}} - \sqrt{\alpha}}{2}\right]^2,$$

$$v_{\rm OUT} = \frac{(\alpha + 4v_{\rm o}) - 2\sqrt{\alpha^2 + 4v_{\rm o}\alpha} + \alpha}{4},$$

$$v_{\rm OUT} = \frac{2v_{\rm o} + \alpha - \sqrt{\alpha^2 + 4v_{\rm o}\alpha}}{2}.$$

b) Two conditions must be met for the MOSFET to remain in saturation:

$$v_{\rm GS} \geq V_{\rm T} \tag{7.1}$$

$$v_{\rm DS} \geq v_{\rm GS} - V_{\rm T} \tag{7.2}$$

In addition, we require that $V_{\rm S} \geq v_{\rm OUT} \geq 0V$ and $\frac{V_{\rm S}}{R} \geq i_{\rm D} \geq 0{\rm A}$.

Condition (1) requires that $v_{\rm GS} = v_{\rm IN} - v_{\rm OUT} \geq V_{\rm T}$. The minimum value of $v_{\rm OUT}$ is 0V (i_D = 0A). Then we require that $v_{\rm IN} \geq V_{\rm T}$.

Note that condition (1) also requires that

$$v_{\rm IN} \geq v_{\rm OUT} + V_{\rm T} = v_{\rm IN} + \frac{1}{RK} \pm \sqrt{\frac{v_{\rm IN} - V_{\rm T}}{RK} + \left(\frac{1}{RK}\right)^2}$$

$$0 \geq \frac{1}{RK} \pm \sqrt{\frac{v_{\rm IN} - v_{\rm T}}{RK} + \left(\frac{1}{RK}\right)^2}$$

Thus we must take the negative root in the formula for $v_{\rm OUT}$:

$$v_{\rm OUT} = v_{\rm IN} - V_{\rm T} + \frac{1}{RK} - \sqrt{\left(\frac{1}{RK}\right)^2 + (v_{\rm IN} - v_{\rm T})\frac{2}{RK}} \tag{7.3}$$

Condition (2) requires that $v_{\rm DS} \geq v_{\rm GS} - V_{\rm T} \Rightarrow V_{\rm S} - v_{\rm OUT} \geq v_{\rm IN} - v_{\rm OUT} - V_{\rm T}$. Then we require that $V_{\rm S} + V_{\rm T} \geq v_{\rm IN}$.

To be thorough, check that this value of $v_{\rm IN}$ will not cause $v_{\rm OUT}$ to exceed $V_{\rm S}$. The maximum value of $v_{\rm OUT}$ is $V_{\rm S}$ ($i_{\rm D} = \frac{V_{\rm S}}{R}$).

$$i_{\rm D} = \frac{V_{\rm S}}{R} = \frac{K}{2}(v_{\rm GS} - V_{\rm T})^2$$

$$\Rightarrow v_{\rm IN} = V_{\rm S} + V_{\rm T} + \sqrt{V_{\rm S}\frac{2}{RK}}$$

Hence $v_{\rm OUT}$ will not exceed $V_{\rm S}$ while the MOSFET is in saturation.

ANS:: (b) $V_T \leq v_{IN} \leq V_S + V_T$

Problem 7.6 This problem studies the use of a mythical MOSFET-like device called a ZFET to construct an amplifier as shown in Figure 7.17. The ZFET operates in its saturation region when $v_{\rm GS} \geq 0$ and $v_{\rm DS} > 0$. In this region, the drain-source terminal relation is $i_{\rm DS} = K v_{\rm GS}^3$, where K is a constant having units of A/V^3. When $v_{\rm DS} = 0$, the ZFET exhibits a short circuit between its drain and source terminals, and is said to operate outside its saturation region. Similarly, the ZFET exhibits an open circuit for $v_{\rm GS} < 0$ as it again operates outside its saturation region. Finally, the gate terminal always exhibits an open circuit. These characteristics are summarized in the figure, beneath the symbol for the ZFET.

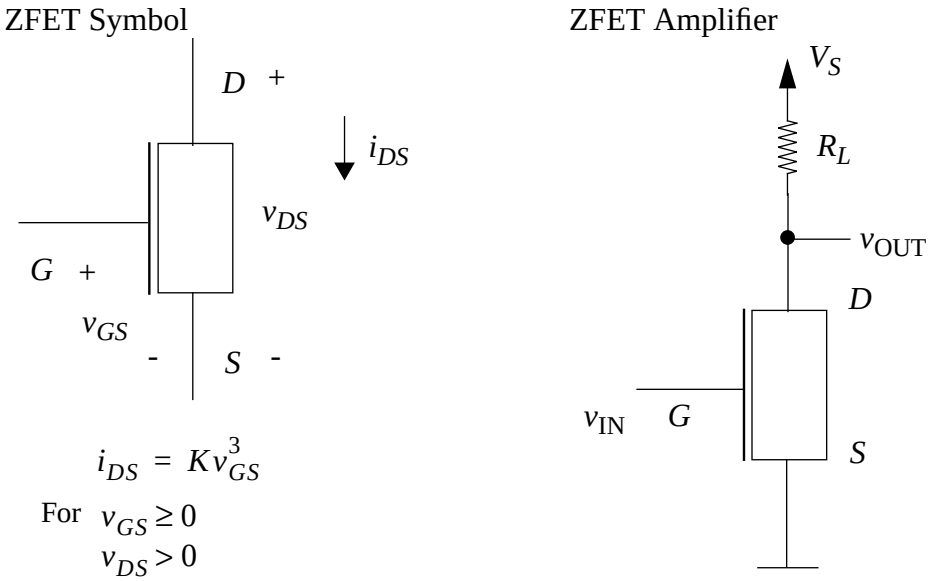

ZFET Symbol
D +
i_{DS}
v_{DS}
G +
v_{GS}
- S -
$i_{DS} = Kv_{GS}^3$
For $v_{GS} \geq 0$
$v_{DS} > 0$
ZFET Amplifier
V_S
R_L
v_{OUT}
D
v_{IN} G
S

Figure 7.17:

a) Assuming saturated operation of the ZFET, determine v_{OUT} as a function of v_{IN}.

b) Over what range of v_{IN} will the ZFET operate in its saturation region?

c) Assume that $V_{\mathrm{S}} = 10$ V, $R_{\mathrm{L}} = 1$ kΩ and $K = 0.001$ A/V^3. Sketch and clearly label v_{OUT} as a function of v_{IN} for -1 V $\leq v_{\mathrm{IN}} \leq 3$ V.

d) Given the parameters of part (c), can the amplifier can be used as an inverter that provides a valid output high voltage threshold of $V_{\mathrm{H}} = 7$ V. Why or why not? Assume that $V_{\mathrm{L}} = 2$ V.

e) Given the parameters of part (c), can the amplifier can be used as an inverter that provides a valid output high voltage threshold of $V_{\mathrm{H}} = 7$ V. Why or why not? This time around, assume that $V_{\mathrm{L}} = 1$ V.

Solution:

a) Using a single KVL equation, we get that $V_{\mathrm{S}} - v_{\mathrm{R}} - v_{\mathrm{OUT}} = 0$, where v_{R} is the voltage drop across the resistor. This is given by the current through the ZFET (since it is the same as the current through the resistor) multiplied by the resistance. Therefore, we get that

$$v_{\mathrm{OUT}} = V_{\mathrm{S}} - KRv_{\mathrm{IN}}^3$$

b) First of all, $v_{\mathrm{IN}} \geq 0$. Then, $v_{\mathrm{OUT}} < 0$, so if we substitute 0 into the previously determined formula, we get that

$$0 \leq v_{\mathrm{IN}} < \left(\frac{V_{\mathrm{S}}}{RK}\right)^{\frac{1}{3}}.$$

c) $RK = 1$. For the saturation region, $v_{\mathrm{OUT}} = 10 - v_{\mathrm{IN}}^3$. This is shown in figure 7.18.

d) No. The output that corresponds to $V_{\mathrm{L}} = 2$ is $v_{\mathrm{OUT}} = 2$, so for some values less than V_{L}, a value that is less than V_{H}, so it cannot be used as an inverter.

e) Yes. In this case, the device can be used as an inverter, since the output corresponding to $V_{\mathrm{L}} = 1$ is $v_{\mathrm{OUT}} = 9$, so for all values that are less than V_{L}, a value that is greater than V_{H} will result.

ANS:: (a) $v_{\mathrm{OUT}} = V_{\mathrm{S}} - KRv_{\mathrm{IN}}^3$ (b) $0 \leq v_{\mathrm{IN}} < \left(\frac{V_{\mathrm{S}}}{RK}\right)^{\frac{1}{3}}$ (d) no (e) yes

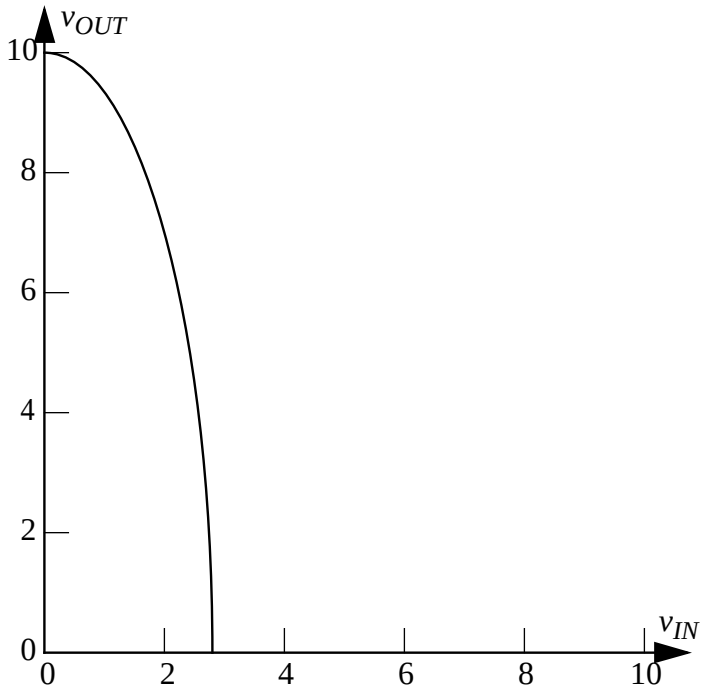


Figure 7.18:

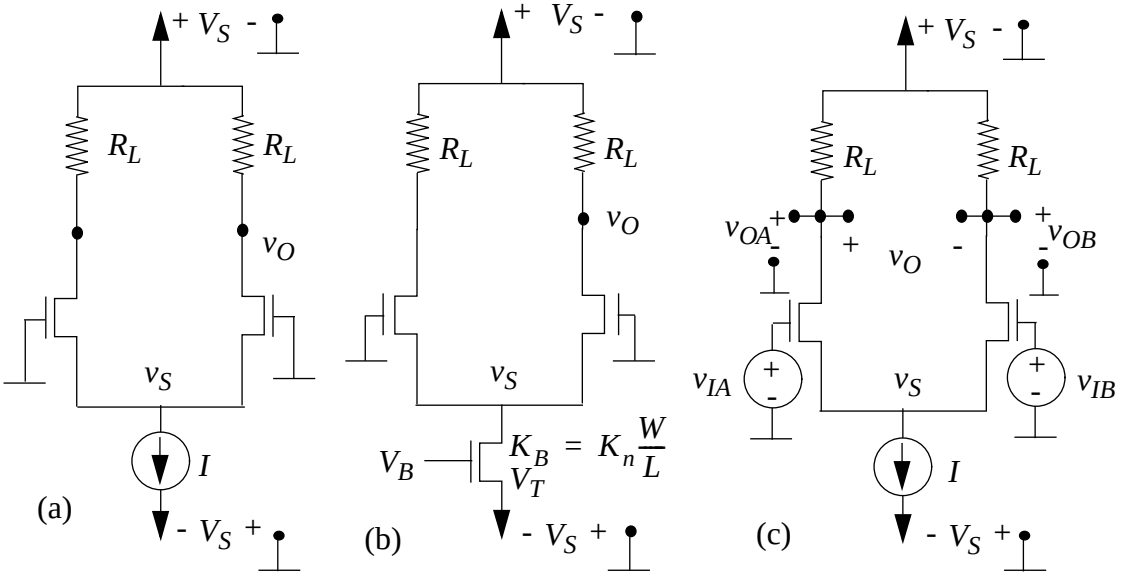


Figure 7.19:

Problem 7.7 Consider the difference amplifier circuit shown in Figure 7.19. Notice that the difference amplifier is powered by $+V_{\rm S}$ and $-V_{\rm S}$ power supplies. Assume that all MOSFETs operate under the saturation discipline, and, unless indicated otherwise, are characterized by the parameters K and V_T.

a) Determine $v_{\rm O}$ and $v_{\rm S}$ for the connection shown in Figure 7.19a. In this figure, the gates of the MOSFETs are connected to ground.

b) Consider the difference amplifier version shown in Figure 7.19b. In this figure, a MOSFET implementation of a current source replaces the abstract current source from Figure 7.19a. Determine values for $V_{\rm B}$ and W/L such that the circuit in (b) is equivalent to that in (a).

c) The difference amplifier in Figure 7.19c is driven by two input voltages $v_{\rm IA}$ and $v_{\rm IB}$ as shown. Assume that the input voltages satisfy the following constraint $v_{\rm IA} = -v_{\rm IB}$ at all times. Determine $v_{\rm OA}$, $v_{\rm OB}$, and $v_{\rm O}$ as a function of $v_{\rm IA}$.

Solution:

a) Because both FETs are identical, we know that $v_{\rm GS} = 0 - v_{\rm S}$ and $2i_{\rm D} = I = K(-v_{\rm S} - V_{\rm T})^2$. Solving for $v_{\rm S}$,

$$v_{\rm S} = \frac{-2KV_{\rm T} - \sqrt{4K^2V_{\rm T}^2 - 4K^2V_{\rm T}^2 + 4IK}}{2K}$$

Simplifying, $v_{\rm S} = -V_{\rm T} - \sqrt{\frac{I}{K}}$. $v_{\rm O}$ can be found using KVL: $v_{\rm O} = V_{\rm S} - \frac{R_{\rm L}I}{2}$.

b) The current through the new mosfet must be equal to the current of the old current source, $i_{\rm D} = \frac{K_{\rm B}}{2}(v_{\rm GS} - V_{\rm T})^2 = I$, where $K_{\rm B} = \frac{K_{\rm n}W}{2L}$. The gate to source voltage of the new MOSFET is $v_{\rm GS} = V_{\rm B} + V_{\rm S}$. Substituting and letting K be the K value associated with the transistors of part a.,

$$\frac{K_{\rm n}W}{2L}(V_{\rm B} + V_{\rm S} - V_{\rm T})^2 = K(-v_{\rm S} - V_{\rm T})^2$$

Therefore $\frac{W}{L} = \frac{2K}{K_{\rm n}}$ and $V_{\rm B} + V_{\rm S} = -v_{\rm S}$, or $V_{\rm B} = V_{\rm T} + \sqrt{\frac{I}{K}} - V_{\rm S}$.

c) Using MOSFET characteristics and KVL, $v_{\rm OA} = V_{\rm S} - \frac{KR_L}{2}(v_{\rm IA} - v_{\rm S} - V_{\rm T})^2$ and $v_{\rm OB} = V_{\rm S} - \frac{KR_L}{2}(-v_{\rm IA} - v_{\rm S} - V_{\rm T})^2$. By KVL, $v_{\rm O} = v_{\rm OA} - v_{\rm OB}$. Substituting for $v_{\rm OA}$ and $v_{\rm OB}$ using the above equations and cancelling, $v_{\rm O} = 2KR_{\rm L}v_{\rm IA}(v_{\rm S} + V_{\rm T})^2$.

ANS:: (a) $v_{\rm S} = -V_{\rm T} - \sqrt{\frac{I}{K}}$, $v_{\rm O} = V_{\rm S} - \frac{R_{\rm L}I}{2}$ (b) $\frac{W}{L} = \frac{2K}{K_{\rm n}}$, $V_{\rm B} = V_{\rm T} + \sqrt{\frac{I}{K}} - V_{\rm S}$ (c) $v_{\rm OA} = V_{\rm S} - \frac{KR_L}{2}(v_{\rm IA} - v_{\rm S} - V_{\rm T})^2$, $v_{\rm OB} = V_{\rm S} - \frac{KR_L}{2}(-v_{\rm IA} - v_{\rm S} - V_{\rm T})^2$, $v_{\rm O} = 2KR_{\rm L}v_{\rm IA}(v_{\rm S} + V_{\rm T})^2$

Problem 7.8 Consider the amplifier circuit shown in Figure 7.20. The amplifier is powered by a $+V_{\rm S}$ and a $-V_{\rm S}$ power supply.

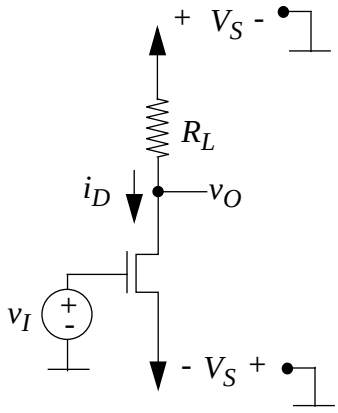


Figure 7.20:

a) Determine $v_{\rm O}$ and $i_{\rm D}$ as a function of $v_{\rm I}$ under the saturation discipline. Assume that the MOSFET parameters K and V_T are given.

b) Determine the range of valid input voltages for saturation region operation. Determine the corresponding valid range for $v_{\rm O}$ and $i_{\rm D}$.

c) Determine the output voltage when the input is grounded. In other words, for $v_{\rm I} = 0$.

d) Determine the value of $v_{\rm I}$ for which $v_{\rm I} = v_{\rm O}$ in terms of $V_{\rm S}$, $R_{\rm L}$ and the MOSFET parameters.

Solution:

a) Using a single Kirchoff voltage loop, we get that $V_{\rm S} - v_{\rm R} - v_{\rm FET} + V_{\rm S} = 0$. We can also get that $i_{\rm D} = \frac{K}{2}(v_{\rm IN} + V_{\rm S} - V_{\rm T})^2$.

Since $v_{\rm FET} = v_{\rm OUT}$ and $v_{\rm R} = i_{\rm D}R_{\rm L}$, we can substitute, to get that $v_{\rm OUT} = V_{\rm S} - \frac{RK}{2}(v_{\rm IN} + V_{\rm S} - V_{\rm T})^2$.

b) The two threshold conditions are $V_{\rm GS} \geq V_{\rm T}$ and $V_{\rm DS} \geq V_{\rm GS} - V_{\rm T}$.

For the threshold between saturation and cutoff: $v_{\rm IN} + V_{\rm S} \geq V_{\rm T}$. The MOSFET is off at this point, so $i_{\rm D} = 0$ and $v_{\rm OUT} = V_{\rm S}$.

For the threshold between saturation and triode:

$$V_{\mathrm{S}} - \frac{KR}{2}(v_{\mathrm{IN}} + V_{\mathrm{S}} - V_{\mathrm{T}})^2 \geq v_{\mathrm{IN}} + V_{\mathrm{S}} - V_{\mathrm{T}}.$$

Simplifying this, one gets that the saturation range is

$$V_{\mathrm{T}} - V_{\mathrm{S}} \leq v_{\mathrm{IN}} \leq V_{\mathrm{T}} - V_{\mathrm{S}} + \frac{\sqrt{1 + 2V_{\mathrm{S}}KR}}{KR} - \frac{1}{KR}.$$

For the upper bound, the current and output voltage can be found by substituting into the saturation equation. The current is:

$$i_{\mathrm{D}} = \frac{K}{2}\left(\frac{-1}{KR} + \frac{\sqrt{1 + 2V_{\mathrm{S}}KR}}{KR}\right)^2.$$

This can be simplified to:

$$i_{\mathrm{D}} = \frac{1}{KR^2}(1 + V_{\mathrm{S}}KR - \sqrt{1 + 2V_{\mathrm{S}}KR}).$$

The voltage can be found by finding the voltage drop across the resistor and subtracting it from the supply voltage.

$$v_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{1}{KR}(1 + V_{\mathrm{S}}KR - \sqrt{1 + 2V_{\mathrm{S}}KR}).$$

c) We must first determine which region we are in. If $V_{\mathrm{S}} \leq V\mathrm{T}$ then we are in cutoff and $v_{\mathrm{OUT}} = V_{\mathrm{S}}$. This is not very likely for our purposes, since our supply voltages are at least 3 volts usually, and MOSFET threshold voltages tend to be below 2.5 volts. (For lower supply voltages, lower threshold voltages are used too.)

However, if the following condition exists, then we are in triode:

$$V_{\mathrm{S}} - V_{\mathrm{T}} \geq \frac{\sqrt{1 + 2V_{\mathrm{S}}KR} - 1}{KR}$$

Using the values $V_{\mathrm{S}} = 5\mathrm{V}$ and $V_{\mathrm{T}} = 2\mathrm{V}$, we can find a a suitable threshold for KR. Solving the quadratic equation results in the possibilities $KR \leq 0$ (not possible) or $KR \geq \frac{4}{9}$. Therefore, if we want to be in saturation for the chosen voltages, then we have to choose $KR \leq \frac{4}{9}$.

If we are in saturation, then by substitution:

$$v_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{KR}{2}(V_{\mathrm{S}} - V_{\mathrm{T}})^2.$$

d) For this, assume that we are in saturation.

$$v_{\rm MID} = V_{\rm S} - \frac{RK}{2}(v_{\rm MID} + V_{\rm S} - V_{\rm T})^2.$$

This can be solved for $v_{\rm MID}$, resulting in:

$$v_{\rm MID} = V_{\rm T} - V_{\rm S} - \frac{1}{KR} + \frac{\sqrt{1 + 4KRV_{\rm S} - 2KRV_{\rm T}}}{KR}$$

ANS:: (a) $i_{\rm D} = \frac{K}{2}(v_{\rm IN} + V_{\rm S} - V_{\rm T})^2$, $v_{\rm OUT} = V_{\rm S} - \frac{RK}{2}(v_{\rm IN} + V_{\rm S} - V_{\rm T})^2$ (c) $v_{\rm OUT} = V_{\rm S} - \frac{KR}{2}(V_{\rm S} - V_{\rm T})^2$ (d) $v_{\rm MID} = V_{\rm T} - V_{\rm S} - \frac{1}{KR} + \frac{\sqrt{1+4KRV_{\rm S}-2KRV_{\rm T}}}{KR}$

Problem 7.9 Consider the current mirror circuit in Figure 7.21.

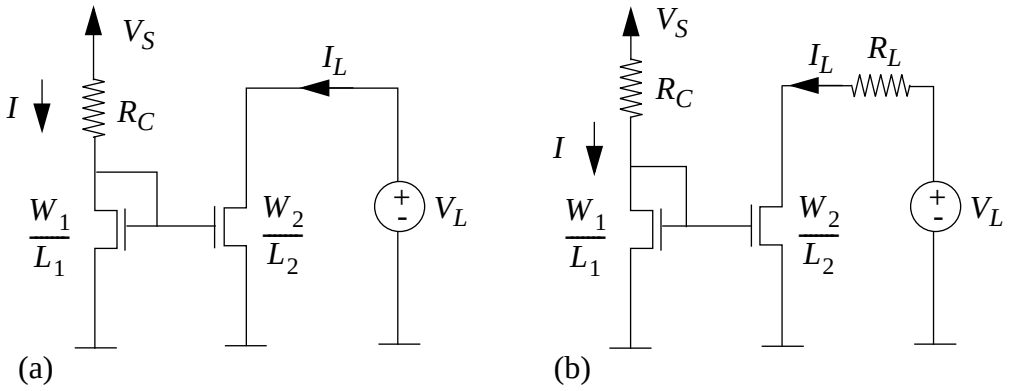


Figure 7.21:

a) Referring to Figure 7.21a, determine $I_{\rm L}$ as a function of I assuming both MOSFETs operate under the saturation discipline. Both MOSFETs have the same values for K_n and V_T. Does $I_{\rm L}$ change if $V_{\rm L}$ changes? What are the conditions under which $I_{\rm L} = I$?

b) Now consider Figure 7.21b. The current I can be increased either by increasing $V_{\rm S}$ or decreasing $R_{\rm C}$. Assuming that either $V_{\rm S}$ or $R_{\rm C}$ may be changed, and that $W_1/L_1 = W_2/L_2 = W/{\rm L}$, determine the range of values of I for which both MOSFETs operate under the saturation discipline. Assume both MOSFETs have the same values for K_n and V_T.

Solution:

a) We know that $v_{\rm GS} = V_{\rm S} - IR_{\rm C}$. Therefore, substituting appropriate parameters, $I_{\rm L} = \frac{K_{\rm n}W_2}{2L_2}(V_{\rm S} - IR_{\rm C} - V_{\rm T})^2$. The equation for $I_{\rm L}$ can not change if $V_{\rm L}$ changes as $V_{\rm L}$ is not present anywhere in the equation for $I_{\rm L}$. Logically this is so because a MOSFET's drain to source current is only dependent on its input voltage, its threshold voltage, and its geometric parameters, of which only its input voltage can be changed, and $V_{\rm L}$ can have no effect on this MOSFETs input voltage due the configuration of the circuit. As the input voltages for both MOSFETs are equivalent, $I_{\rm L}$ will equal I when $\frac{W_1}{L_1} = \frac{W_2}{L_2}$.

b) To operate under the saturation discipline, $v_{\rm GS} \geq V_{\rm T}$ and $v_{\rm DS} \geq v_{\rm GS} - V_{\rm T}$. Substituting into the first inequality from part a., $V_{\rm S} - IR_{\rm C} \geq V_{\rm T}$ or $I \leq \frac{V_{\rm S}-V_{\rm T}}{R_{\rm C}}$ for both MOSFETs. Given that for MOSFET 1 $v_{\rm GS} = v_{\rm DS}$, the second inequality always holds for that MOSFET. For MOSFET 2, $v_{\rm DS} = V_{\rm L} - I_{\rm L}R_{\rm L}$, where we know that $I = I_{\rm L}$. Substituting and solving, $I \geq \frac{V_{\rm S}-V_{\rm T}-V_{\rm L}}{R_{\rm C}-R_{\rm L}}$. Finally,

$$\frac{V_{\rm S} - V_{\rm T}}{R_{\rm C}} \geq I \geq \frac{V_{\rm S} - V_{\rm T} - V_{\rm L}}{R_{\rm C} - R_{\rm L}}$$

ANS:: (b) $\frac{V_{\rm S}-V_{\rm T}}{R_{\rm C}} \geq I \geq \frac{V_{\rm S}-V_{\rm T}-V_{\rm L}}{R_{\rm C}-R_{\rm L}}$

Problem 7.10 Consider the circuit shown in Figure 7.22. Assume that the MOSFET operates under the saturation discipline.

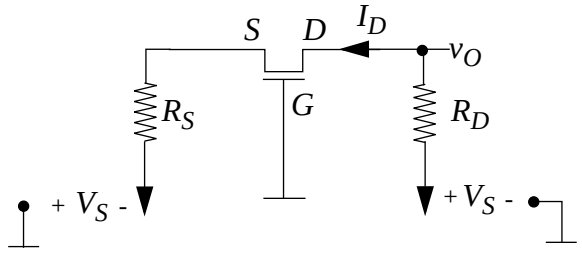


Figure 7.22:

a) Draw the SCS equivalent circuit by replacing the MOSFET by its SCS model.

b) Determine $v_{\rm O}$ and $i_{\rm D}$ in terms of $R_{\rm D}$, $R_{\rm S}$, $V_{\rm S}$, and the MOSFET parameters K and $V_{\rm T}$.

Solution:

a) See Figure 7.23.

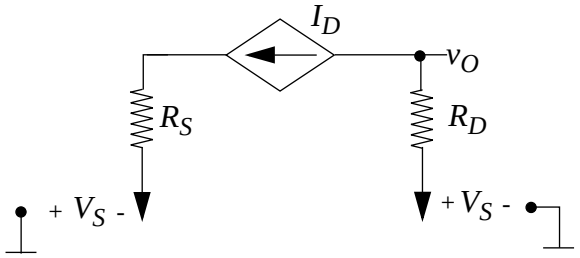


Figure 7.23:

b) By KVL, $v_{\rm GS} = V_{\rm S} - R_{\rm S} i_{\rm D}$ and $i_{\rm D} = \frac{K}{2}(V_{\rm S} - R_{\rm S} i_{\rm D} - V_{\rm T})^2$. Expanding, $0 = \frac{K}{2} R_{\rm S}^2 i_{\rm D}^2 - (K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1) i_{\rm D} + \frac{K}{2}(V_{\rm S} - V_{\rm T})^2$. From here we can solve for $i_{\rm D}$ and substitute into the equation $v_{\rm O} = V_{\rm S} - R_{\rm D} i_{\rm D}$.

$$i_{\rm D} = \frac{V_{\rm S} - V_{\rm T}}{R_{\rm S}} + \frac{1}{K R_{\rm S}^2} + \frac{\sqrt{2K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1}}{K R_{\rm S}^2}$$

$$v_{\rm O} = V_{\rm S} - \frac{R_{\rm D}}{K R_{\rm S}^2}(K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1 + \sqrt{2K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1})$$

ANS:: (b) $i_{\rm D} = \frac{V_{\rm S} - V_{\rm T}}{R_{\rm S}} + \frac{1}{K R_{\rm S}^2} + \frac{\sqrt{2K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1}}{K R_{\rm S}^2}$, $v_{\rm O} = V_{\rm S} - \frac{R_{\rm D}}{K R_{\rm S}^2}(K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1 + \sqrt{2K R_{\rm S}(V_{\rm S} - V_{\rm T}) + 1})$

Problem 7.11 Consider the "common-gate amplifier" circuit shown in Figure 7.24. Assume that the MOSFET operates under the saturation discipline.

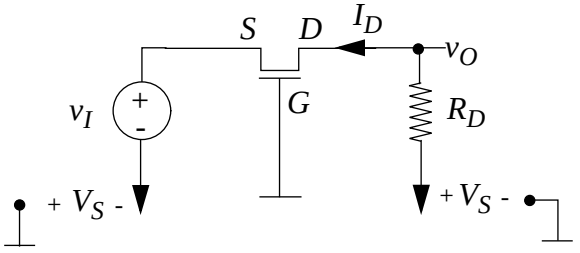


Figure 7.24:

a) Draw the SCS equivalent circuit by replacing the MOSFET by its SCS model.

b) Determine $v_{\rm O}$ and $i_{\rm D}$ in terms of $v_{\rm I}$, $R_{\rm D}$, $V_{\rm S}$, and the MOSFET parameters K and $V_{\rm T}$.

c) Determine the range of values of v_{I} for which the MOSFET operates under the saturation discipline. What is the corresponding range of v_{O}?

Solution:

a) See Figure 7.25.

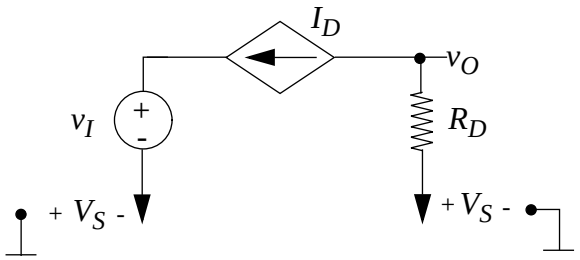


Figure 7.25:

b) There is only one relevant current, and it passes through the MOSFET, so we assume that the MOSFET is in saturation and use the relevant formula.

$$i_{\mathrm{D}} = \frac{K}{2}(V_{\mathrm{S}} - v_{\mathrm{IN}} - V_{\mathrm{T}})^2.$$

Then, using a Kirchoff voltage rule, we can find that

$$v_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{KR_2}{2}(V_{\mathrm{S}} - v_{\mathrm{IN}} - V_{\mathrm{T}})^2.$$

c) Again, we must consider the boundaries for saturation: $V_{\mathrm{GS}} \geq V_{\mathrm{T}}$ and $V_{\mathrm{DS}} \geq V_{\mathrm{GS}} - V_{\mathrm{T}}$.

For the boundary between saturation and cutoff:

$$V_{\mathrm{S}} - v_{\mathrm{IN}} \geq V_{\mathrm{T}}.$$

And for the boundary between saturation and triode:

$$V_{\mathrm{S}} - \frac{KR}{2}(-v_{\mathrm{IN}} + V_{\mathrm{S}} - V_{\mathrm{T}})^2 - v_{\mathrm{IN}} + V_{\mathrm{S}} \geq V_{\mathrm{S}} - v_{\mathrm{IN}} - V_{\mathrm{T}}.$$

These two can be simplified to get

$$V_{\rm S} - V_{\rm T} - \sqrt{\frac{2}{KR}(V_{\rm S} + V_{\rm T})} \leq v_{\rm IN} \leq V_{\rm S} - V_{\rm T}.$$

The output conditions can be found by substituting into the previously derived formula. Simplifying results in

$$-V_{\rm T} \leq v_{\rm OUT} \leq V_{\rm S}.$$

ANS:: (b) $i_{\rm D} = \frac{K}{2}(V_{\rm S} - v_{\rm IN} - V_{\rm T})^2$, $v_{\rm OUT} = V_{\rm S} - \frac{KR_D}{2}(V_{\rm S} - v_{\rm IN} - V_{\rm T})^2$ (c) $-V_{\rm T} \leq v_{\rm OUT} \leq V_{\rm S}$

Problem 7.12 Consider the MOSFET circuit shown in Figure 7.26. Determine the value of $v_{\rm O}$ in terms of the other circuit parameters. Assume the MOSFET is in saturation and is characterized by the parameters K and $V_{\rm T}$.

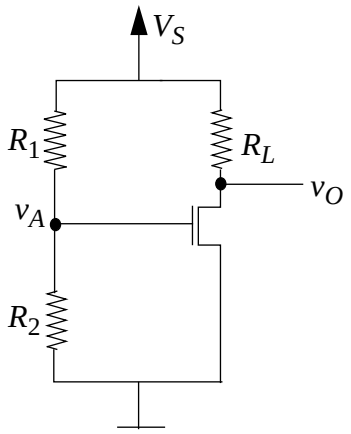


Figure 7.26:

Solution:

Due to the fact that the gate of a MOSFET has no input current, we can determine the Thevenin equivalent of the voltage divider produced by $V_{\rm S}$, R_1, and R_2 to find $v_{\rm A}$ and then substitute appropriate parameters into the KVL equation $v_{\rm O} = V_{\rm S} - R_{\rm L} i_{\rm D}$.

$$v_{\rm O} = V_{\rm S} - \frac{KR_{\rm L}}{2}(\frac{R_2 V_{\rm S}}{R_1 + R_2} - V_{\rm T})^2$$

ANS:: $v_{\rm O} = V_{\rm S} - \frac{KR_{\rm L}}{2}(\frac{R_2 V_{\rm S}}{R_1 + R_2} - V_{\rm T})^2$

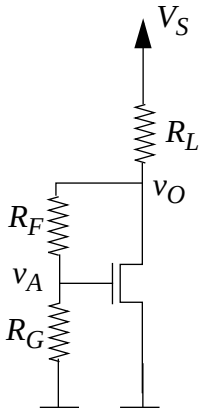


Figure 7.27:

Problem 7.13 Consider the MOSFET circuit shown in Figure 7.27. Determine the value of $v_{\rm O}$ in terms of the other circuit parameters. Assume the MOSFET is in saturation and is characterized by the parameters K and $V_{\rm T}$.

Solution:

Due to the fact that the gate of a MOSFET has no input current, we can determine the Thevenin equivalent of the voltage divider produced by $V_{\rm S}$, $R_{\rm L}$, $R_{\rm F}$ and $R_{\rm G}$ to find $v_{\rm A} = \frac{R_{\rm G}V_{\rm S}}{R_{\rm L}+R_{\rm F}+R_{\rm G}}$. If the current through $R_{\rm L}$ is $i_{\rm T}$, the current produced by the MOSFET is $i_{\rm D}$, and the current through $R_{\rm F}$ is $i_{\rm R}$, by KCL $i_{\rm T} = i_{\rm R} + i_{\rm D}$. By KVL, $V_{\rm S} - R_{\rm L}i_{\rm T} = (R_{\rm F}+R_{\rm G})i_{\rm R}$, which is equal to $v_{\rm O}$. Solving for $i_{\rm T}$ in terms of $i_{\rm R}$ and substituting into our KCL equation, we can solve for $i_{\rm R}$.

$$\frac{V_{\rm S} - (R_{\rm F}+R_{\rm G})i_{\rm R}}{R_{\rm L}} = i_{\rm R} + \frac{K}{2}\left(\frac{R_{\rm G}V_{\rm S}}{R_{\rm L}+R_{\rm F}+R_{\rm G}} - V_{\rm T}\right)^2$$

$$i_{\rm R} = \frac{V_{\rm S} - \frac{KR_{\rm L}}{2}\left(\frac{R_{\rm G}V_{\rm S}}{R_{\rm L}+R_{\rm F}+R_{\rm G}} - V_{\rm T}\right)^2}{R_{\rm L}+R_{\rm F}+R_{\rm G}}$$

Finally, because $v_{\rm O} = i_{\rm R}(R_{\rm F}+R_{\rm F})$, we find that

$$v_{\rm O} = \frac{R_{\rm F}+R_{\rm G}}{R_{\rm L}+R_{\rm F}+R_{\rm G}}\left(V_{\rm S} - \frac{KR_{\rm L}}{2}\left(\frac{R_G V_S}{R_L+R_F+R_G} - V_T\right)^2\right)$$

ANS:: $v_{\rm O} = \frac{R_{\rm F}+R_{\rm G}}{R_{\rm L}+R_{\rm F}+R_{\rm G}}\left(V_{\rm S} - \frac{KR_{\rm L}}{2}\left(\frac{R_G V_S}{R_L+R_F+R_G} - V_T\right)^2\right)$

Problem 7.14 Figure 7.28 shows a MOSFET amplifier driving a load resistor $R_{\rm E}$. The MOSFET operates in saturation and is characterized by parameters K and V_T. Determine $v_{\rm OUT}$ versus $v_{\rm IN}$ for the circuit shown.

Solution:

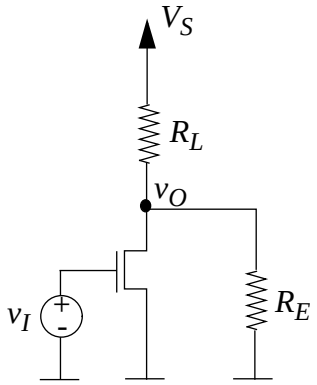


Figure 7.28:

First of all, assume that the circuit is in saturation. Call the three currents as follows: through resistor $R_{\rm L}$: I_1, through the MOSFET: I_2, and through resistor $R_{\rm E}$: I_3. All three of them point from higher voltage to lower, so therefore $I_1 = I_2 + I_3$. This is shown in Figure 7.29.

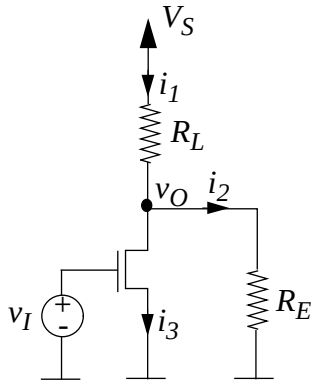


Figure 7.29:

The three currents can be determined in terms of $v_{\rm IN}$, $v_{\rm OUT}$, and MOSFET parameters:

$$v_{\rm OUT} = I_3 R_{\rm E},$$
$$V_{\rm S} - I_1 R_{\rm L} - v_{\rm OUT},$$
$$I_2 = \frac{K}{2}(v_{\rm IN} - V_{\rm T})^2.$$

Substituting this into the KCL equation and solving for $v_{\rm OUT}$, we get

$$v_{\rm OUT} = \frac{V_{\rm S} - \frac{K R_{\rm L}}{2}(v_{\rm IN} - V_{\rm T})^2}{1 + \frac{R_{\rm L}}{R_{\rm E}}} = \frac{2V_{\rm S}R_{\rm E} - K R_{\rm E} R_{\rm L}(v_{\rm IN} - V_{\rm T})^2}{2(R_{\rm L} + R_{\rm E})}.$$

However, this only applies for when the MOSFET is in saturation. We must find the range of $v_{\rm IN}$ for which this holds valid. The boundary between saturation and cutoff is merely $v_{\rm IN} \geq V_{\rm T}$. The boundary between saturation and triode can be found as follows.

$$\frac{2V_{\rm S}R_{\rm E} - R_{\rm E}R_{\rm L}K(v_{\rm IN} - V_{\rm T})^2}{2(R_{\rm L} + R_{\rm E})} \geq v_{\rm IN} - V_{\rm T}.$$

Solving this for $v_{\rm IN}$, one gets the following boundary conditions for saturation:

$$V_{\rm T} \leq v_{\rm IN} \leq V_{\rm T} - \frac{R_{\rm L} + R_{\rm E}}{KR_{\rm L}R_{\rm E}} + \sqrt{\frac{1}{K^2}\left(\frac{1}{R_{\rm L}} + \frac{1}{R_{\rm E}}\right)^2 + \frac{2V_{\rm S}}{KR_{\rm L}}}.$$

For the cutoff region, we can find the output voltage through a simple voltage divider relation, since no current flows through the MOSFET:

$$v_{\rm OUT} = V_{\rm S}\frac{R_{\rm E}}{R_{\rm E} + R_{\rm L}}.$$

The voltage transfer characteristic for triode region will not be considered for this problem.

ANS:: $v_{\rm OUT} = \frac{2V_{\rm S}R_{\rm E} - KR_{\rm E}R_{\rm L}(v_{\rm IN} - V_{\rm T})^2}{2(R_{\rm L} + R_{\rm E})}$

Problem 7.15 Determine $v_{\rm OUT}$ versus $v_{\rm IN}$ for the circuit shown in Figure 7.30. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T. What is the value of $v_{\rm OUT}$ when $v_{\rm IN} = 0$?

Solution:

Start off with the following KVL equation, where $v_{\rm RD}$, $v_{\rm FET}$, and $v_{\rm RS}$ are the voltages across $R_{\rm D}$, the MOSFET, and $R_{\rm S}$, respectively.

$$V_{\rm S} - v_{\rm RD} - v_{\rm FET} - v_{\rm RS} + V_{\rm S} = 0.$$

This is shown in Figure 7.31.

Since the voltage across a resistor is equal to the current through it times the resistance, and there is only one relevant current in the problem, we can rewrite the equation as follows:

$$2V_{\rm S} - i(R_{\rm D} + R_{\rm S}) = V_{\rm FET}.$$

Now, we must find the current. Assume that the MOSFET is in saturation - we will find the boundaries for this assumption to be valid in a bit.

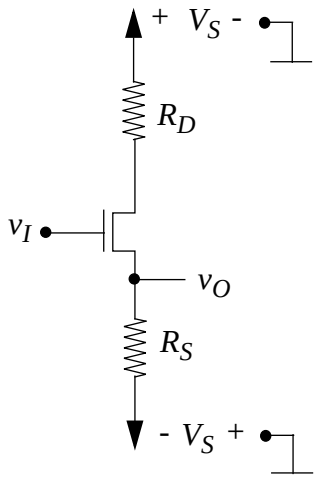


Figure 7.30:

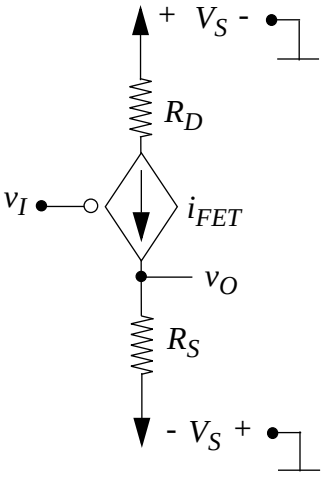


Figure 7.31:

$$i = \frac{K}{2}(v_{\mathrm{IN}} - iR_{\mathrm{S}} + V_{\mathrm{S}} - V_{\mathrm{T}})^2.$$

We solve for i to get

$$i = \frac{v_{\mathrm{IN}} + V_{\mathrm{S}} - V_{\mathrm{T}}}{R_{\mathrm{S}}} + \frac{1}{KR_{\mathrm{S}}^2} - \sqrt{\frac{2(v_{\mathrm{IN}} + V_{\mathrm{S}} - V_{\mathrm{T}})}{KR_{\mathrm{S}}^3} + \frac{1}{K^2R_{\mathrm{S}}^4}}.$$

Now, we must find the boundary conditions for the saturation region. For the boundary between saturation and cutoff, there is no current flowing through the MOSFET, so there is no voltage drop across the resistors, so we simply have

$$v_{\mathrm{I}} \geq V_{\mathrm{T}} - V_{\mathrm{S}}.$$

Now, for the boundary between saturation and triode, we have this equation.

$$v_{\mathrm{I}} + V_{\mathrm{S}} - V_{\mathrm{T}} = iR_{\mathrm{D}}.$$

Let $v_{\mathrm{X}} = v_{\mathrm{I}} + V_{\mathrm{S}} - V_{\mathrm{T}}$, and substitute in for i:

$$\frac{v_{\mathrm{X}} - 2V_{\mathrm{S}}}{R_{\mathrm{D}}} = \sqrt{\frac{2v_{\mathrm{X}}}{KR_{\mathrm{S}}^2} - \frac{1}{K^2R_{\mathrm{S}}^4}} - \frac{v_{\mathrm{X}}}{R_{\mathrm{S}}} - \frac{1}{KR_{\mathrm{S}}^2}.$$

We solve this for v_{X} since that is in terms of v_{I} and constants.

$$V_{\mathrm{X}} = \frac{\frac{2V_{\mathrm{S}}}{R_{\mathrm{D}}} + \frac{2V_{\mathrm{S}}}{R_{\mathrm{S}}R_{\mathrm{D}}} - \frac{1}{KR_{\mathrm{D}}R_{\mathrm{S}}^2} - \sqrt{\frac{1}{K^2R_{\mathrm{S}}^4R_{\mathrm{D}}^2} + \frac{4V_{\mathrm{S}}}{KR_{\mathrm{S}}^3R_{\mathrm{D}}^2} + \frac{4V_{\mathrm{S}}}{KR_{\mathrm{S}}^4R_{\mathrm{D}}}}}{\left(\frac{1}{R_{\mathrm{D}}} + \frac{1}{R_{\mathrm{S}}}\right)^2}$$

Now, solve for V_{IN}, and find the boundaries of the saturation region:

$$V_{\mathrm{T}} - V_{\mathrm{S}} \leq V_{\mathrm{I}}$$

$$V_{\mathrm{I}} \leq V_{\mathrm{T}} - V_{\mathrm{S}} + \frac{2V_{\mathrm{S}}R_{\mathrm{S}}^2 + 2V_{\mathrm{S}}R_{\mathrm{S}}R_{\mathrm{D}} - \frac{R_{\mathrm{D}}}{K} - \sqrt{\frac{R_{\mathrm{D}}^2}{K^2} + \frac{4V_{\mathrm{S}}R_{\mathrm{S}}R_{\mathrm{D}}^2}{K} + \frac{4V_{\mathrm{S}}R_{\mathrm{D}}^3}{K}}}{(R_{\mathrm{D}} + R_{\mathrm{S}})^2}$$

Now, to actually find v_{OUT}. Using a KVL equation, we can find that $v_{\mathrm{OUT}} = iR_{\mathrm{S}} - V_{\mathrm{S}}$. In cutoff, $v_{\mathrm{OUT}} = -V_{\mathrm{S}}$ since there is no current through the resistors. In saturation,

$$v_{\rm OUT} = v_{\rm IN} - V_{\rm T} + \frac{1}{KR_{\rm S}} - \sqrt{\frac{2(v_{\rm IN} + V_{\rm S} - V_{\rm T})}{KR_{\rm S}} + \frac{1}{K^2R_{\rm S}^2}}$$

When there is an input voltage of zero, the system could be in cutoff, saturation, or triode. For typical values of $V_{\rm S}$ and $V_{\rm T}$, the device will not be in cutoff. But if it were, the output voltage would be $-V_{\rm S}$.

For values of $V_{\rm S} = 5$V, and $V_{\rm T} = 2$V, we can find a relation between $R_{\rm S}$, $R_{\rm D}$, and K that allows the device to avoid the triode region.

If we substitute into the boundary condition, we get this relation:

$$3 \leq \frac{10R_{\rm S}}{R_{\rm S} + R_{\rm D}} - \frac{1}{(R_{\rm S} + R_{\rm D})^2}\left(\frac{R_{\rm S}}{K} - R_{\rm D}\sqrt{\frac{1}{K^2} + \frac{40}{K}(R_{\rm S} + R_{\rm D})}\right).$$

Further analysis is optional - we can assume that the device is in saturation for $V_{\rm IN} = 0$. If this is the case, then

$$v_{\rm OUT} = -V_{\rm T} + \frac{1}{KR_{\rm S}} - \sqrt{\frac{2(V_{\rm S} - V_{\rm T})}{KR_{\rm S}} + \frac{1}{K^2R_{\rm S}^2}}.$$

ANS:: $v_{\rm OUT} = v_{\rm IN} - V_{\rm T} + \frac{1}{KR_{\rm S}} - \sqrt{\frac{2(v_{\rm IN}+V_{\rm S}-V_{\rm T})}{KR_{\rm S}} + \frac{1}{K^2R_{\rm S}^2}}$

Problem 7.16 Determine $v_{\rm O}$ versus $v_{\rm I}$ for the circuit shown in Figure 7.32. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T. What is the value of $v_{\rm O}$ when $v_{\rm I} = 0$?

Solution:

Most of the work has already been done in the previous problem. The boundaries for cutoff, saturation, and triode remain the same, as does the current. All that changes is the output voltage.

Using a KVL equation, we find that $v_{\rm OUT} = V_{\rm S} - iR_{\rm D}$. This is shown in Figure 7.33.

In cutoff, $v_{\rm OUT} = V_{\rm S}$. In saturation, we get that

$$v_{\rm OUT} = V_{\rm S} - \frac{R_{\rm D}}{R_{\rm S}}(v_{\rm IN} - V_{\rm T} + V_{\rm S}) + \frac{R_{\rm D}}{KR_{\rm S}^2} - \sqrt{\frac{2R_{\rm D}^2(v_{\rm IN} + V_{\rm S} - V_{\rm T})}{KR_{\rm S}^3} + \frac{R_{\rm D}^2}{K^2R_{\rm S}^4}}.$$

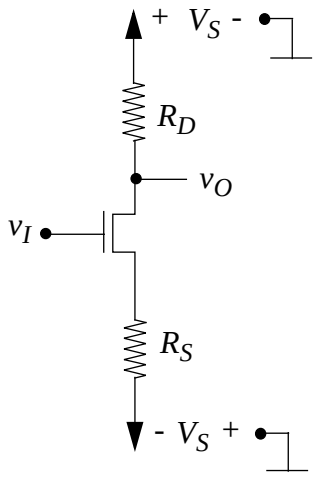


Figure 7.32:

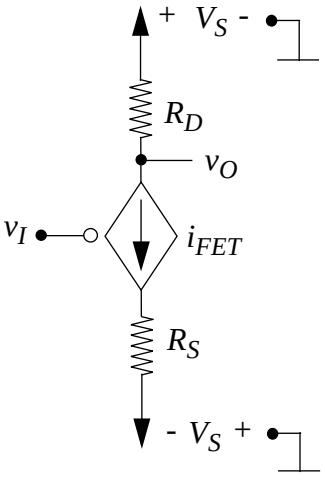


Figure 7.33:

For an input voltage of zero, we will assume that the system is in saturation since the cutoff calculation is simply the rail voltage $v_{\rm OUT} = V_{\rm S}$, and the triode calculations are unnecessarily terrible. In saturation,

$$v_{\rm OUT} = V_{\rm S} - \frac{R_{\rm D}}{R_{\rm S}}(-V_{\rm T} + V_{\rm S}) + \frac{R_{\rm D}}{KR_{\rm S}^2} - \sqrt{\frac{2R_{\rm D}^2(V_{\rm S} - V_{\rm T})}{KR_{\rm S}^3} + \frac{R_{\rm D}^2}{K^2R_{\rm S}^4}}.$$

ANS:: $v_{\rm OUT} = V_{\rm S} - \frac{R_{\rm D}}{R_{\rm S}}(-V_{\rm T} + V_{\rm S}) + \frac{R_{\rm D}}{KR_{\rm S}^2} - \sqrt{\frac{2R_{\rm D}^2(V_{\rm S} - V_{\rm T})}{KR_{\rm S}^3} + \frac{R_{\rm D}^2}{K^2R_{\rm S}^4}}$

Problem 7.17 Determine $v_{\rm O}$ versus $v_{\rm I}$ for the circuit shown in Figure 7.34. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T.

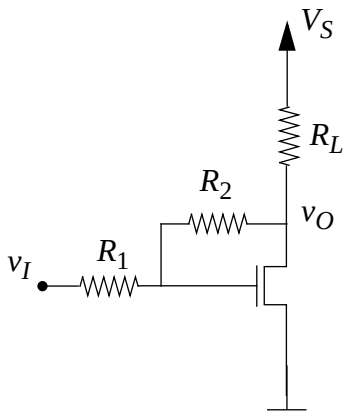


Figure 7.34:

Solution:

First of all, define $v_{\rm G}$ to be the gate voltage. Also, define three currents i_1, i_2, and i_3 to be the currents flowing through $R_{\rm L}$, R_2, and the MOSFET, respectively. Define i_3 to be flowing towards ground, and let $i_1 + i_2 = i3$. This is shown in Figure 7.35.

The gate voltage can be found through a voltage divider rule since no current flows from between R_1 and R_2 to the gate.

$$v_{\rm G} = \frac{R_2}{R_1 + R_2}v_{\rm IN} + \frac{R_1}{R_1 + R_2}v_{\rm OUT}$$

In cutoff, the output voltage and the input voltage are related by a voltage divider rule:

$$v_{\rm OUT} = \frac{V_{\rm S}(R_1 + R_2) + V_{\rm IN}R_{\rm L}}{R_1 + R_2 + R_{\rm L}}$$

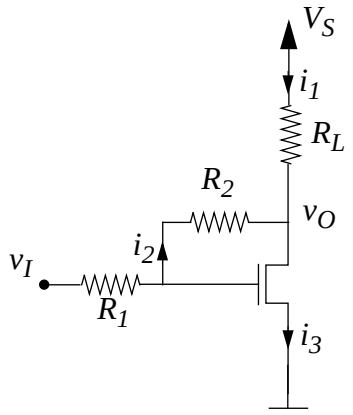


Figure 7.35:

In saturation, we have an extra current to worry about. We substitute into our original KCL equation to get

$$\frac{V_{\rm S} - v_{\rm OUT}}{R_{\rm L}} + \frac{v_{\rm IN} - v_{\rm OUT}}{R_{\rm L}} = \frac{K}{2}\left(\frac{R_2}{R_1+R_2}v_{\rm IN} + \frac{R_1}{R_1+R_2}v_{\rm OUT} - V_{\rm T}\right)^2$$

We can solve this for $v_{\rm OUT}$, but it ends up being quite monstrous. Let $R_{\rm T} = R_1 + R_2$.

$$v_{\rm OUT} = \frac{R_2 R_{\rm T} V_{\rm T}}{R_1^2} - \frac{R_2 v_{\rm IN}}{R_1} - \frac{R_{\rm T}^2}{K R_{\rm L} R_1} - \frac{R_{\rm T}}{K R_1^2} + \frac{\sqrt{L+M+N}}{2K R_{\rm L} R_1},$$

with the following subexpressions:

$$L = R_{\rm T}^2 (R_{\rm T} + R_{\rm L})^2,$$

$$M = K^2 R_{\rm L}^2 R_{\rm T}^2 V_{\rm T} (R_1 - R_2)(2 v_{\rm IN} R_1 - V_{\rm T} R_{\rm T}),$$

$$N = 2K(V_{\rm S} R_{\rm L} R_1^2 R_{\rm T}^2 - V_{\rm T} R_1 R_2 R_{\rm T}^2 (R_1 + R_2 + R_{\rm L}) + v_{\rm IN} R_{\rm L} R_1 R_{\rm T}^2 (R_{\rm L} + R_2)).$$

The boundaries for which the device is in saturation can be found by evaluating $v_{\rm G} \geq V_{\rm T}$ and $v_{\rm OUT} \geq v_{\rm G} - v_{\rm T}$. This evaluation is even more complicated than the previous equation, since $v_{\rm G}$ is given in terms of $v_{\rm OUT}$, and needs to be put in terms of $v_{\rm IN}$. In terms of both $v_{\rm IN}$ and $v_{\rm OUT}$, the boundary conditions are derived much more easily.

Between saturation and cutoff:

$$\frac{R_2}{R_1+R_2}v_{\rm IN}+\frac{R_1}{R_1+R_2}v_{\rm OUT}\geq V_{\rm T}$$

Between saturation and triode:

$$v_{\rm OUT}\geq v_{\rm IN}-\frac{R_1+R_2}{R_2}v_{\rm T}$$

Problem 7.18 Consider the BJT circuit called the "common-collector amplifier" shown in Figure 7.36. This BJT amplifier configuration is also called the source follower circuit. For this problem, use the piecewise linear BJT model from Exercise 7.8. Assume that the BJT operates in its active region.

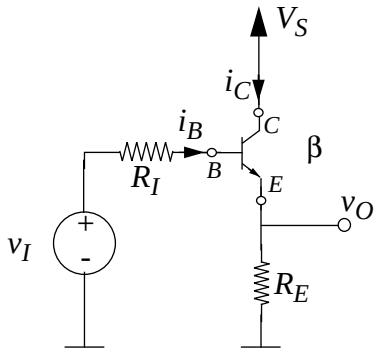


Figure 7.36:

a) Draw the active-region equivalent circuit of the BJT source follower by replacing the BJT by its piecewise linear model.

b) Assuming active region operation, determine v_O in terms of v_I, R_I, R_E and the BJT parameter β.

c) What is the value of v_O when $\beta R_E >> R_I$?

d) Compute the value of v_O given that $v_I = 3V$, $R_I = 10k$, $R_E = 100k$, $\beta = 100$, and $V_S = 10V$.

e) Determine the range of values of v_I for which the BJT operates in its active region for the parameter values given in (d). What is the corresponding range of v_O?

Solution:

a)

b)

$$\begin{aligned} v_O &= i_E R_E \\ &= i_B(\beta+1)R_E \\ &= \frac{v_I-(v_O+0.6)}{R_I}(\beta+1)R_E \\ &= (v_I - v_O - 0.6)(\beta+1)\frac{R_E}{R_I} \\ &= \frac{v_I-0.6}{1+\frac{R_I}{(\beta+1)R_E}} \end{aligned}$$

c) When $\beta R_E >> R_I$,

$$v_O \approx v_I - 0.6$$

d) Substituting into

$$v_O = \frac{v_I - 0.6}{1+\frac{R_I}{(\beta+1)R_E}}$$

we have

$$v_O = \frac{3-0.6}{1+\frac{10k}{(100+1)100k}}$$

Or,

$$v_O \approx 2.4V$$

e) At the low end, $v_I > 0.6$, so that the BJT is not in cutoff.

At the high end, v_I must not be too large, or else the BJT will enter saturation. The BJT enters saturation when

$$v_{BE} = v_{CE} + 0.4$$

Or, substituting for v_{BE} and v_{CE}

$$0.6 = V_S - v_O + 0.4$$

In other words, when

$$V_S - v_O = 0.2$$

We know

$$v_O = v_I - 0.6$$

Therefore, we need to solve for v_I from

$$V_S - v_I - 0.6 = 0.2$$

Or,

$$v_I = 9.2V$$

Thus the constraints on v_I for active region operation are

$$0.6 < v_I < 9.2V$$

The corresponding constraints on v_O are

$$0 < v_O < 8.6V$$

ANS:: (b) $v_O = \frac{v_I - 0.6}{1 + R_I/((\beta+1)R_E)}$ (c) $v_O = v_I - 0.6$ (d) $v_O = 2.4V$ (e) $0.6 < v_I < 9.2V$ and $0 < v_O < 8.6V$

Problem 7.19 Consider the compound three terminal device formed by connecting two BJTs in the configuration shown in Figure 7.37. The three terminals are labeled C', B' and E'. The two BJTs are identical, each with $\beta = 100$. Assume that each of the BJTs operates in the active region.

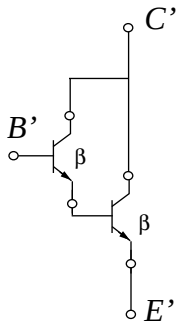


Figure 7.37:

a) Draw the active-region equivalent circuit of the compound BJT by replacing each of the BJTs by the piecewise linear model shown in Exercise 7.8. Clearly label the C', B' and E' terminals.

b) In the configuration shown, the compound device behaves like a BJT. Determine the value of the current gain β' for this compound BJT.

c) When the base current $i_{B'} > 0$, determine the voltage between the B' and E' terminals.

Solution:

a)

b) The current gain of the new device is given by

$$\beta' = (\beta + 2)\beta$$

c) When the base current $i_{B'} > 0$, both transistors are in their active region. In this situation, the voltage between the B' and E' terminals is 1.2V.

ANS:: (b) $\beta' = (\beta + 2)\beta$ (c) 1.2V

Chapter 8

The Small Signal Model

Exercises

Exercise 8.1 Consider the amplifier shown in Figure 8.1. The MOSFET operates in its saturation region and is characterized by the parameters V_T and K. The input voltage v_I comprises the sum of a DC bias voltage V_I and a sinusoid of the form $v_i = A\sin\omega t$. Assume that A is very small compared to V_I. Let the output voltage v_O comprise a DC bias term V_O and a small-signal response term v_o.

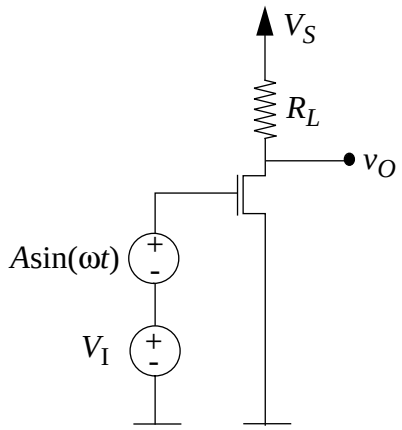


Figure 8.1:

a) Determine the output operating point voltage V_O for the input bias of V_I.

b) Determine the small signal gain of the amplifier.

c) Draw the form of the input and output voltages as a function of time, clearly showing the DC and time-varying small-signal components.

Solution:

a) $V_O = V_S - \frac{KR_L}{2}(V_I - V_T)^2$

b) small signal gain = $\frac{dv_O}{dv_I}|_{v_I=V_I} = -KR_L(V_I - V_T)$

c) See Figure 8.2.

ANS:: (a) $V_O = V_S - \frac{KR_L}{2}(V_I - V_T)^2$ (b) $\frac{dv_O}{dv_I}|_{v_I=V_I} = -KR_L(V_I - V_T)$

Exercise 8.2 Develop the small signal model for a two-terminal device formed by a MOSFET with its gate tied to its drain, operating under the saturation discipline, with parameters V_T and K.

Solution:

$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$

$i_{DS} = \frac{K}{2}(v_{DS} - V_T)^2$

$\frac{di_{DS}}{dv_{DS}}|_{v_{DS}=V_{DS}} = K(V_{DS} - V_T)$

The small signal model is resistor $r_{ds} = \frac{1}{K(V_{DS}-V_T)}$.

ANS:: resistor $r_{ds} = \frac{1}{K(V_{DS}-V_T)}$

Exercise 8.3 Develop the small signal model for a two-terminal device formed between the drain and source terminals of a MOSFET with a 2 volt DC source connected between its gate and source terminals ($V_{GS} = 2V$). Assume the MOSFET operates under the saturation discipline. Assume further that $V_T = 1$ volt for the MOSFET.

Solution:

$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$

$i_{DS} = \frac{K}{2}(2 - 1)^2 = \frac{K}{2}$

In other words, the two-terminal device formed between the drain and source terminals of the MOSFET is a current source with current $(K/2)$. Thus, the small signal model of the two-terminal device is an open circuit.

ANS:: Current source $i_{DS} = \frac{K}{2}$, so that the small signal model is an open circuit

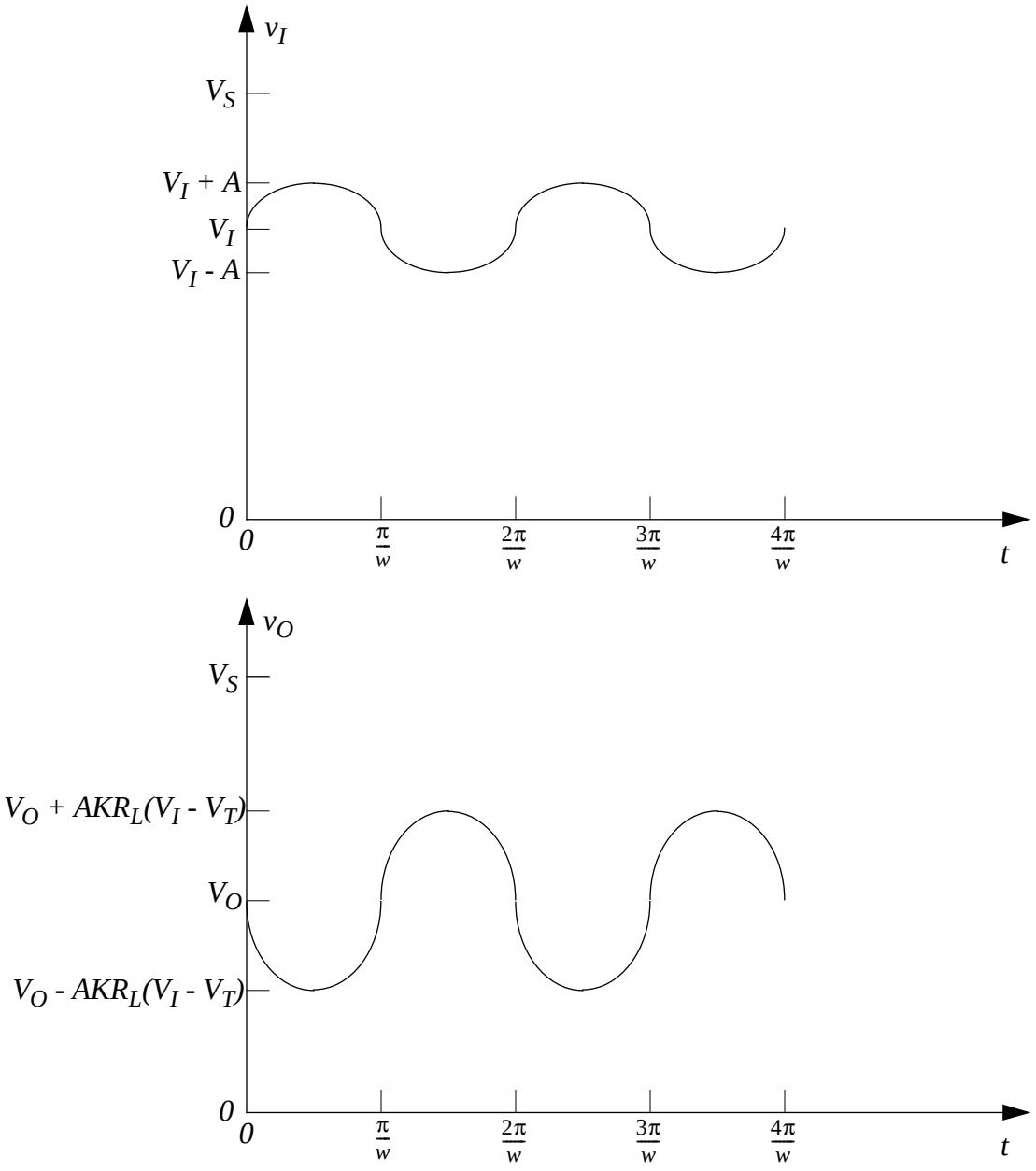

v_I
V_S
$V_I + A$
V_I
$V_I - A$
0
0
$\frac{\pi}{w}$
$\frac{2\pi}{w}$
$\frac{3\pi}{w}$
$\frac{4\pi}{w}$
t
v_O
V_S
$V_O + AKR_L(V_I - V_T)$
V_O
$V_O - AKR_L(V_I - V_T)$
0
0
$\frac{\pi}{w}$
$\frac{2\pi}{w}$
$\frac{3\pi}{w}$
$\frac{4\pi}{w}$
t

Figure 8.2:

Exercise 8.4 Consider the MOSFET amplifier shown in Figure 8.3. Assume that the amplifier is operated under the saturation discipline. In its saturation region, the MOSFET is characterized by the equation

$$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$$

where i_{DS} is the drain-to-source current when a voltage v_{GS} is applied across its gate-to-source terminals.

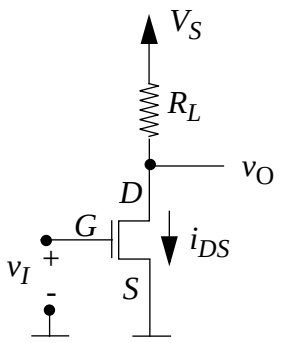


Figure 8.3:

a) Write an expression relating v_O to v_I. What is its operating point output voltage V_O, given an input operating point voltage of V_I? What is the corresponding operating point current I_{DS}?

b) Assuming an operating point input voltage of V_I, derive the expression relating the small signal output voltage v_o to the small signal input v_i from the relationship between v_O and v_I. What is the small signal gain of the amplifier at the input operating point of V_I?

c) Draw the small signal equivalent circuit for the amplifier based on the SCS model of the MOSFET assuming the operating point input voltage is V_I.

d) Derive an expression for the small signal gain of the amplifier from the small signal equivalent circuit. Verify that the gain computed from the small signal equivalent circuit is identical to the gain computed in part (b).

e) By what factor must R_L change to double the small signal gain of the amplifier? What is the corresponding change in the output bias voltage?

f) By what factor must V_I change to double the small signal gain of the amplifier? What is the corresponding change in the output bias voltage?

Solution:

a) $v_O = V_S - \frac{KR_L}{2}(v_I - V_T)^2$
$V_O = V_S - \frac{KR_L}{2}(V_I - V_T)^2$
$I_{DS} = \frac{K}{2}(V_I - V_T)^2$

b) $\frac{dv_O}{dv_I}|_{v_I=V_I} = -KR_L(V_I - V_T)$
$v_o = -KR_L(V_I - V_T)v_i$
The small signal gain is $\frac{v_o}{v_i} = -KR_L(V_I - V_T)$.

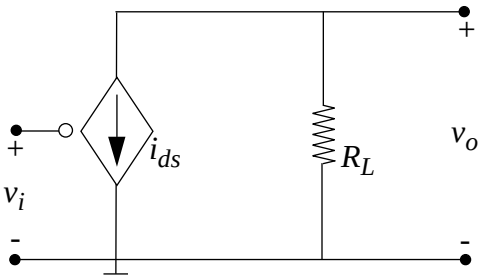


Figure 8.4:

c) See Figure 8.4.

d) $v_o = -i_{ds}R = -KR_L(V_I - V_T)v_i$
$\frac{v_o}{v_i} = -KR_L(V_I - V_T)$

e) To double the small signal gain, R_L must double. This will decrease V_O by $\frac{KR_L}{2}(V_I - V_T)^2$

f) $2(V_I - V_T) = (XV_I - V_T)$
$2V_I - 2V_T = (XV_I - V_T)$
To double the small signal gain, scale V_I by $X = \frac{2V_I - V_T}{V_I}$
The output bias will decrease by $\frac{3}{2}KR_L(V_I - V_T)^2$ to $V_S - 2KR_L(V_I - V_I)^2$

ANS:: (a) $V_O = V_S - \frac{KR_L}{2}(V_I - V_T)^2$, $I_{DS} = \frac{K}{2}(V_I - V_T)^2$ (b) $v_o = -KR_L(V_I - V_T)v_i$, $\frac{v_o}{v_i} = -KR_L(V_I - V_T)$ (d) $\frac{v_o}{v_i} = -KR_L(V_I - V_T)$ (e) R_L doubles (f) scale factor: $X = \frac{2V_I - V_T}{V_I}$

Exercise 8.5 Consider again the MOSFET amplifier shown in Figure 8.3. Assume as before that the MOSFET is operated under the saturation discipline, and that its parameters are V_T and K.

a) What is the range of valid input voltages for the amplifier? What is the corresponding range of valid output voltages?

b) Assuming we desire to use voltages of the form $A \sin \omega t$ as AC inputs to the amplifier, determine the input bias point V_I for the amplifier which will allow maximum input swing under the saturation discipline. What is the corresponding output bias point voltage V_O?

c) What is the largest value of A that will allow saturation region operation for the bias point determined in (b)?

d) What is the small signal gain of the amplifier for the bias point determined in (b)?

e) Suppose A is small compared to V_I. Write an expression for the small signal output voltage v_o for the bias point determined in (b).

Solution:

a) $v_{GS} \geq V_T$

$v_{GS} - V_T \leq v_{DS}$

$v_I - V_T \leq V_S - \frac{KR_L}{2}(v_I - V_T)^2$

$V_T \leq v_I \leq V_T + \frac{\sqrt{1+2KR_LV_S}-1}{KR_L}$

$v_O = V_S - \frac{KR_L}{2}(v_I - V_T)^2$

$\frac{\sqrt{1+2KR_LV_S}-1}{KR_L} \leq v_O \leq V_S$

b) To maximize input swing, pick V_I in the center of the range of valid input voltages.

$V_I = V_T + \frac{\sqrt{1+2KR_LV_S}-1}{2KR_L}$

$V_O = \frac{3KR_LV_S+\sqrt{1+2KR_LV_S}-1}{4KR_L}$

c) $A \leq \frac{\sqrt{1+2KR_LV_S}-1}{2KR_L}$

d) $\frac{v_o}{v_i} = -KR_L(V_I - V_T)$

$\frac{v_o}{v_i} = \frac{1-\sqrt{1+2KR_LV_S}}{2}$

e) $v_o = \frac{A}{2}(1 - \sqrt{1 + 2KR_LV_S}) \sin(\omega t)$

ANS:: (a) $v_I - V_T \leq V_S - \frac{KR_L}{2}(v_I - V_T)^2$, $\frac{\sqrt{1+2KR_LV_S}-1}{KR_L} \leq v_O \leq V_S$ (b) $V_I = V_T + \frac{\sqrt{1+2KR_LV_S}-1}{2KR_L}$, $V_O = \frac{3KR_LV_S+\sqrt{1+2KR_LV_S}-1}{4KR_L}$ (c) $\frac{\sqrt{1+2KR_LV_S}-1}{2KR_L}$ (d) $\frac{1-\sqrt{1+2KR_LV_S}}{2}$ (e) $v_o = \frac{A}{2}(1 - \sqrt{1 + 2KR_LV_S}) \sin(\omega t)$

Exercise 8.6 Consider once more the MOSFET amplifier shown in Figure 8.3. Assume as before that the amplifier is operated under the saturation discipline, and that its parameters are V_T and K.

a) Using the small signal circuit model of the amplifier, and assuming an input bias voltage V_I, determine the small-signal output resistance of the amplifier. That is, determine the equivalent resistance of the amplifier at the output port of its small-signal model with $v_{\rm i} \equiv 0$.

b) Develop a Thévenin equivalent model for the small signal amplifier as observed at its output port.

c) What is its input resistance? That is, determine the equivalent resistance of the amplifier at the input port of its small-signal model.

Solution:

a) $r_{output} = R_L$

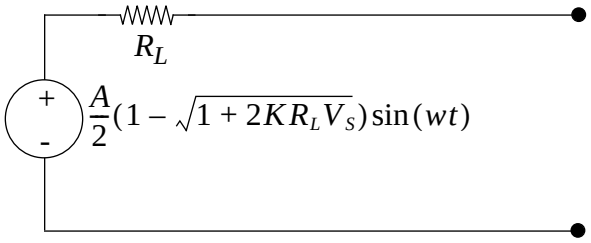


Figure 8.5:

b) See Figure 8.5.

$r_{th} = R_L$

$v_{oc} = \frac{A}{2}(1 - \sqrt{1 + 2KR_LV_S})\sin(\omega t)$

c) $r_{input} = \infty$

ANS:: (a) $r_{output} = R_L$ (b) $r_{th} = R_L$, $v_{oc} = \frac{A}{2}(1 - \sqrt{1 + 2KR_LV_S})\sin(\omega t)$ (c) $r_{input} = \infty$

Exercise 8.7 Consider the common emitter BJT amplifier shown in Figure 8.6. The input voltage v_I comprises the sum of a DC bias voltage $V_I = 0.7V$ and a sinusoid of the form $v_i = A\sin\omega t$, where $A = 0.001$V. For the values shown, you may assume that A is very

small compared to V_I. You may further assume that the BJT always operates in its active region. Figure 8.7 shows a small signal model for the BJT operating in its active region. Let the output voltage v_O comprise a DC bias term V_O and a small-signal response term v_o.

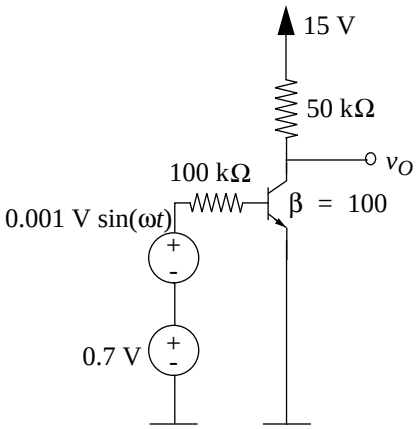
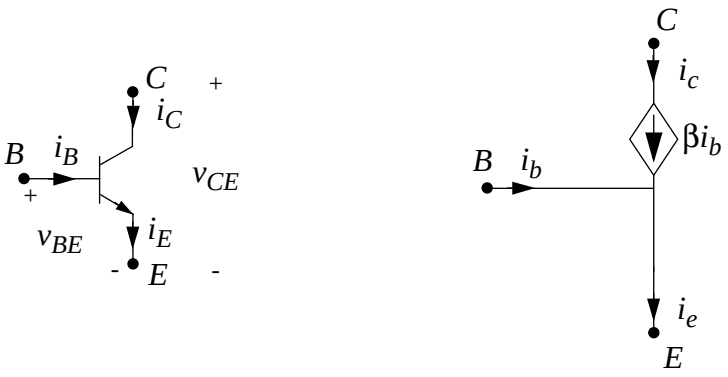


Figure 8.6:



(a) BJT

(b) BJT small signal model

Figure 8.7:

a) Determine the output operating point voltage V_O for the input bias of $V_I = 0.7$V.

b) Draw the small signal equivalent circuit for the amplifier.

c) Determine the small signal gain of the amplifier.

d) What is the value of v_o, the small signal component of the output, given the small signal input shown in Figure 8.6.

e) Determine the small signal input and output resistances of the amplifier.

f) Determine the small signal current and power gain of the amplifier, assuming that the amplifier drives a load $R_O = 50k$ that is connected between the output node and ground.

Solution:

a) We determine the operating point using a large signal analysis of the BJT amplifier. Since a specific large-signal model of the BJT is not suggested, we will go ahead and use the large-signal model of the BJT (in its active region) suggested in the text book. (The text book gives an example of an operating point calculation for a BJT amplifier in the large-signal amplifier chapter.)

The relation between V_O and V_I can now be derived as

$$V_O = V_S - \beta R_L \frac{V_I - 0.6}{R_I}$$

(The above formula is also derived in the text book in one of the BJT examples in the large signal amplifier chapter).

Substituting known values

$$V_O = 10V$$

b)

c) Load R_L is 50k.

$$v_o = -\frac{v_i}{R_I}\beta R_L$$

Or

$$\frac{v_o}{v_i} = -50$$

d)

$$v_o = -50 \times 0.001 \sin \omega t$$

Or

$$v_o = -0.05 \sin \omega t$$

e)

$$r_i = R_I = 100k$$

$$r_o = R_L = 50k$$

f) Load is now $R_L = 50k$ in parallel with $R_O = 50k$.

A current i_b at the input results in a current

$$i_c = \beta i_b$$

through the collector terminal. This current divides between R_L and R_O according to the current divider relation. The current gain is given by the ratio of i_b and the current through R_O. We must also add on a minus sign since the direction of i_o is opposite to that of i_c. Thus the current gain is given by

$$\frac{i_o}{i_b} = -\beta R_L/(R_L + R_O)$$

For the parameter values given

$$\frac{i_o}{i_b} = -50$$

The power gain is the product of the voltage gain and the current gain. The absolute value of the voltage gain with R_O added in parallel with R_L will be cut in half from 50 to 25.

Thus, the power gain is given by

$$\frac{v_o}{v_i}\frac{i_o}{i_b} = (-25) \times (-50) = 1250$$

ANS:: (a) $V_O = 10V$ (c) -50 (d) $v_o = -0.05 \sin \omega t$ (e) $r_i = 100k$ and $r_o = 50k$ (f) $\frac{i_o}{i_b} = -50$ and $\frac{v_o}{v_i}\frac{i_o}{i_b} = 1250$

Problems

Problem 8.1 This problem studies the small-signal analysis of the MOSFET amplifier discussed in Problem 7.3 (Figure 7.13) in the previous chapter.

a) First consider biasing the amplifier. Determine $V_{\rm IN}$, the bias component of $v_{\rm IN}$, so that $v_{\rm OUT}$ is biased to $V_{\rm OUT}$ where $0 < V_{\rm OUT} < V_{\rm S}$. Find $V_{\rm MID}$, the bias component of $v_{\rm MID}$ in the process.

b) Next, let $v_{\rm IN} = V_{\rm IN} + v_{\rm in}$ where $v_{\rm in}$ is considered to be a small perturbation of $v_{\rm IN}$ around $V_{\rm IN}$. Make the substitution for $v_{\rm IN}$ and linearize the resulting expression for $v_{\rm OUT}$. Your answer should take the form $v_{\rm OUT} = V_{\rm OUT} + v_{\rm out}$, where $v_{\rm out}$ takes the form $v_{\rm out} = Gv_{\rm in}$. Note that $v_{\rm out}$ is the small-signal output and G is the small-signal gain. Derive an expression for G.

c) For what value of $V_{\rm IN}$ is $v_{\rm OUT}$ biased to $V_{\rm OUT} = V_{\rm S}/2$? For this value of $V_{\rm IN}$, evaluate $G_{\rm m}$ using the numerical parameters given in Problem 7.2 in the previous chapter. You should find that this gain is the slope of the input-output graph from Problem 7.3 in the previous chapter evaluated at the bias point.

Solution:

a)

$$\begin{aligned} V_{\rm MID} &= V_{\rm S} - I'_{\rm D}R \\ &= V_{\rm S} - 0.5KR(V_{\rm IN} - v_{\rm T})^2 \end{aligned}$$

$$\begin{aligned} V_{\rm OUT} &= V_{\rm S} - I''_{\rm D}R \\ &= V_{\rm S} - 0.5KR(V_{\rm MID} - v_{\rm T})^2 \end{aligned}$$

From above we can solve for $V_{\rm MID}$,

$$V_{\rm MID} = \sqrt{\frac{2(V_{\rm S} - V_{\rm OUT})}{KR}} + v_{\rm T}$$

Similarly,

$$\begin{aligned} V_{\rm IN} &= \sqrt{\frac{2(V_{\rm S} - V_{\rm MID})}{KR}} + v_{\rm T} \\ &= \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} - \sqrt{\frac{8V_{\rm S}}{K^3R^3} - \frac{8V_{\rm OUT}}{K^3R^3}}} + V_{\rm T} \end{aligned}$$

b) Let $v_{\rm IN} = V_{\rm IN} + v_{in}$, we first solve for the current $i'_{\rm D}$ going through the first amplifier,

$$\begin{aligned} i'_{\rm D} &= .5K(V_{\rm IN} + v_{in} - v_{\rm T})^2 \\ &= .5K(V_{\rm IN} - v_{\rm T})^2 + Kv_{in}(V_{\rm IN} - v_{\rm T}) + .5Kv_{in}^2 \\ &\approx .5K(V_{\rm IN} - v_{\rm T})^2 + Kv_{in}(V_{\rm IN} - v_{\rm T}) \\ &= I'_{\rm D} + i'_{\rm d} \end{aligned}$$

$v_{\rm MID}$ is related to $i'_{\rm D}$ by the following equations:

$$\begin{aligned} v_{\rm MID} &= V_{\rm S} - (I'_{\rm D} + i'_{\rm d})R \\ &= V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - RKv_{in}(V_{\rm IN} - v_{\rm T}) \end{aligned}$$

Now we solve for the current $i''_{\rm D}$, which goes through the second amplifier,

$$\begin{aligned} i''_{\rm D} &= .5K(v_{\rm MID} - v_{\rm T})^2 \\ &= .5K(V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - RKv_{in}(V_{\rm IN} - v_{\rm T}) - v_{\rm T})^2 \\ &= .5K[V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}]^2 \\ &\quad - [V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}][RK^2(V_{\rm IN} - v_{\rm T})]v_{in} \\ &\quad + .5K^3R^2(V_{\rm IN} - v_{\rm T})^2 v_{in}^2 \\ &\approx .5K[V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}]^2 \\ &\quad - [V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}][RK^2(V_{\rm IN} - v_{\rm T})]v_{in} \end{aligned}$$

Finally we relate $v_{\rm OUT}$ to $v_{\rm IN}$,

$$\begin{aligned} v_{\rm OUT} &= V_{\rm S} - i''_{\rm D}R \\ &= V_{\rm S} - .5KR[V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}]^2 \\ &\quad + K^2R^2[V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}](V_{\rm IN} - v_{\rm T})v_{in} \\ &= V_{\rm OUT} + v_{out} \\ &= V_{\rm OUT} + G_m v_{in} \end{aligned}$$

where $G_m = K^2R^2[V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}](V_{\rm IN} - v_{\rm T})$.

c) Recalling the equation derived in part (a), we get that

$$\frac{V_{\rm S}}{2} = \sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} - \sqrt{\frac{4V_{\rm S}}{K^3R^3}}} + V_{\rm T}.$$

We substitute this into the formula for gain, getting that

$$G_{\rm m} = K^2R^2\left(\sqrt{\frac{V_{\rm S}}{KR}}\right)\left(\sqrt{\frac{2V_{\rm S}}{KR} - \frac{2V_{\rm T}}{KR} - \sqrt{\frac{4V_{\rm S}}{K^3R^3}}}\right)$$

The parameters given previously were $V_{\rm S} = 5$V, $V_{\rm T} = 2$V, and $KR = 30$. From these parameters, we can find a numerical value of $G_{\rm m}$, which turns out to be approximately 136.

ANS:: (a) $V_{\rm MID} = \sqrt{\frac{2(V_{\rm S}-V_{\rm OUT})}{KR}} + v_{\rm T}$, $V_{\rm IN} = \sqrt{\frac{2(V_{\rm S}-V_{\rm MID})}{KR}} + v_{\rm T}$ (b) $G_m = K^2R^2[V_{\rm S} - .5KR(V_{\rm IN} - v_{\rm T})^2 - v_{\rm T}](V_{\rm IN} - v_{\rm T})$ (c) 136

Problem 8.2 Consider again the buffer described in Problem 7.5 (Figure 7.15) in the previous chapter. Perform a small-signal analysis of this circuit according to the following steps. Assume that the MOSFET operates in its saturation region and continue to use the SCS MOSFET model with parameters V_T and K.

a) Draw the small-signal circuit model of the buffer.

b) Show that the small-signal transconductance g_m of the MOSFET is given by

$$g_m = K(V_{\rm IN} - V_{\rm OUT} - V_{\rm T})$$

where $V_{\rm IN}$ and $V_{\rm OUT}$ are the bias, or operating-point, input and output voltages, respectively.

c) Determine the small-signal gain of the buffer. That is, determine the ratio $v_{\rm out}/v_{\rm in}$.

d) Determine the small-signal output resistance of the buffer. That is, determine the equivalent resistance of the buffer at the output port of its small-signal model with $v_{\rm in} \equiv 0$.

e) Assume that $V_{\rm T} = 1$ V, $K = 2$ mA/V^2, $R = 1$ kΩ and $V_{\rm S} = 10$ V. Under this assumption, design the input bias voltage to satisfy the following two objectives. First, MOSFET operation must remain within the saturation region for $|v_{\rm in}| \leq 0.25$ V. Second, the output resistance of the small-signal model must be minimized.

f) Again assume that $V_{\rm T} = 1$ V, $K = 2$ mA/V^2, $R = 1$ kΩ and $V_{\rm S} = 10$ V. For $V_{\rm IN} = 3$ V, compute the small-signal gain and output resistance.

g) Determine the small-signal input resistance of the buffer. That is, determine the equivalent resistance of the buffer at the input port of its small-signal model.

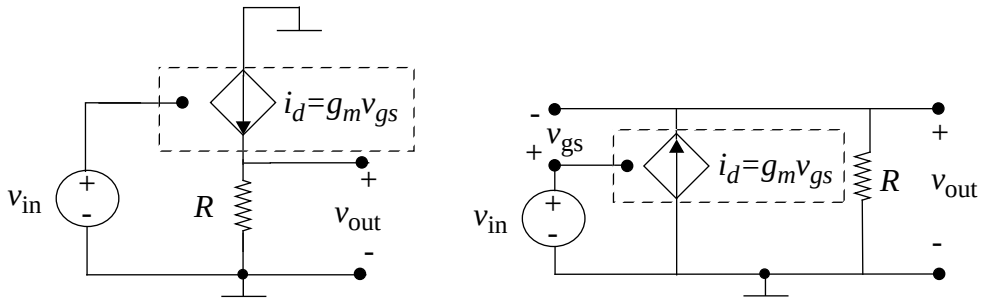
Solution:

a)

b) Use the formula for the MOSFET large-signal current source (in saturation):

$$i_{\rm D} = \frac{K}{2}(v_{\rm GS} - v_{\rm T})^2$$

Expand this formula in a Taylor series for $v_{\rm GS} = V_{\rm GS} + v_{\rm gs}$ (Total Signal = LARGE-SIGNAL + small-signal).



$$\mathrm{I_D} + i_\mathrm{d} = \left[\frac{K}{2}(v_\mathrm{GS} - v_\mathrm{T})^2\right] + v_\mathrm{gs}\left[2 * \frac{K}{2}(v_\mathrm{GS} - v_\mathrm{T})\right] + \frac{v_\mathrm{gs}^2}{2}[K] + \ldots$$

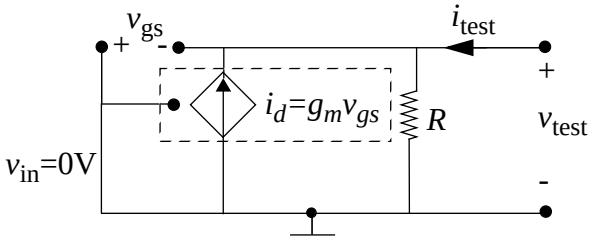
where the bracketed terms are evaluated at the large-signal bias point $v_\mathrm{GS} = V_\mathrm{GS}$. Then $\mathrm{I_D} = \frac{K}{2}(V_\mathrm{GS} - v_\mathrm{T})^2$. Ignoring higher-order terms, $i_\mathrm{d} = g_\mathrm{m} v_\mathrm{gs}$ where

$$g_\mathrm{m} = K(V_\mathrm{GS} - v_\mathrm{T}) = K(V_\mathrm{IN} - V_\mathrm{OUT} - v_\mathrm{T}) \tag{8.1}$$

c) Using small-signal equivalents, $v_\mathrm{out} = i_\mathrm{d} R = g_\mathrm{m} v_\mathrm{gs} R = g_\mathrm{m}(v_{in} - v_{out})R$.

$$gain = \frac{v_\mathrm{out}}{v_\mathrm{in}} = \frac{g_\mathrm{m} R}{1 + g_\mathrm{m} R} \tag{8.2}$$

d) Connect v_in to ground. Apply v_test at the output and measure i_test. Note that v_test and i_test appear to be anti-associated variables, but they will be associated variables for the equivalent resistance we are measuring.



Using KCL,

$$i_\mathrm{d} + i_\mathrm{test} = \frac{v_\mathrm{test}}{R}$$

Note that $i_\mathrm{d} = g_\mathrm{m} v_\mathrm{gs} = g_\mathrm{m}(-v_\mathrm{test})$ when v_in is grounded.

$$-g_\mathrm{m} v_\mathrm{test} + i_\mathrm{test} = \frac{v_\mathrm{test}}{R}$$

$$R_\mathrm{out} = \frac{v_\mathrm{test}}{i_\mathrm{test}} = \frac{R}{1 + g_\mathrm{m} R} \tag{8.3}$$

e) To minimize the output resistance for a fixed value of R, we need to maximize g_{m}.

$$g_{\mathrm{m}} = K(V_{\mathrm{IN}} - V_{\mathrm{OUT}} - V_{\mathrm{T}})$$

Substitute in the formula for V_{OUT}:

$$\frac{g_{\mathrm{m}}}{K} = \left[V_{\mathrm{IN}} - \left(V_{\mathrm{IN}} - V_{\mathrm{T}} + \frac{1}{RK} - \frac{1}{2}\sqrt{\left(\frac{2}{RK}\right)^2 + 4(V_{\mathrm{IN}} - v_{\mathrm{T}})\frac{2}{RK}}\right) - V_{\mathrm{T}}\right]$$

$$g_{\mathrm{m}} = K\left(\sqrt{\left(\frac{1}{RK}\right)^2 + (V_{\mathrm{IN}} - V_{\mathrm{T}})\frac{2}{RK}} - \frac{1}{RK}\right)$$

To maximize g_{m}, maximize V_{IN}.
Choose $V_{\mathrm{IN}} = V_{\mathrm{IN\cdot max}} - v_{in\cdot max} = V_{\mathrm{S}} + V_{\mathrm{T}} - v_{in\cdot max}$ = 10V + 1V - 0.25V = 10.75V

f) Find V_{OUT} using equation (3) (derived in Exercise 5-1).

$$V_{\mathrm{OUT}} = 1V$$

Find g_m using equation (4).

$$g_m = 2\frac{\mathrm{mA}}{\mathrm{V}}$$

Plug-and-play using equations (5) and (6):

$$gain = \frac{2}{3}$$

$$R_{\mathrm{out}} = 333.3\Omega$$

g) The input resistance is infinite since the gate of a MOSFET has infinite input impedance.

ANS:: (c) $\frac{g_{\mathrm{m}}R}{1+g_{\mathrm{m}}R}$ (d) $\frac{R}{1+g_{\mathrm{m}}R}$ (e) 10.75V (f) $gain = \frac{2}{3}$, $R_{\mathrm{out}} = 333.3\Omega$ (g) infinite

Problem 8.3 This problem studies the small signal analysis of the ZFET amplifier from Problem 7.6 (Figure 7.17) in the previous chapter. Assume that the amplifier is biased at an input voltage V_{IN} such that the ZFET exhibits saturated operation; the corresponding bias output voltage is V_{OUT}. For this case, derive the small-signal voltage gain $v_{\mathrm{out}}/v_{\mathrm{in}}$ of the amplifier.

Solution:

Referring to Problem 7.6, the large signal output is $V_{\mathrm{OUT}} = V_{\mathrm{S}} - KRV_{\mathrm{IN}}^3$. Taking the derivative of this with respect to V_{IN}, one gets that

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = -3RKV_{\rm IN}^2.$$

This is, by definition, equal to the small-signal gain $v_{\rm out}/v_{\rm in}$.

ANS:: $-3RKV_{\rm IN}^2$

Problem 8.4 The circuit shown in Figure 8.8 delivers a nearly constant current to its load despite the fact that the power supply is noisy. The noise is modeled by the small signal $v_{\rm s}$ superimposed on the constant supply voltage $V_{\rm S}$. Thus, $V_{\rm S}$ and $v_{\rm s}$ are the large-signal and small-signal components of the total power supply voltage $v_{\rm S}$, respectively. $I_{\rm L}$ and $i_{\rm l}$ are the large-signal and small-signal components of the load current $i_{\rm L}$, respectively. The noise $v_{\rm s}$ in the power supply voltage satisfies $v_{\rm s} \ll V_{\rm S}$, and is responsible for the presence of $i_{\rm l}$ in $i_{\rm L}$.

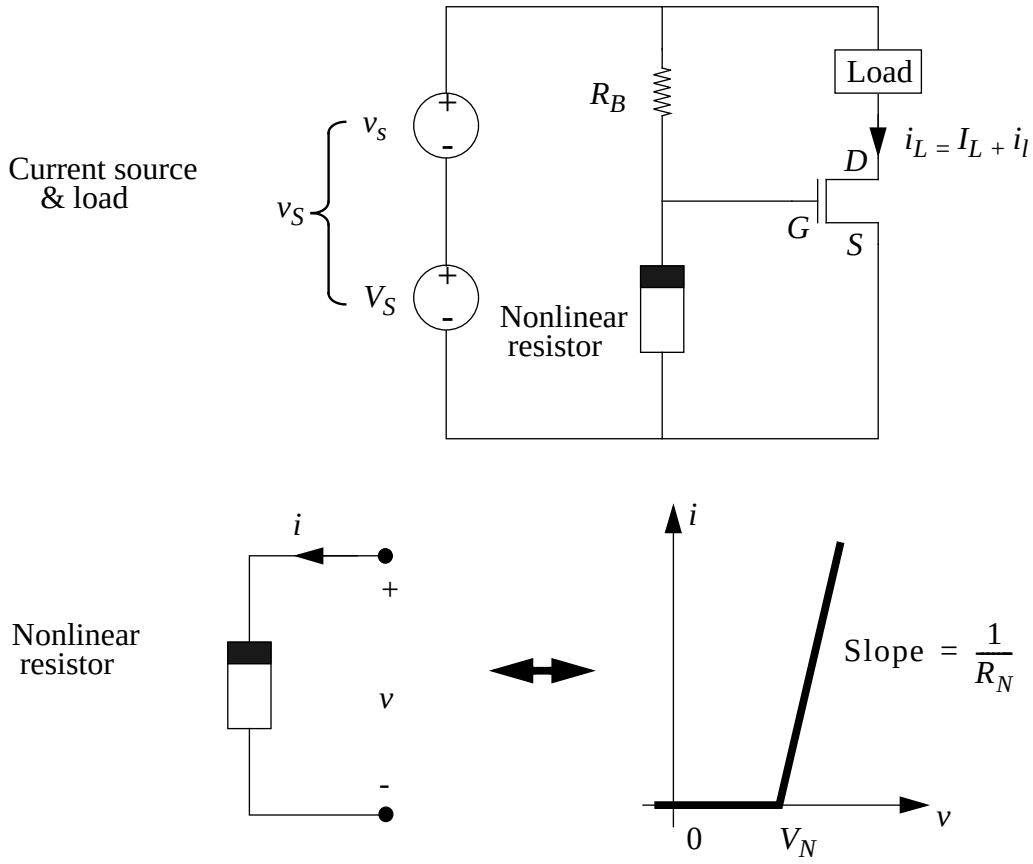


Figure 8.8:

The current source contains a MOSFET which operates in its saturation region such that $i_{\rm DS} = \frac{K}{2}(v_{\rm GS} - V_{\rm T})^2$. The current source also contains a nonlinear resistor whose terminal characteristics are described graphically below. Assume that $V_{\rm S} > V_{\rm N} > V_{\rm T}$.

a) Assume $v_{\rm s} = 0$. Determine $V_{\rm GS}$, the large-signal component of $v_{\rm GS}$, in terms of $R_{\rm B}$, $R_{\rm N}$, $V_{\rm N}$ and $V_{\rm S}$.

b) Following the result of Part (a), determine $I_{\rm L}$ in terms of $R_{\rm B}$, $R_{\rm N}$, $V_{\rm N}$, $V_{\rm S}$, K and $V_{\rm T}$.

c) Now assume that $v_{\rm s} \neq 0$. Draw a small-signal circuit model for the combined circuit comprising the power supply, current source and load, with which $i_{\rm l}$ can be found from $v_{\rm s}$. Clearly label the value of each component in the circuit model.

d) Using the small-signal model from part (c), determine the ratio $i_{\rm l}/v_{\rm s}$.

Solution:

a) We know that $v_{\rm GS} = v_{\rm N} = V_{\rm S} - Ri_{\rm N}$, so $i_{\rm N} = \frac{v_{\rm N} - V_{\rm N}}{R_{\rm N}}$. Substituting into the first equation, $v_{\rm GS} - V_{\rm S} - R_{\rm B}(\frac{V_{\rm GS} - V_{\rm N}}{R_{\rm N}})$. Solving,

$$V_{\rm GS} = \frac{V_{\rm S}R_{\rm N} + V_{\rm N}R_{\rm B}}{R_{\rm N} + R_{\rm B}}$$

b)

$$I_L = \frac{K}{2}(\frac{V_{\rm S}R_{\rm N} + V_{\rm N}R_{\rm B}}{R_{\rm N} + R_{\rm B}} - V_{\rm T})^2$$

c) See Figure 8.9.

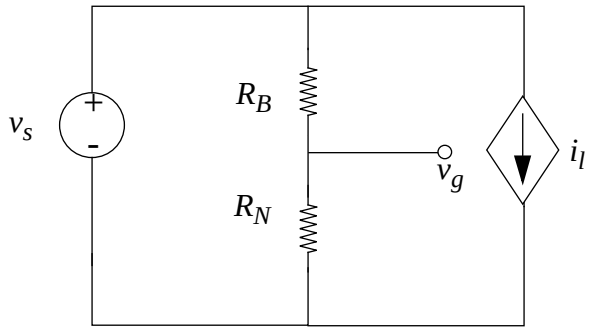


Figure 8.9:

d) Using Thevenin equivalents, $v_{\rm gs} = \frac{\frac{1}{R_{\rm N}} v_{\rm s}}{R_{\rm B} + \frac{1}{R_{\rm V}}} = \frac{v_{\rm s}}{R_{\rm B} R_{\rm N} + 1}$. Given that $i_l = K(V_{\rm GS} - V_{\rm T})^2 v_{\rm gs}$, we can solve for $i_{\rm l}$ and then divide through by $v_{\rm s}$ to find the ratio $\frac{i_{\rm l}}{v_{\rm s}}$.

$$\frac{i_{\rm l}}{v_{\rm s}} = \frac{K(\frac{V_{\rm S} R_{\rm N} + V_{\rm N} R_{\rm B}}{R_{\rm B} R_{\rm N} + 1} - V_{\rm T}}{R_{\rm B} R_{\rm N} + 1}$$

ANS:: (a) $V_{\rm GS} = \frac{V_{\rm S} R_{\rm N} + V_{\rm N} R_{\rm B}}{R_{\rm N} + R_{\rm B}}$ (b) $I_L = \frac{K}{2}(\frac{V_{\rm S} R_{\rm N} + V_{\rm N} R_{\rm B}}{R_{\rm N} + R_{\rm B}} - V_{\rm T})^2$ (d) $\frac{K(\frac{V_{\rm S} R_{\rm N} + V_{\rm N} R_{\rm B}}{R_{\rm B} R_{\rm N} + 1} - V_{\rm T}}{R_{\rm B} R_{\rm N} + 1}$

Problem 8.5 Figure 8.10 depicts a bipolar junction transistor (BJT). Recall that a BJT has three terminals called the base (B), the collector (C) and the emitter (E). Figure 8.10 also shows an alternative small signal model for the BJT operating in its active region. This model is slightly different from the small signal BJT model discussed in this chapter in that it includes a base resistance R_B. In the model shown in the figure, β is a constant.

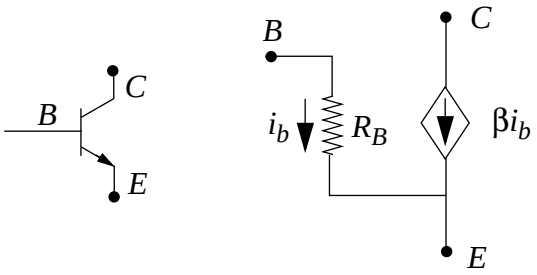


Figure 8.10:

a) Draw the small-signal equivalent circuit for the BJT amplifier shown in Figure 8.11. Use the small-signal equivalent circuit to derive the small-signal gain of the amplifier.

b) Draw the small-signal equivalent circuit for the BJT amplifier shown in Figure 8.12. Notice that the resistor divider provides the necessary bias voltage. Use the small-signal equivalent circuit to derive the small-signal gain of the amplifier.

Solution:

a) See Figure 8.13.

By KVL, $i_{\rm b} = \frac{v_i}{R_{\rm B}}$. Substituting in to the KVL equation for the other side of the circuit, $v_{\rm o} = \frac{-\beta R_{\rm L} v_{\rm i}}{R_{\rm B}}$. Therefore the gain is

$\frac{v_{\rm o}}{v_{\rm i}} = \frac{-\beta R_{\rm L}}{R_{\rm B}}$.

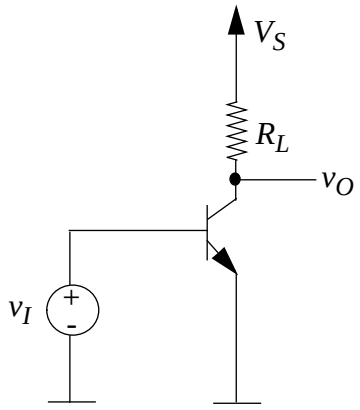


Figure 8.11:

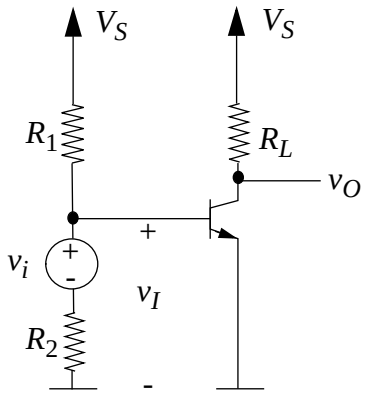


Figure 8.12:

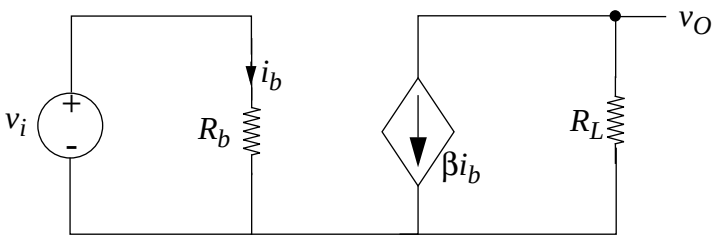


Figure 8.13:

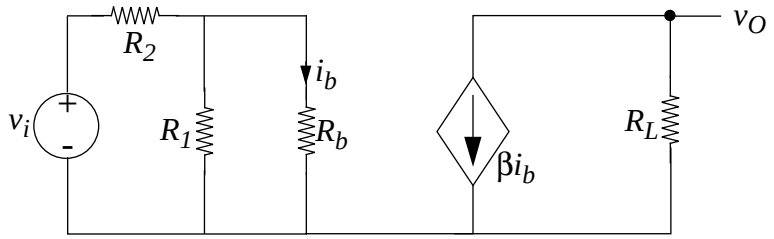


Figure 8.14:

b) See Figure 8.14.

Using KVL to find the voltage across R_1 and combining that with $v = iR$, we find that $i_{\rm b} = \frac{1}{R_{\rm B}}(\frac{R_1 v_{\rm i}}{R_1+R_2}$. By the same argument in part a., the gain is $\frac{v_{\rm o}}{v_{\rm i}} = \frac{-\beta R_{\rm L} R_1}{R_{\rm B}(R_1+R_2)}$.

ANS:: (a) $\frac{v_{\rm o}}{v_{\rm i}} = \frac{-\beta R_{\rm L}}{R_{\rm B}}$ (b) $\frac{v_{\rm o}}{v_{\rm i}} = \frac{-\beta R_{\rm L} R_1}{R_{\rm B}(R_1+R_2)}$

Problem 8.6 Consider the MOSFET-based amplifier circuit discussed in Problem 7.8 (Figure 7.20) in the previous chapter. Assuming an input bias point voltage $V_{\rm I}$, draw the small signal circuit equivalent of the amplifier. Determine the small signal gain of the amplifier. Assume throughout that the MOSFET operates in its saturation region.

Solution:

The small signal model is shown in Figure 8.15.

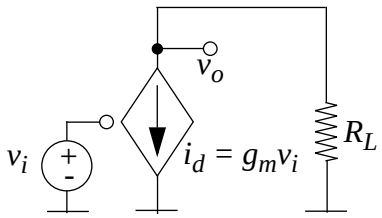


Figure 8.15:

Recall that the large-signal transfer characteristic for saturation derived in Problem 7.8 was:

$$V_{\rm OUT} = V_{\rm S} - \frac{KR}{2}(V_{\rm IN} + V_{\rm S} - V_{\rm T})^2.$$

Taking the derivative of this with respect to $V_{\rm IN}$, one gets

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = -KR(V_{\rm IN} + V_{\rm S} - V_{\rm T}).$$

This is, by definition, equal to the small-signal gain.

ANS:: $-KR(V_{\rm IN} + V_{\rm S} - V_{\rm T})$

Problem 8.7 Consider again the amplifier circuit discussed in Problem 7.8 (Figure 7.20) in the previous chapter. Suppose that the amplifier is biased such that $v_I = v_O$ at the bias point. Draw the small signal circuit equivalent of the amplifier assuming this bias point. Determine the small signal gain of the amplifier at this bias point. Assume that the MOSFET operates in its saturation region.

Solution:

The small signal circuit is shown in Figure 8.15.

Recall the formulae derived in the solutions to Problem 7.8 in the previous chapter and Problem 8.6 in this chapter.

The large-signal transfer curve in saturation is equal to:

$$V_{\rm OUT} = V_{\rm S} - \frac{KR}{2}(V_{\rm IN} + V_{\rm S} - V_{\rm T})^2.$$

Setting $V_{\rm OUT} = V_{\rm IN}$, and solving for $V_{\rm IN}$, we get that

$$V_{\rm IN} = V_{\rm T} - V_{\rm S} + \sqrt{\frac{2V_{\rm S}}{KR} + \frac{2V_{\rm T}}{KR}}.$$

Recalling the small-signal gain from Problem 8.6,

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = -RK(V_{\rm IN} + V_{\rm S} - V_{\rm T}),$$

we substitute our freshly derived value of $V_{\rm IN}$, and after simplifying, get that

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = \sqrt{2V_{\rm S}KR - 2V_{\rm T}KR}.$$

ANS:: $\sqrt{2V_{\rm S}KR - 2V_{\rm T}KR}$

Problem 8.8 Consider the common gate amplifier circuit shown in Figure 7.24, and analyzed earlier in Problem 7.11 of the previous chapter. Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K.

a) Draw the SCS equivalent circuit by replacing the MOSFET by its SCS model.

b) Determine the output operating point voltage $V_{\rm OUT}$ and operating point current $I_{\rm D}$ in terms of an input operating point voltage $V_{\rm IN}$.

c) Assuming an input bias point voltage $V_{\rm IN}$, draw the small signal model of the amplifier.

d) Determine the small signal gain $v_{\rm out}/v_{\rm in}$ of the amplifier.

e) Determine the small-signal output resistance of the amplifier. That is, determine the equivalent resistance of the amplifier at the output port of its small-signal model with $v_{\rm i} \equiv 0$. Is the small signal output resistance greater than, less than, or equal to that of the "common source" amplifier shown in Figure 8.3.

f) Determine the small-signal input resistance of the amplifier. That is, determine the equivalent resistance of the amplifier at the input port of its small-signal model. Is the small signal input resistance greater than, less than, or equal to that of the "common source" amplifier shown in Figure 8.3.

Solution:

a) See Figure 7.25 in the previous chapter.

b) As previously determined,

$$I_{\rm D} = \frac{K}{2}(V_{\rm S} - V_{\rm IN} - V_{\rm T})^2,$$

$$V_{\rm OUT} = V_{\rm S} - \frac{KR}{2}(V_{\rm S} - V_{\rm IN} - V_{\rm T})^2.$$

c) See Figure 8.16.

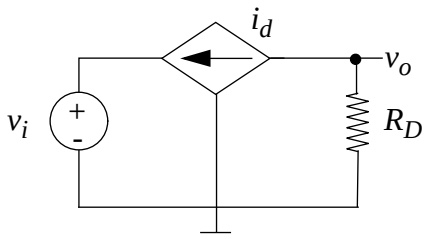


Figure 8.16:

d) Taking the derivative and simplifying, we get that

$$\frac{dV_{\rm OUT}}{dV_{rmIN}} = KR(V_{\rm S} - V_{\rm IN} - V_{\rm T}).$$

e) There is no current flowing through the MOSFET since there is no signal coming into the gate and the source is grounded. Therefore, the output resistance must simply be R.

This is larger than the output resistance of the common-source amplifier.

f) Place a test voltage across the resistor, and measure the corresponding test current.

$$i_{\rm TEST} + i_{\rm FET} = i_{\rm R}.$$

This is shown in Figure 8.17.

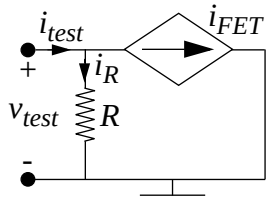


Figure 8.17:

Plugging in

$$i_{\rm FET} = G_{\rm m} v_{\rm TEST},$$

$$i_{\rm R} = \frac{v_{\rm TEST}}{R},$$

and simplifying, we get that

$$R_{\rm IN} = \frac{R}{1 - RG_{\rm m}}.$$

This is smaller than the input resistance of the common-source amplifier.

ANS:: (b) $I_{\rm D} = \frac{K}{2}(V_{\rm S} - V_{\rm IN} - V_{\rm T})^2$, $V_{\rm OUT} = V_{\rm S} - \frac{KR}{2}(V_{\rm S} - V_{\rm IN} - V_{\rm T})^2$ (d) $KR(V_{\rm S} - V_{\rm IN} - V_{\rm T})$ (e) R (f) $R_{\rm IN} = \frac{R}{1-RG_{\rm m}}$

Problem 8.9 Consider the circuit illustrated in Figure 7.30 and analyzed in Problem 7.15 in the previous chapter. Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K.

a) Draw the SCS equivalent circuit by replacing the MOSFET by its SCS model.

b) Determine the output operating point voltage $V_{\rm O}$ and operating point current $I_{\rm D}$ in terms of an input operating point voltage $V_{\rm I}$.

c) Assuming an input bias point voltage $V_{\rm I}$, draw the small signal model.

d) Determine the small signal gain $v_{\rm o}/v_{\rm i}$.

e) Determine the small-signal output resistance.

f) Determine the small-signal input resistance.

Solution:

a) See Figure 7.31 in the previous chapter.

b) We refer to Problem 7.15 for the corresponding large-signal model, as well as several key derivations, including this one for the current through the MOSFET:

$$I_{\rm D} = \frac{1}{RS}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{KR_{\rm S}^2} - \sqrt{\frac{2}{KR_{\rm S}^3}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{K^2R_{\rm S}^4}}.$$

From this, we can calculate the bias voltage to be

$$V_{\rm OUT} = \frac{1}{KR_{\rm S}} + V_{\rm I} - V_{\rm T} - \sqrt{\frac{2}{KR_{\rm S}}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{K^2R_{\rm S}^2}}.$$

The full calculation is done in Problem 7.15.

c) See Figure 8.18.

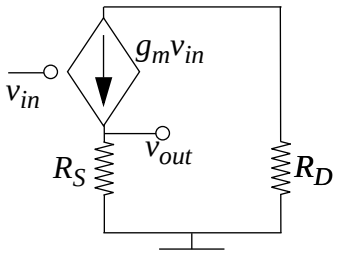


Figure 8.18:

The transconductance $g_{\rm m}$ is equal to the derivative of the I-$V_{\rm IN}$ transfer curve at the bias point.

$$g_{\rm m} = \frac{dI}{dV_{\rm IN}} = \frac{1}{R_{\rm S}} + \left(2KR_{\rm S}^3[V_{\rm IN} + V_{\rm S} - V_{\rm T}] + R_{\rm S}^2\right)^{-\frac{1}{2}}.$$

d) The small-signal gain is equal to the derivative of the $V_{\rm OUT}$-$V_{\rm IN}$ transfer curve at the operating point.

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = 1 - (2KR_{\rm S}[V_{\rm IN} + V_{\rm S} - V_{\rm T}] + 1)^{-\frac{1}{2}} .$$

e) As shown in Figure 8.19, we place a test voltage across the output, and measure the corresponding current.

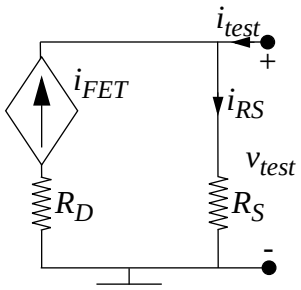


Figure 8.19:

$$i_{\rm test} + i_{\rm FET} = i_{\rm RS}.$$

Substituting in known values, we get that

$$0 + i_{\rm test} = \frac{v_{\rm test}}{R_{\rm S}}.$$

Simplifying this, one gets that

$$R_{\rm OUT} = \frac{v_{\rm test}}{i_{\rm test}} = R_{\rm S}.$$

f) Infinite. The MOSFET gate has infinite input impedance, so the input resistance is therefore infinite.

ANS:: (b) $V_{\rm OUT} = \frac{1}{KR_{\rm S}} + V_{\rm I} - V_{\rm T} - \sqrt{\frac{2}{KR_{\rm S}}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{K^2R_{\rm S}^2}}$ (d) $\frac{dV_{\rm OUT}}{dV_{\rm IN}} = 1 - (2KR_{\rm S}[V_{\rm IN} + V_{\rm S} - V_{\rm T}] + 1)^{-\frac{1}{2}}$ (e) $\frac{v_{\rm test}}{i_{\rm test}} = R_{\rm S}$ (f) infinite

Problem 8.10 Consider the circuit illustrated in Figure 7.32 and analyzed in Problem 7.16 in the previous chapter. Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K.

a) Draw the SCS equivalent circuit by replacing the MOSFET by its SCS model.

b) Determine the output operating point voltage $V_{\rm O}$ and operating point current $I_{\rm D}$ in terms of an input operating point voltage $V_{\rm I}$.

c) Assuming an input bias point voltage $V_{\rm I}$, draw the small signal model.

d) Determine the small signal gain $v_{\rm o}/v_{\rm i}$.

e) Determine the small-signal output resistance.

f) Determine the small-signal input resistance.

Solution:

a) See Figure 7.33 in the previous chapter.

b) From Problem 7.16, we get that the current is

$$I_{\rm D} = \frac{1}{RS}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{KR_{\rm S}^2} - \sqrt{\frac{2}{KR_{\rm S}^3}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{K^2R_{\rm S}^4}}.$$

From this, we can determine the voltage to be

$$V_{\rm OUT} = V_{\rm S} - \frac{R_{\rm D}}{KR_{\rm S}^2} + \frac{R_{\rm D}}{R_{\rm S}}(V_{\rm I} - V_{\rm T} + V_{\rm S}) - \sqrt{\frac{2R_{\rm D}^2}{KR_{\rm S}^3}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{R_{\rm D}^2}{K^2R_{\rm S}^4}}.$$

This was calculated in problem Problem 7.16.

c) See Figure 8.20.

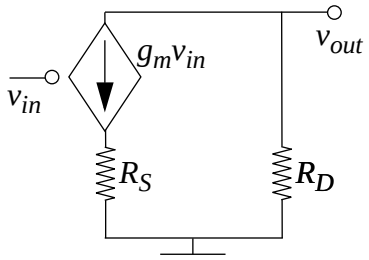


Figure 8.20:

The transconductance is the same as had been derived in Problem 8.9.

$$g_{\rm m} = \frac{dI}{dV_{\rm IN}} = \frac{1}{R_{\rm S}} + \left(2KR_{\rm S}^3[V_{\rm IN} + V_{\rm S} - V_{\rm T}] + R_{\rm S}^2\right)^{-\frac{1}{2}}.$$

d) This is equal to the slope of the $V_{\rm O}$-$V_{\rm I}$ transfer curve at the operating point.

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = \frac{R_{\rm D}}{R_{\rm S}} - \left(\frac{2KR_{\rm S}^3}{R_{\rm D}^2}[V_{\rm IN} + V_{\rm S} - V_{\rm T}] + \frac{R_{\rm S}^2}{R_{\rm D}^2} \right)^{-\frac{1}{2}}.$$

e) As shown in Figure 8.21, we place a test voltage across the output, and measure the corresponding current.

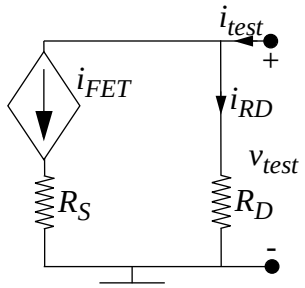


Figure 8.21:

$$i_{\rm test} = i_{\rm FET} + i_{\rm RD}.$$

Substituting in known values, we get that

$$i_{\rm test} = 0 + \frac{v_{\rm test}}{R_{\rm D}}.$$

Simplifying this, one gets that

$$R_{\rm OUT} = \frac{v_{\rm test}}{i_{\rm test}} = R_{\rm D}.$$

f) Infinite. The MOSFET gate has infinite input impedance, so the input resistance is therefore infinite.

ANS:: (b) $I_{\rm D} = \frac{1}{RS}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{KR_{\rm S}^2} - \sqrt{\frac{2}{KR_{\rm S}^3}(V_{\rm IN} + V_{\rm S} - V_{\rm T}) + \frac{1}{K^2R_{\rm S}^4}}$ (d) $\frac{R_{\rm D}}{R_{\rm S}} - \left(\frac{2KR_{\rm S}^3}{R_{\rm D}^2}[V_{\rm IN} + V_{\rm S} - V_{\rm T}] + \frac{R_{\rm S}^2}{R_{\rm D}^2} \right)^{-\frac{1}{2}}$ (e) $R_{\rm OUT} = \frac{v_{\rm test}}{i_{\rm test}} = R_{\rm D}$ (f) infinite

Problem 8.11 This problem studies the small signal analysis of the amplifier analyzed in Problem 7.14 of the previous chapter (see Figure 7.28). Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K.

a) Draw the small signal equivalent circuit of the amplifier driving the load resistor $R_{\rm E}$, assuming an input bias voltage $V_{\rm I}$.

b) Determine the small signal gain of the amplifier when it is driving the load $R_{\rm E}$.

Solution:

a) See Figure 8.22.

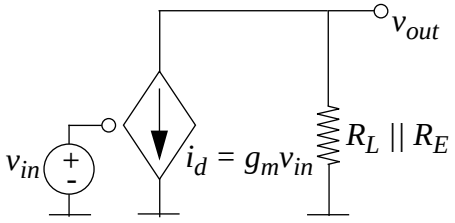


Figure 8.22:

From Problem 7.14, we get that the current through the MOSFET is as follows:

$$I = \frac{K}{2}(V_{\rm IN} - V_{\rm T})^2.$$

Taking the derivative of this, we get the transconductance,

$$g_{\rm m} = K(V_{\rm IN} - V_{\rm T}).$$

b) We note that the current has nowhere to go but through the two resistors in parallel, so we use a simple $V = IR$ relationship to determine the output voltage.

$$-v_{\rm out} = g_{\rm m} v_{\rm in}(R_{\rm L}||R_{\rm E}).$$

The gain is equal to the small-signal output voltage divided by the small-signal input voltage.

$$\frac{v_{\rm out}}{v_{\rm in}} = -\frac{R_{\rm L}R_{\rm E}}{R_{\rm L} + R_{\rm E}} K(V_{\rm IN} - V_{\rm T}).$$

This may be checked by the more traditional method of finding the output voltage as a function of the input voltage, and taking its derivative.

ANS:: (b) $-\frac{R_{\rm L}R_{\rm E}}{R_{\rm L}+R_{\rm E}}K(V_{\rm IN}-V_{\rm T})$

Problem 8.12 This problem studies the small signal analysis of the circuit analyzed in Problem 7.17 of the previous chapter (see Figure 7.34). Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K.

a) Draw the small signal equivalent circuit assuming an input bias voltage $V_{\rm I}$. What is the value of $g_{\rm m}$ for the MOSFET under the given biasing conditions?

b) Determine the small signal voltage gain $v_{\rm o}/v_{\rm i}$. What does the $v_{\rm o}/v_{\rm i}$ expression simplify to when each of $g_{\rm m}R_1$, $g_{\rm m}R_2$, and $g_{\rm m}R_{\rm L}$ is much greater than 1.

Solution:

a) See Problem 7.17 for key large-signal derivations. See Figure 8.23 for the small-signal model.

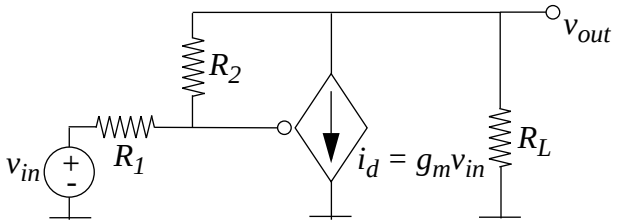


Figure 8.23:

$$g_{\rm m} = K(V_{\rm G} - V_{\rm T}).$$

$V_{\rm G}$ was derived as a function of $V_{\rm IN}$ and $V_{\rm OUT}$ in Problem 7.17. $V_{\rm OUT}$ can be found in terms of $V_{\rm IN}$, but the derivation is quite messy.

b) We must use implicit differentiation to find the small-signal gain, since we do not have $V_{\rm OUT}$ in terms of $V_{\rm IN}$, but we do have an expression that relates the two:

$$\frac{V_{\rm S}-V_{\rm OUT}}{R_{\rm L}} + \frac{V_{\rm IN}-V_{\rm OUT}}{R_1+R_2} = \frac{K}{2}\left(\frac{R_2}{R_1+R_2}V_{\rm IN} + \frac{R_1}{R_1+R_2}V_{\rm OUT} - V_{\rm T}\right)^2.$$

Differentiating this, we get

$$A = K(B)(C).$$

$$A = \frac{-dV_{\rm OUT}}{R_{\rm L}} + \frac{dV_{\rm IN} - dV_{\rm OUT}}{R_1 + R_2}$$

$$B = \frac{R_2}{R_1 + R_2} V_{\rm IN} + \frac{R_1}{R_1 + R_2} V_{\rm OUT} - V_{\rm T}.$$

$$C = \frac{R_2}{R_1 + R_2} dV_{\rm IN} + \frac{R_1}{R_1 + R_2} dV_{\rm OUT}.$$

We can substitute in $g_{\rm M} = K(V_{\rm G} - V_{\rm T})$, and solve for the ratio of the differentials:

$$\frac{dV_{\rm OUT}}{dV_{\rm IN}} = \frac{R_{\rm L} - g_{\rm m} R_2 R_{\rm L}}{R_1 + R_2 + R_{\rm L} + g_{\rm m} R_1 R_{\rm L}}.$$

From this, when R_1 becomes very large, then the gain goes to zero. This is because resistor R_1 is the only connection from $V_{\rm IN}$ to the gate, so if it is opened up, any change in $V_{\rm IN}$ is made irrelevant.

When R_2 becomes very large, the gain approaches $-g_{\rm m} R_{\rm L}$. This makes sense because the input impedance is dependent on R_2, and if it becomes infinitely large, we are dealing with a standard MOSFET amplifier.

When $R_{\rm L}$ becomes very large, the gain theoretically approaches $-R_2/R_1$, but this is not actually realistic since that implies cutting off the supply voltage, and thereby taking the MOSFET out of saturation.

ANS:: (a) $g_{\rm m} = K(V_{\rm G} - V_{\rm T})$

Problem 8.13 This problem studies the small signal analysis of the source follower (or common collector) BJT circuit analyzed in Problem 7.18 of the previous chapter (see Figure 7.36). Assume that the BJT operates in its active region throughout this problem.

a) Determine the output operating point voltage V_O and operating point current I_E in terms of an input operating point voltage V_I.

b) Assuming an input bias point voltage V_I, draw the small signal model of the source follower amplifier.

c) Determine the small signal gain v_o/v_i of the amplifier.

d) Determine the small-signal output resistance of the source follower amplifier. Is this resistance greater than, less than, or equal to that of the "common emitter" amplifier analyzed in Exercise 8.7 and shown in Figure 8.6.

e) Determine the small-signal input resistance of the amplifier. Is the input resistance greater than, less than, or equal to that of the "common emitter" amplifier shown in Figure 8.6.

f) Determine the small signal current and power gain of the source follower amplifier. Assume for this part that the amplifier is driving an output load of R_O connected between the output node and ground.

Solution:

a)

$$\begin{aligned} V_O &= I_E R_E \\ &= I_B(\beta+1)R_E \\ &= \tfrac{V_I-(V_O+0.6)}{R_I}(\beta+1)R_E \\ &= (V_I - V_O - 0.6)(\beta+1)\tfrac{R_E}{R_I} \\ &= \tfrac{V_I-0.6}{1+\frac{R_I}{(\beta+1)R_E}} \end{aligned}$$

$$I_E = \frac{V_O}{R_E} = \frac{V_I - 0.6}{R_E + \frac{R_I}{(\beta+1)}}$$

b)

c)

$$\begin{aligned} v_o &= i_e R_E \\ &= i_b(\beta+1)R_E \\ &= \tfrac{v_i-v_o}{R_I}(\beta+1)R_E \\ &= (v_i - v_o)(\beta+1)\tfrac{R_E}{R_I} \\ &= \tfrac{v_i}{1+\frac{R_I}{(\beta+1)R_E}} \end{aligned}$$

Or, the small gain is

$$\frac{v_o}{v_i} = \frac{1}{1+\frac{R_I}{(\beta+1)R_E}}$$

Further, when $\beta R_E >> R_I$,

$$\frac{v_o}{v_i} \approx 1$$

d) The small-signal output resistance is determined by applying a test voltage v_{test} at the output and measuring the resulting current i_{test} into the output node from the test voltage. We also set the input voltage v_i to zero.

$$i_{test} = \frac{v_{test}}{R_E||R_I} + \beta\frac{v_{test}}{R_I}$$

Or

$$\frac{v_{test}}{i_{test}} = 1/\left(\frac{1}{R_E||R_I} + \beta\frac{1}{R_I}\right)$$

In other words

$$r_o = \frac{v_{test}}{i_{test}} = (R_E||R_I)/\left(1 + \beta\frac{R_E||R_I}{R_I}\right)$$

When $\beta(R_E||R_I)/R_I >> 1$,

$$r_o \approx R_I/\beta$$

The β factor in the denominator makes the output resistance of the BJT source-follower significantly lower than that of the BJT common-emitter amplifier (for comparable values of R_E and R_L).

e) The small-signal input resistance is determined by applying a test voltage v_{test} at the input and measuring the resulting current i_b into the input node from the test voltage.

$$i_b = \frac{v_{test} - v_o}{R_I}$$

Or, substituting for v_o

$$i_b = \frac{v_{test} - \beta i_b R_E}{R_I}$$

Multiplying throughout by R_I and dividing throughout by i_b, and simplifying, we get

$$r_i = \frac{v_{test}}{i_b} = R_I + \beta R_E$$

When $\beta R_E >> R_I$,

$$r_i \approx \beta R_E$$

The β factor in the numerator makes the input resistance of the BJT source-follower significantly higher than that of the BJT common-emitter amplifier (assuming $\beta R_E >> R_I$, and the same value of R_I for both amplifiers).

f) To compute the current gain and power gain, we are given that there is a resistance R_O connected between the output node and ground.

The small-signal current gain is the ratio i_o/i_b, where i_o is the current into the output load resistor R_O.

The total current into the resistance pair formed by R_E and R_O is

$$i_b + \beta i_b = (\beta + 1) i_b$$

Applying the current divider relation,

$$i_o = (\beta + 1) i_b \frac{R_E}{R_E + R_O}$$

Dividing by i_b, we get the current gain as

$$\text{Current Gain} = \frac{i_o}{i_b} = (\beta + 1) \frac{R_E}{R_E + R_O}$$

We know that the power gain is given by

$$\text{Power Gain} = \frac{v_o}{v_i} \frac{i_o}{i_b}$$

Substituting for the voltage gain and the current gain

$$\text{Power Gain} = \frac{v_o}{v_i} \frac{i_o}{i_b} = \frac{1}{1 + \frac{R_I}{(\beta+1)(R_E || R_O)}} \times (\beta + 1) \frac{R_E}{R_E + R_O}$$

Notice that we have substituted $R_L || R_O$ as the effective load resistance in computing the voltage gain. Simplifying,

$$\text{Power Gain} = (\beta + 1)^2 \frac{R_E^2}{(R_E + R_O)^2} \frac{1}{R_I + (\beta + 1) R_E || R_O}$$

ANS:: (a) $V_O = \frac{V_I - 0.6}{1 + \frac{R_I}{(\beta+1)R_E}}$ and $I_E = \frac{V_I - 0.6}{R_E + \frac{R_I}{(\beta+1)}}$ (c) $\frac{v_o}{v_i} = \frac{1}{1 + \frac{R_I}{(\beta+1)R_E}}$ (d) $r_o = (R_E || R_I) / \left(1 + \beta \frac{R_E || R_I}{R_I}\right)$ and $r_i = R_I + \beta R_E$ (f) $\frac{i_o}{i_b} = (\beta + 1) \frac{R_E}{R_E + R_O}$ and Power Gain $= (\beta + 1)^2 \frac{R_E^2}{(R_E + R_O)^2} \frac{1}{R_I + (\beta+1) R_E || R_O}$

Problem 8.14 Consider again the compound three terminal device formed by connecting two BJTs in the configuration shown in Figure 7.37 (Problem 7.19) in the previous chapter. This problem relates to the small signal analysis of this device. Assume that the two BJTs are identical, each with $\beta = 100$, and that each of the BJTs operates in the active region.

a) Draw the active-region equivalent circuit of the compound BJT by replacing each of the BJTs by the piecewise linear (large signal) model shown in Exercise 7.8. Clearly label the C', B' and E' terminals.

b) Develop a small signal model containing a single dependent current source for the compound device by linearizing the circuit model in (a) and simplifying suitably.

Chapter 9

Capacitors and Inductors

Exercises

Exercise 9.1 Find the equivalent capacitance between the two terminals in each of the networks in Figure 9.1.

Solution:

(a) $3/4\mu F$

(b) $4\mu F$

(c) $4/3\mu F$

ANS:: (a) $3/4\mu F$ (b) $4\mu F$ (c) $4/3\mu F$

Exercise 9.2 Find the equivalent capacitance or inductance for each case in Figure 9.2.

Solution:

(a)

$$\frac{1\mu F \cdot 2\mu F}{1\mu F + 2\mu F} = \frac{2}{3}\mu F$$

(b)

$$\frac{1\mu F \cdot 10pF}{1\mu F \cdot 10pF} = 9.9pF \rightarrow \text{“p” = “pico” = } 10^{-12}$$

(c)

$$\frac{40pF \cdot 1\mu F}{40pF + 1\mu F} = 38.5pF$$

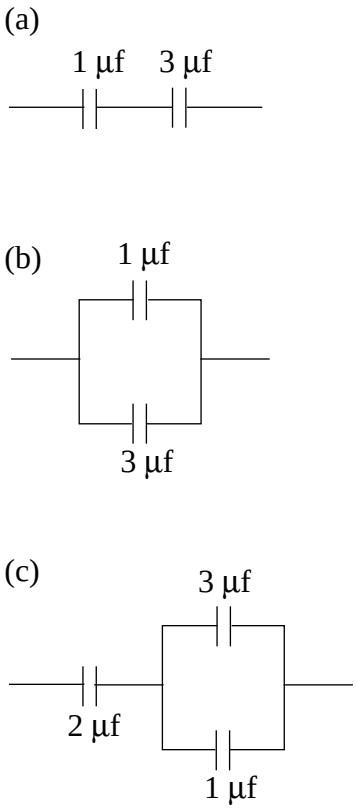


Figure 9.1:

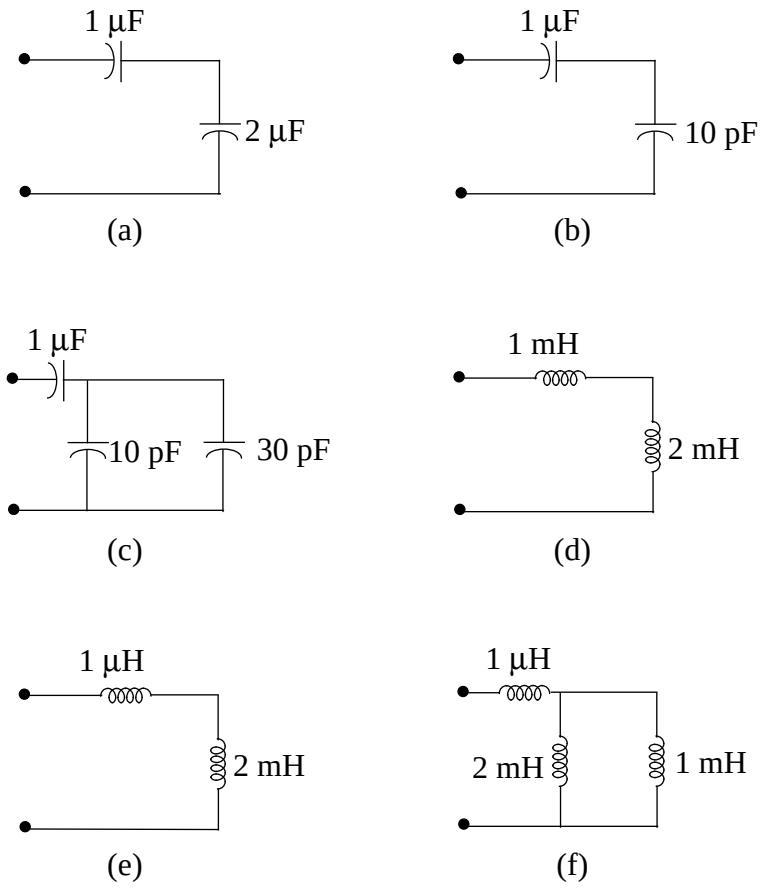

1 μF
2 μF
(a)
1 μF
10 pF
(b)
1 μF
10 pF
30 pF
(c)
1 mH
2 mH
(d)
1 μH
2 mH
(e)
1 μH
2 mH
1 mH
(f)

Figure 9.2:

(d)

$$1mH + 2mH = 3mH$$

(e)

$$2mH + 1\mu H = 2.00mH$$

(f)

$$\frac{2mH \cdot 1mH}{2mH + 1mH} + 1\mu H \cong 2/3mH$$

ANS:: (a) 2/3 μ F (b) 9.9pF (c) 38.5pF (d) 3mH (e) 2mH (f) 2/3mH

Exercise 9.3 Consider a power line on a computer backplane that is 2.5 mm wide, and separated from its underlying ground plane by 25 μm. Let the permittivity and permeability of the separating insulator be $2\epsilon_\circ$ and $\mu_\circ$, respectively. What is the capacitance and inductance of the line per 10 cm of length?

If the voltage on the line is 5 V how much energy is stored in its capacitance per 10 cm of length? If the current through the line is 1 A how much energy is stored in its inductance per 10 cm of length?

Solution:

Exercise 9.4 A current source drives a capacitor as shown in Figure 9.3. The source current is as shown in Figure 9.4 for $0 \leq t \leq T$. If the capacitor voltage is $V_\circ$ at $t = T$, what was it at $t = 0$?

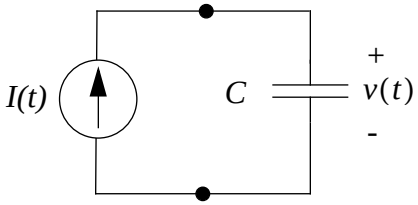


Figure 9.3: A current source driving a capacitor

Solution:

Exercise 9.5 A voltage source drives an inductor as shown in Figure 9.5. The source voltage is as shown in Figure 9.6 for $0 \leq t \leq T$. If the inductor current is $I_\circ$ at $t = T$, what was it at $t = 0$?

Solution:

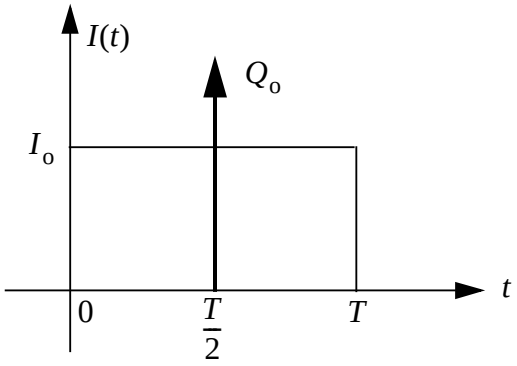


Figure 9.4: Source current

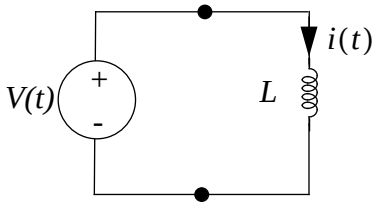


Figure 9.5: A current source driving an inductor

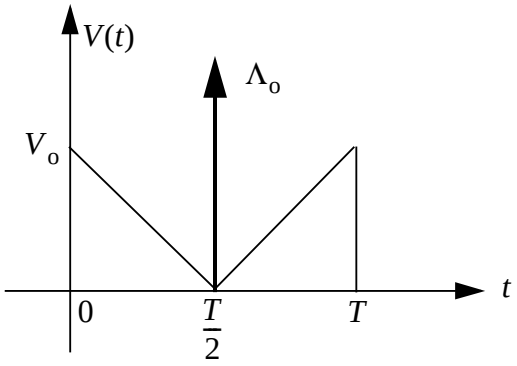


Figure 9.6: Source current

Exercise 9.6 Figure 9.7 shows four circuits, labeled "1" through "4", together with the waveform for the source in each circuit. The figure also shows four branch-variable waveforms, labeled "a" through "d", that could correspond to the branch currents i or branch voltages v labeled in the circuits. Match the branch variable waveforms to the appropriate circuit and source waveform.

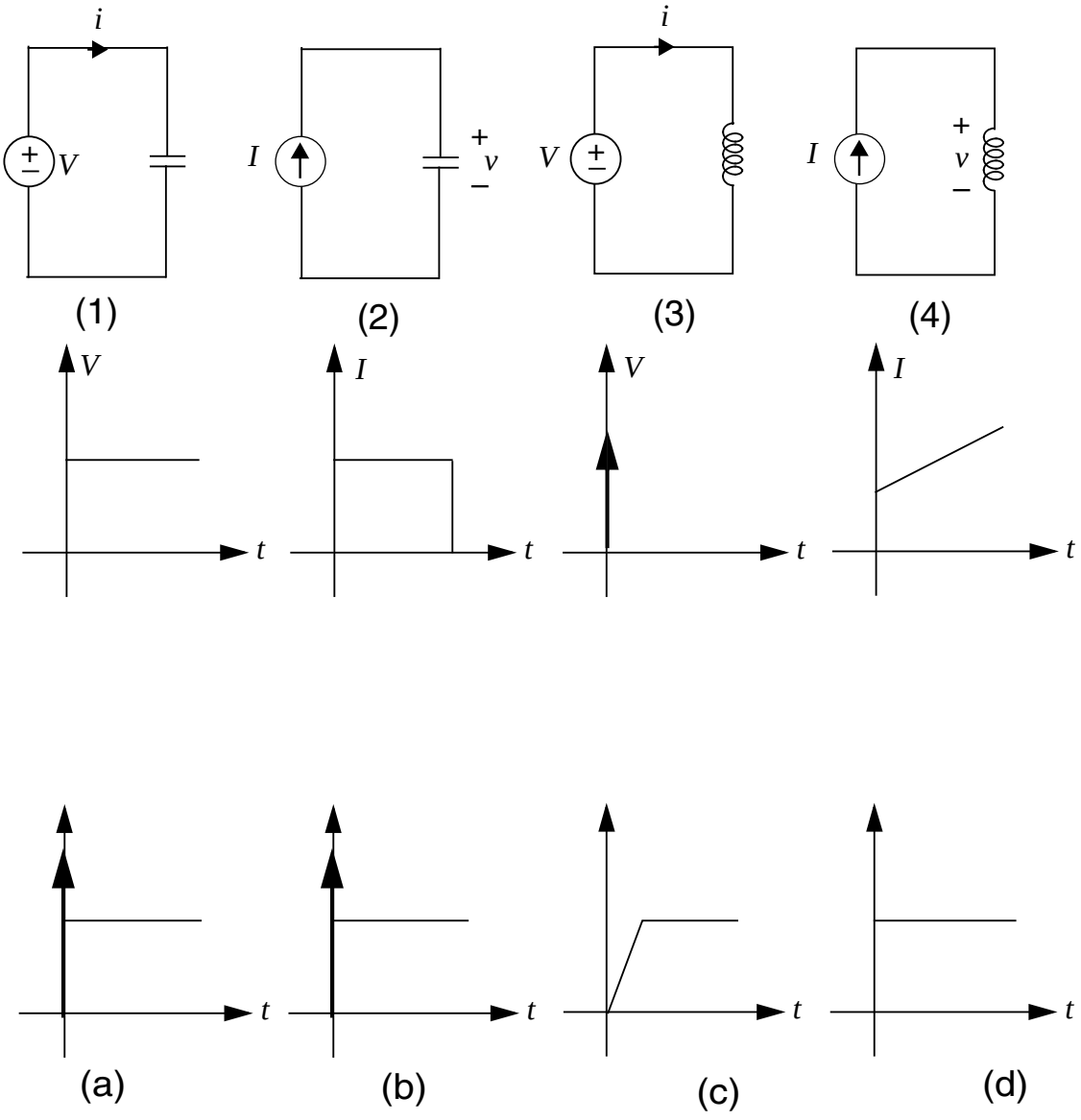


Figure 9.7: Source current

Solution:

Problem 9.1 A voltage source is connected in series with two capacitors as shown in Figure 9.8. The source voltage is $V(t) = 5\ \mathrm{V}\ u(t)$, as shown. If the current i and voltage v are given by $i(t) = 4\ \mu\mathrm{C}\ \delta(t)$ and $v(t) = 1\ \mathrm{V}\ u(t)$, again as shown, what are C_1 and C_2?

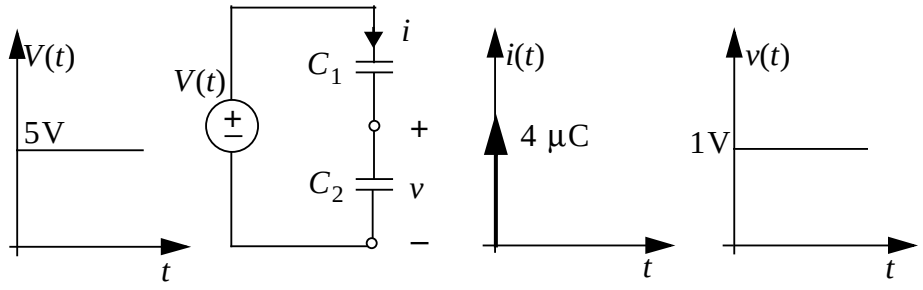


Figure 9.8:

Solution:

Problem 9.2 A current source is connected in parallel with two inductors as shown in Figure 9.9. The source current is $i(t) = 400\ \mathrm{A/s}\ u(t)$, as shown. If the current i and voltage v are given by $i(t) = 100\ \mathrm{A/s}\ u(t)$ and $v(t) = 0.3\ \mathrm{V}\ u(t)$, again as shown, what are L_1 and L_2?

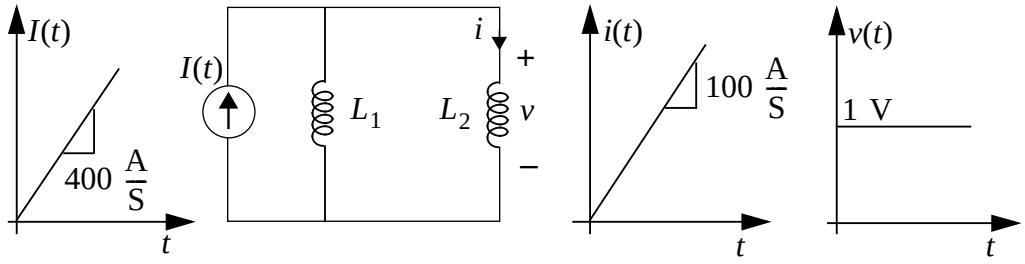


Figure 9.9:

Solution:

Problem 9.3 A current source drives a series-connected capacitor and inductor as shown in Figure 9.10. Let $I(t) = I_\circ \sin(\omega t)u(t)$, and assume that the inductor and capacitor both stored no energy prior to $t = 0$.

Determine the voltage v for $t \geq 0$.

Is there any relation between $I_\circ$, ω, C and L for which v is constant for $t \geq 0$? If so, state the relation and determine v.

Solution:

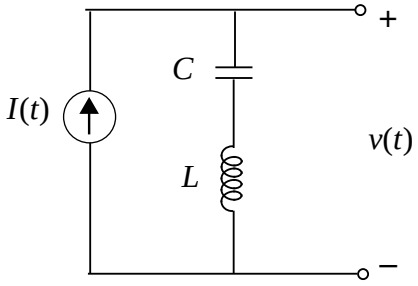


Figure 9.10:

Problem 9.4 A voltage source drives a parallel-connected capacitor and inductor as shown in Figure 9.11. Let $V(t) = V_\circ \sin(\omega t)u(t)$, and assume that the inductor and capacitor both stored no energy prior to $t = 0$.

Determine the current i for $t \geq 0$.

Is there any relation between $V_\circ$, ω, C and L for which i is constant for $t \geq 0$? If so, state the relation and determine i.

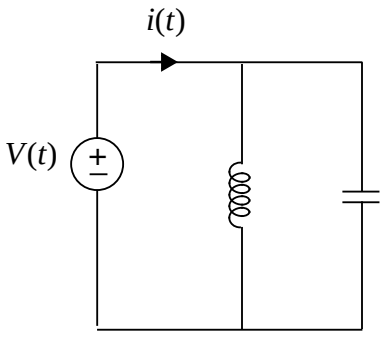


Figure 9.11:

Solution:

Problem 9.5 A constant voltage source having value V drives a time-varying capacitor as shown in Figure 9.12. The time-varying capacitance is given by $C(t) = C_0 + C_1 \sin(\omega t)$. Determine the capacitor current $i(t)$.

Solution:

Problem 9.6 A constant current source having value I drives a time-varying inductor as shown in Figure 9.13. The time-varying inductance is given by $L(t) = L_0 + L_1 \sin(\omega t)$. Determine the inductor voltage $v(t)$.

Solution:

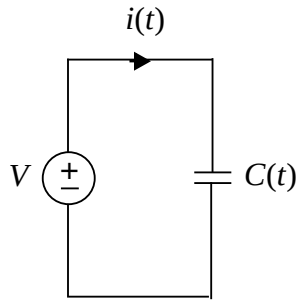


Figure 9.12:

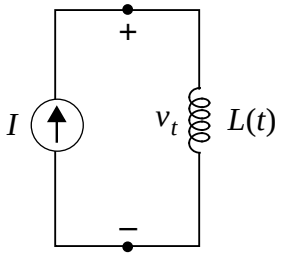


Figure 9.13:

Problem 9.7 Consider the parallel plate capacitor shown in Figure 9.14. Assume that the dielectric is free space so that $\epsilon = \epsilon_\circ$.

Suppose the capacitor is charged to the voltage V. Determine the charge and the electric energy stored in the capacitor in this case.

The capacitor is disconnected from the charging source so that its stored charge remains constant. Following that, its plates are pulled apart so as to double the distance between them; that is, the gap separation is now $2l$. For this new configuration, determine the voltage across the terminals of the capacitor and the energy stored in the capacitor. Explain how the stored energy changes.

Solution:

Problem 9.8 Figure 9.15 shows two capacitive two-port networks. One is a "Π" network, and one is a "T" network. For the Π network, find $i_{1\mathrm{P}}$ and $i_{2\mathrm{P}}$ as functions of $v_{1\mathrm{P}}$ and $v_{2\mathrm{P}}$. For the T network, find $i_{1\mathrm{T}}$ and $i_{2\mathrm{T}}$ as functions of $v_{1\mathrm{T}}$ and $v_{2\mathrm{T}}$.

How must $C_{1\mathrm{P}}$, $C_{2\mathrm{P}}$ and $C_{3\mathrm{P}}$ be related to $C_{1\mathrm{T}}$, $C_{2\mathrm{T}}$ and $C_{3\mathrm{T}}$ for both networks to have the same terminal relations?

Solution:

Problem 9.9 Figure 9.16 shows two inductive two-port networks. One is a "Π" network,

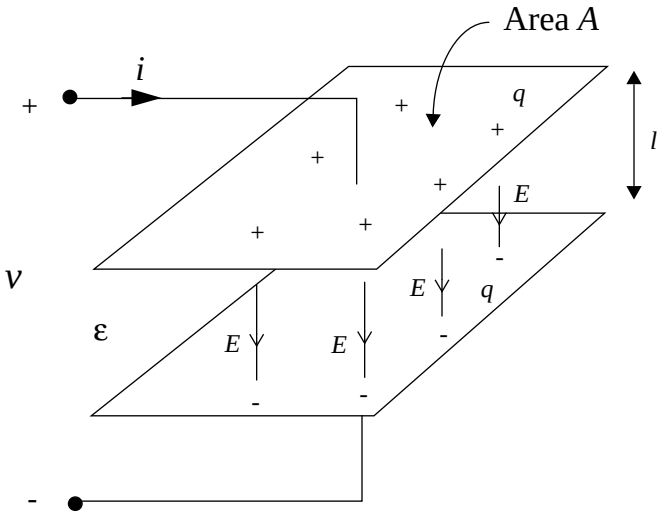


Figure 9.14:

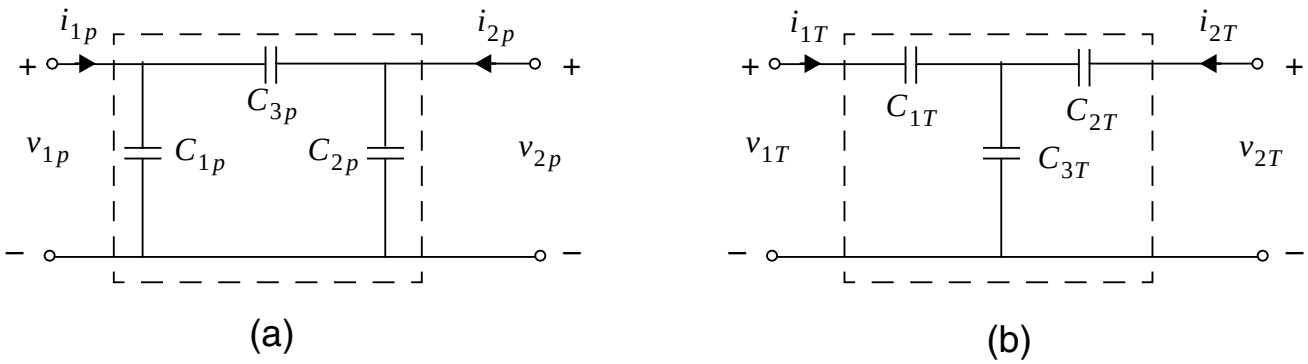


Figure 9.15: (a) a capacitive T two-port network, and (b) a capacitive Π two-port network

and one is a "T" network. For the Π network, find $v_{1\mathrm{P}}$ and $v_{2\mathrm{P}}$ as functions of $i_{1\mathrm{P}}$ and $i_{2\mathrm{P}}$. For the T network, find $v_{1\mathrm{T}}$ and $v_{2\mathrm{T}}$ as functions of $i_{1\mathrm{T}}$ and $i_{2\mathrm{T}}$.

How must $L_{1\mathrm{P}}$, $L_{2\mathrm{P}}$ and $L_{3\mathrm{P}}$ be related to $L_{1\mathrm{T}}$, $L_{2\mathrm{T}}$ and $L_{3\mathrm{T}}$ for both networks to have the same terminal relations?

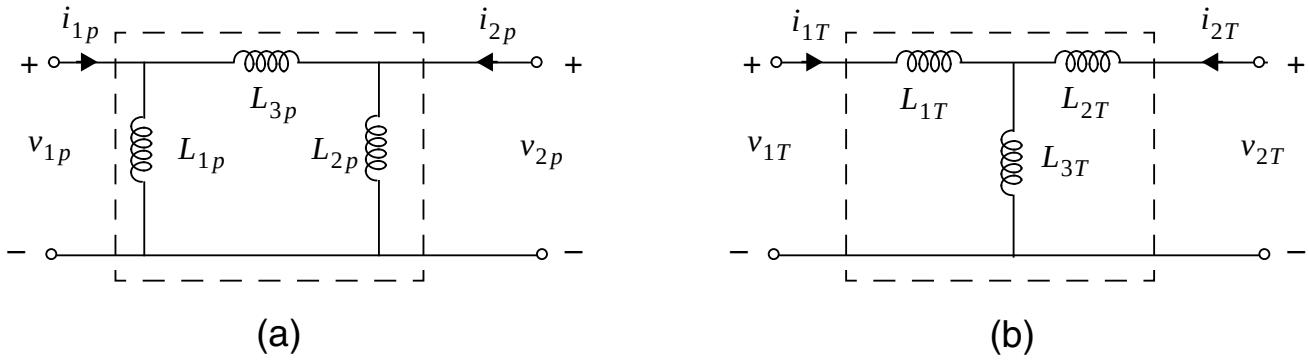


Figure 9.16: (a) an inductive T two-port network, and (b) an inductive Π two-port network

Solution:

Problem 9.10 This problem examines in more detail why energy is lost when the switch in Figure 9.17 closes. To do so, we examine the transient that occurs during the closure of the switch. In preparation for this, let $t = 0$ be the time at which the switch first begins to close, and let $t = T$ be the time at which the circuit reaches steady state. The charges on the two capacitors prior to switch closure are given to be Q_1 and Q_2.

Further, let $q_1(t)$ be any function defined over the interval $0 \leq t \leq T$ such that

$$q_1(0) = Q_1$$

and $q_1(T)$ is the steady state charge on the capacitor given by

$$q_1(T) = \frac{C_1}{C_1 + C_2}(Q_1 + Q_2)$$

In this way, the function q_1 is an arbitrary transient connecting the initial and final charge during the switch closure.

(a) Use the charge conservation relation

$$q_1(t) + q_2(t) = Q_1 + Q_2$$

to find q_2 in terms of q_1 for $0 \leq t \leq T$. Then, use the equation

$$\frac{dq(t)}{dt} = i(t)$$

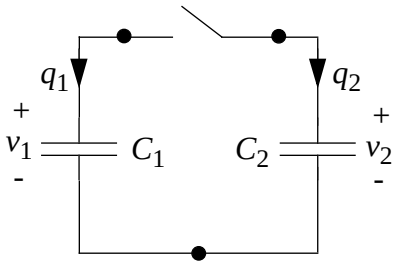


Figure 9.17:

to determine i_1 and i_2, again in terms of q_1 for $0 \leq t \leq T$. Finally, use the equation

$$q(t) = Cv(t)$$

to find v_1 and v_2, also in terms of q_1 for $0 \leq t \leq T$. The entire transient is now described in terms of the arbitrary function q_1.

(b) During the transient, the difference between v_1 and v_2 must appear across some element or elements within the circuit. KVL requires this. For example, it could appear across the wiring resistance or the switch, or a combination of both. In any case, energy is lost as a current passes through this voltage difference. If we consider the voltage difference to be $(v_1 - v_2)$, as opposed to its opposite, then it is i_2 that passes into the positive terminal of this difference. Why?

(c) The product $i_2(v_1 - v_2)$ is the power dissipated during the transient. Determine this power in terms of q_1 for $0 \leq t \leq T$.

(d) Integrate the power found in the previous part over the interval $0 \leq t \leq T$ to find the energy lost during the transient. Also, show that the energy lost is equal to the energy difference in

$$w_{\mathrm{E}}(t < 0) - w_{\mathrm{E}}(t > 0) = \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}\left(\frac{Q_1}{C_1} - \frac{Q_2}{C_2}\right)^2$$

Remarkably, the energy lost is independent of the interior details of the function chosen for q_1. Since these details are equivalent to the details of the loss mechanism, it is apparent that the amount of energy lost is independent of how it is lost.

Solution:

Chapter 10

First-order Transients

Exercises

Exercise 10.1 Using superposition, determine the current $i_1(t)$ for the network shown in Figure 10.1. The network is at rest for $t < 0$.

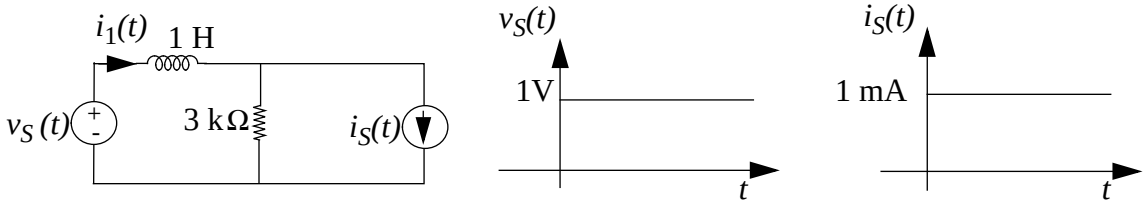


Figure 10.1:

Solution:

The inductor first acts as an open circuit and eventually becomes a wire:

$$t \geq 0 \begin{cases} \text{initially: } i_1(t) = 0 \text{ (open circuit)} \\ \text{finally: } i_1(t) = \frac{V_S(t)}{3k} + i_S(t) = \frac{4}{3} \text{ mA} \end{cases}$$

Assume $i_S(t)$ source points down.

$$i_1(t) = (Final\ Value) + (Initial\ Value - Final\ Value)\ e^{-t/\tau}$$

$$i_1(t) = 4/3\left(1 - e^{-t/\tau}\right)[mA]$$

$$\tau = L/R = 1/3ms$$

ANS:: $i_1(t) = \frac{4}{3}(1 - e^{t/\tau})mA$ for $t \geq 0$; $\tau = \frac{1}{3}ms$

Exercise 10.2 Find and sketch the zero state response for $t > 0$ in Figure 10.2. i_S is a 10 mA step at $t = 0$.

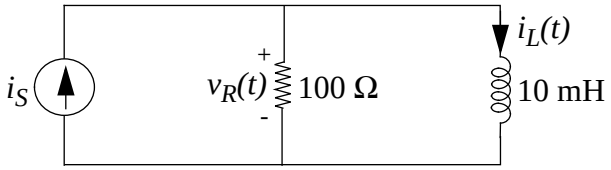


Figure 10.2:

Solution:

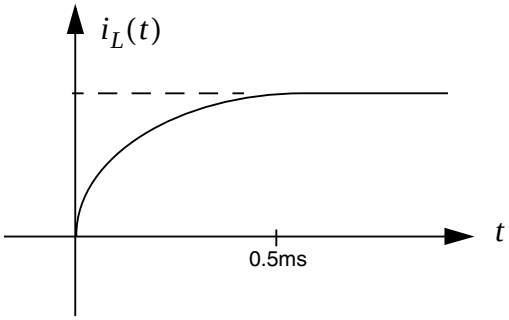


Figure 10.3:

$i_L(t) = 0$ initially

$I_S = 10mA$ finally

$$i_L(t) = 10\left(1 - e^{-t/\tau}\right)[mA]$$

$$\tau = L/R = 0.1ms$$

ANS:: $i_L(t) = 10e^{-t/\tau}mA$; $\tau = 0.1$ms

Exercise 10.3 In the circuit in Figure 10.4, $i(t) = 100$ μA, $0 < t < 1$ second, zero otherwise. At time $t = 2$, the voltage $v_C = 5$ volts. What is v_C at time $t = -1$ second?

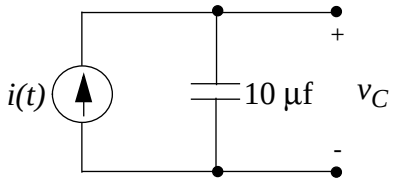


Figure 10.4:

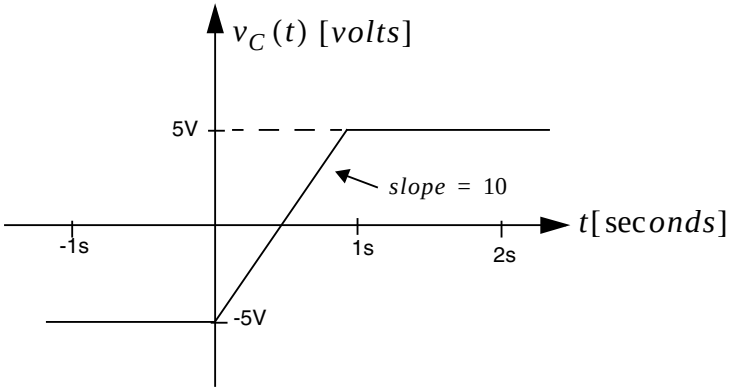


Figure 10.5:

Solution:

$$i_c = C \cdot \frac{dv_c}{dt}$$

$$v_c = \frac{\int i_c}{C} = 10t \quad \text{for} \quad 0 < t < 1 \; second$$

$$v_c = \frac{\int i_c}{C} = \text{ a constant, otherwise, when } i_c = 0$$

Therefore,

$$v_c(t = -1 \text{ second}) = -5V$$

ANS:: -5 volts

Exercise 10.4 In the circuit in Figure 10.6, the switch is closed at time $t = 0$ and opened at $t = 1$ second. Sketch $v_C(t)$ for all times.

Solution:

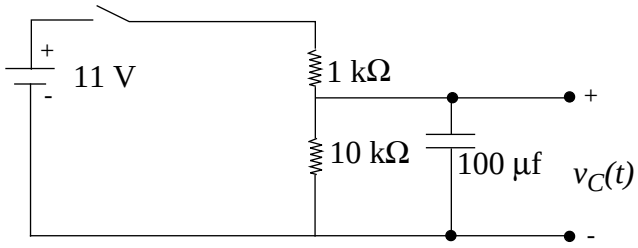


Figure 10.6:

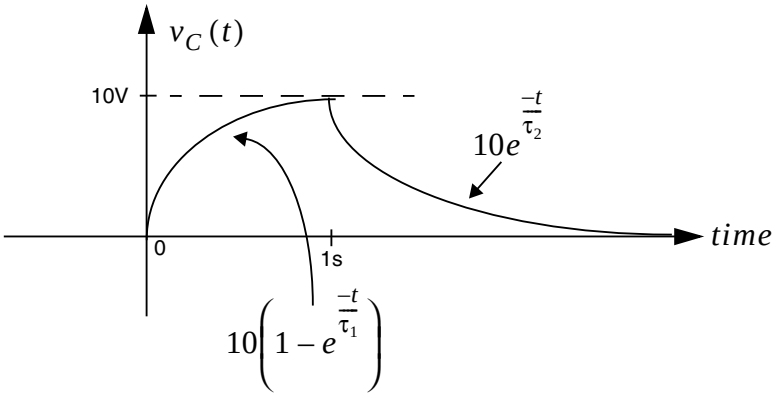


Figure 10.7:

Assume $v_C = 0$ for $t < 0$. When the switch is closed at $t = 0$, v_C rises from 0 to

$$11 \cdot \frac{10k}{10k + 1k} = 10 \text{ Volts} \quad \text{with } \tau_1 = [1k \,||\, 10k] \cdot C$$

$$\tau_1 = 9.09ms$$

When the switch is opened, v_C falls exponentially back to zero with $\tau_2 = 10k \cdot C = 1\ second$

Assuming $v_C = 0$ for $t < 0$, when the switch is closed at $t = 0$, v_C rises from 0 to 10V with $\tau_1 = \tau_1 = 9.09ms$; When the switch is opened, v_C falls exponentially back to zero with $\tau_2 = 1$ second.

Exercise 10.5 Find and sketch the zero-input response for $t > 0$ in each network in Figure 10.8 for the given initial conditions.

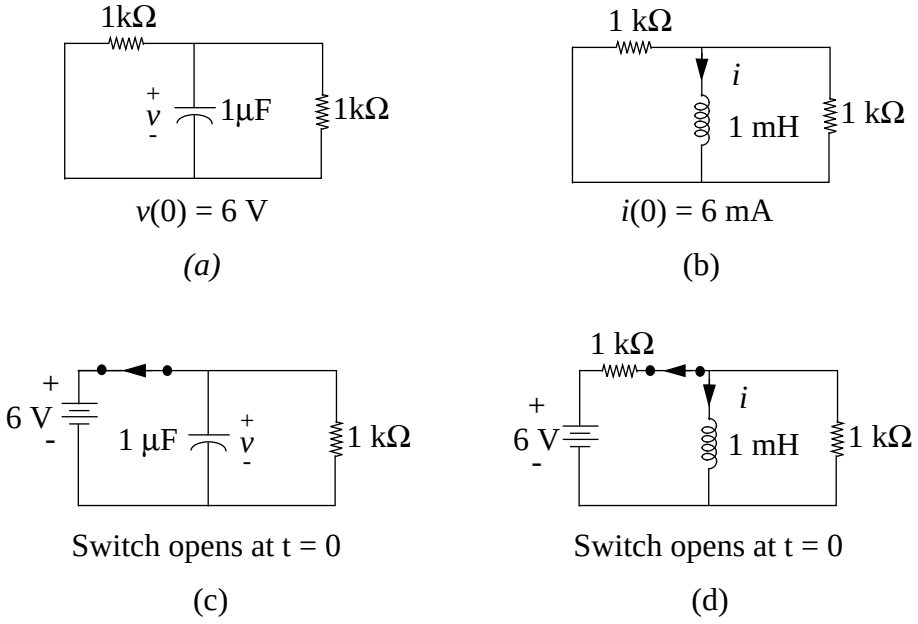


Figure 10.8:

Solution:

(a)

$\tau = [1k \,||\, 1k] \cdot C = 500\mu s$

$v = 6e^{-t/\tau}$

(b)

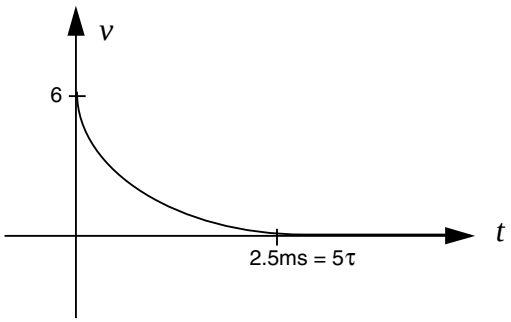


Figure 10.9:

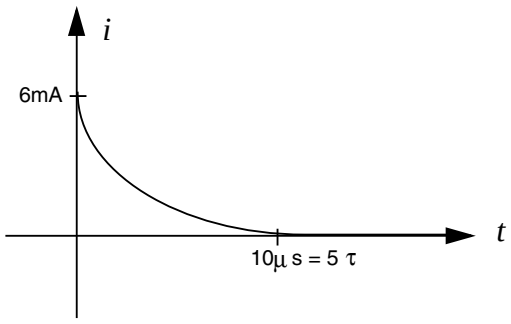


Figure 10.10:

$\tau = L/(1k \mid\mid 1k) = 2\mu s$

$i = (6 \cdot 10^{-3})e^{-t/\tau}$

(c)

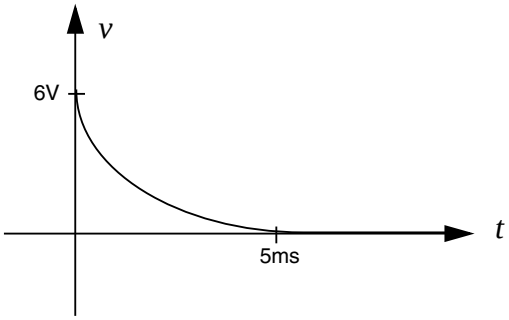


Figure 10.11:

$v(0) = 6$

$\tau = R \cdot C = (1k\Omega)(1\mu F) = 1ms$

$v = 6e^{-t/\tau}$

(d)

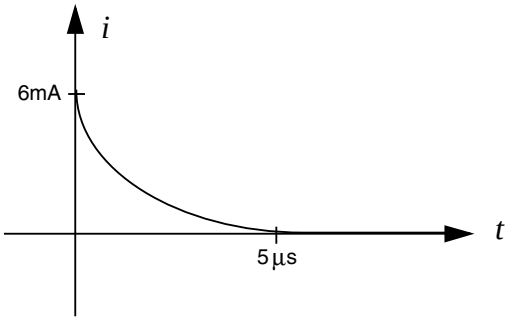


Figure 10.12:

$i(0) = \frac{(6V-0)}{1000\Omega} = 6mA$

$\tau = L/1k = 1\mu s$

$i = 0.006e^{-t/\tau}$

ANS:: (a) $v = 6e^{-t/\tau}$, $\tau = 500\mu s$ (b) $i = (6 \times 10^{-3})e^{-t/\tau}$, $\tau = 2\mu s$ (c) $v = 6e^{-t/\tau}$, $\tau = 1ms$ (e) $i = (6 \times 10^{-3})e^{-t/\tau}$, $\tau = 1\mu s$

Exercise 10.6 Find and sketch the response for $t > 0$ in each network in Figure 10.13. Assume that the input is as shown for $t > 0$, and assume an initial zero state (in other words, show the zero state response).

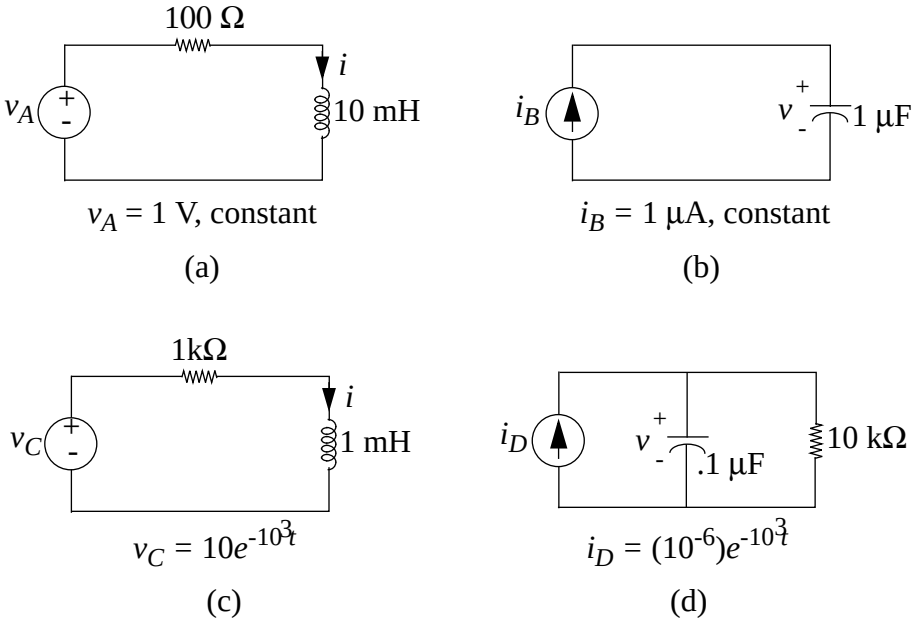


Figure 10.13:

Solution:

(a)

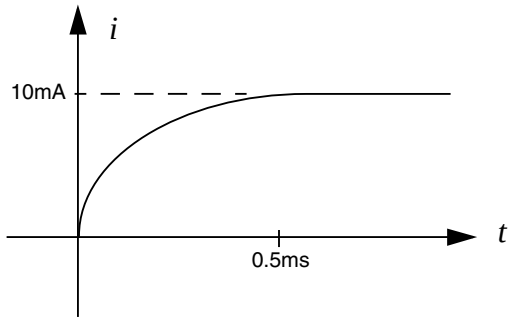


Figure 10.14:

i:

final value: $\frac{V_A}{100\Omega} = 10mA$

initial value: 0

$i = 10mA(1 - e^{-t/\tau})$

$\tau = L/R = 0.1ms$

(b)

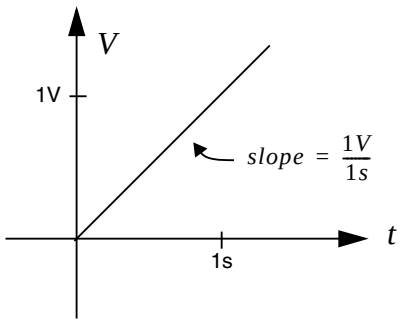


Figure 10.15:

$i_B = 1\mu A = C\frac{dv}{dt}$

$V = \int \frac{1\mu A}{C} \cdot dt = t$

(c)

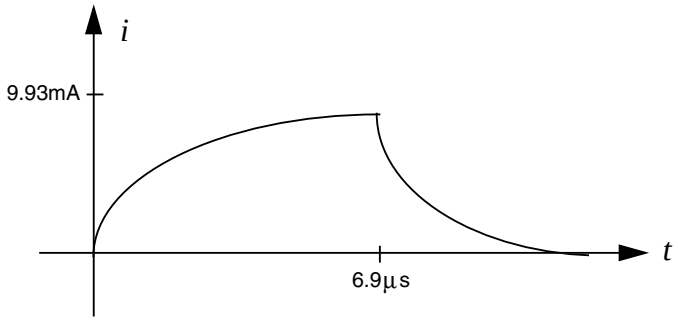


Figure 10.16:

$v_C - 1000i - L \cdot \frac{di}{dt} = 0$

(1) $1000v_C = 10^4\ e^{-1000t} = 10^6 i + \frac{di}{dt} \quad \Rightarrow \quad i = i_{homogeneous} + i_{particular}$

$i_{homogeneous} = Ae^{-10^6 t}$

Assume $i_{particular}$ in the form $= i_{particular} = Be^{-1000t}$

$\frac{di_{particular}}{dt} = -1000B\ e^{-1000t}$

Now plug $i_{particular}$ into (1): $B = 10/999$

Now use the initial condition $i(0) = 0$ to find A:

$$i = A\ e^{-106t} + \frac{10}{999}e^{-1000t} = 0 \text{ when } t = 0 \quad \Rightarrow \quad A = -\frac{10}{999}$$

$$i = \frac{10}{999}\left(e^{-1000t} - e^{-10^6 \cdot t}\right)$$

(d)

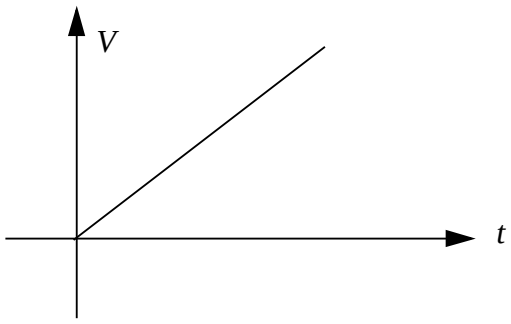


Figure 10.17:

$$10^{-6}\ e^{-1000t} = C\frac{dv}{dt} + \frac{v}{10k}$$

$$10e^{-1000t} = 1000V + \frac{dv}{dt}$$

$$v = \underbrace{A\ e^{-1000t}}_{\text{homo- geneous solution}} + \underbrace{B \cdot t \cdot e^{-1000t}}_{\text{particular solution}}$$

t factor included since forcing τ = homogeneous τ

Plug in particular solution to find $B = 10$. If $v(0) = 0$, then $A = 0$.

$$v = 10 \cdot t\ e{-}1000t$$

ANS:: (a) $i = (10^{-2})\left(1 - e^{-10^4 t}\right)$ (b) $v = Kt$ where $K = 1V/s$ (c) $i = \frac{10}{999}\left(e^{-10^3 t} - e^{-10^6 t}\right)$ (d) $v = 10te^{-10^3 t}$

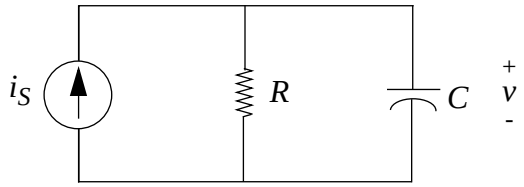


Figure 10.18:

Exercise 10.7 For the current source shown in Figure 10.18, assume i_S consists of a single rectangular current pulse of amplitude I_0 amps and duration t_0 seconds.

a) Find the zero-state response to i_S.

b) Sketch the zero-state response for the cases:

i) $t_0 >> RC$

ii) $t_0 = RC$

iii) $t_0 << RC$

c) Show that for $t_0 << RC$, (the case of a short pulse), the response for $t > t_0$ depends only on the area of the pulse $(I_0 t_0)$, and not on i_0 or t_0 separately.

Solution:

a) v: final value resulting from pulse $= I_0 \cdot R$

initial value $= 0$ (assumed zero state)

$\underline{0 < t < t_0 : v = I_0 \cdot R\,(1 - e^{-t/\tau})\,;\tau = RC}$

When the pulse stops (at $t_0 = t$), exponential decay occurs in v,
with the initial value $= I_0 \cdot R\,(1 - e^{-t_0/RC})$ and final value $= 0$.

$\underline{t > t_0 : v = I_0 \cdot R\,(1 - e^{-t_0/RC})\,e^{-(t-t_0)/RC}}$

b) i) $t_0 >> RC$

For $t_0 \gg RC$, v reaches max value since the pulse is sufficiently long.

ii) $t_0 = RC$

$t_0 = RC$: Here the pulse is not long enough for v to exponentially rise all the way to $I_0 \cdot R$. V only reaches 63% of its maximum before decaying.

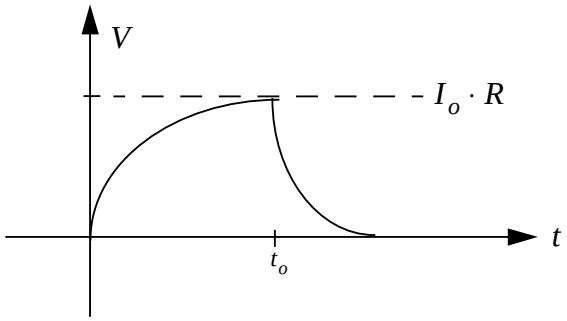


Figure 10.19:

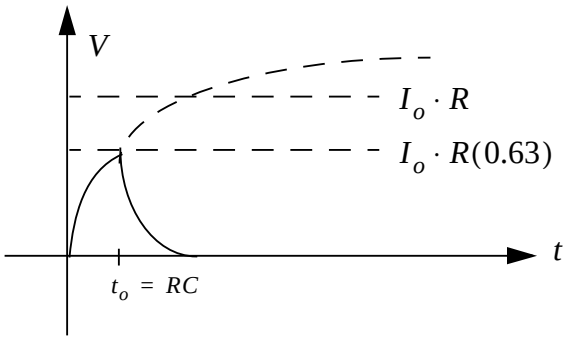


Figure 10.20:

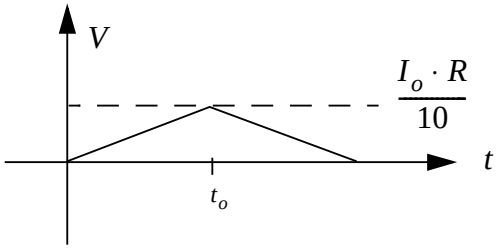


Figure 10.21:

iii) $t_0 << RC$

Here the exponential rise is very short, since the pulse is short

c) In case (iii), we see the output v for a constant pulse input is triangular, or ramped; nearly the integral of the input, i.e. proportional to the area under the input curve.

$i = v/R + C\ \frac{dv}{dt}$

$I_0 \cdot R = v + RC\ \frac{dv}{dt}$

$\frac{I_0}{C} = \frac{v}{RC} + \frac{dv}{dt}$

As RC becomes larger ($\gg t_0$), our equation can be approximated as

$$\frac{dv}{dt} = \frac{I_0}{C} \quad \Rightarrow \quad v = \int_0^{t_0} I_0/C$$

since $v/RC \to 0$ when RC is large.

ANS:: (a) For $0 \leq t \leq t_0$, $v = RI_0\left(1 - e^{-t/RC}\right)$, and for $t > t_0$, $v = RI_0\left(1 - e^{-t_0/RC}\right)e^{-(t-t_0)/RC}$

Exercise 10.8 Identify the state variable in each network in Figure 10.22. Write the corresponding state equation and find the time constants.

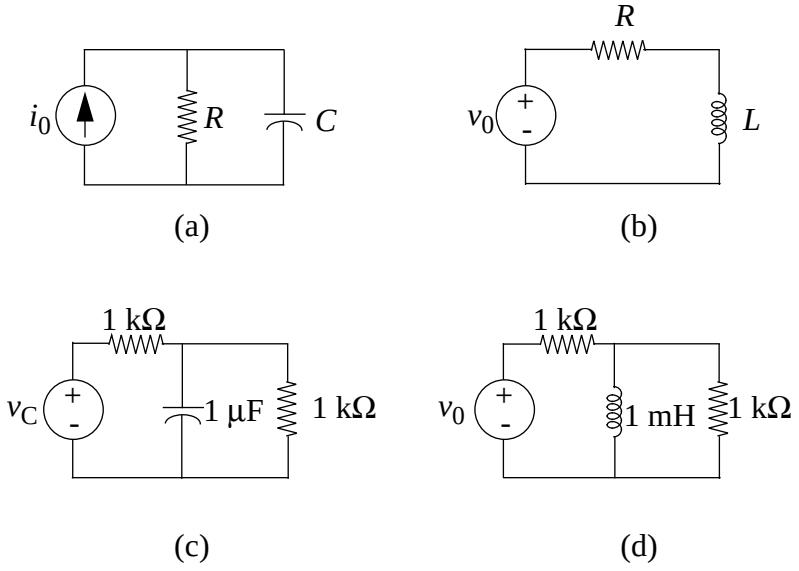


Figure 10.22:

Solution:

(a)

$$i_0 = V/R + C\frac{dV}{dt}$$

State variable: V

Time constant: RC

(b)

$$v_0 = i \cdot R + L\frac{di}{dt}$$

State variable: i

Time constant: L/R

(c)

$$\frac{v_0 - v_C}{1000} = C\,\frac{dv_C}{dt} + \frac{v_C}{1000}$$

State variable: v_C

Time constant: $500\mu s$

(d)

$$\frac{v_0 - v_L}{1000} = i_L + \frac{v_L}{1000}$$

or,

$$\frac{v_0}{1000} = \frac{2L}{1000}\frac{di_L}{dt} + i_L$$

State variable: i_L

Time constant: $2\mu s$

ANS:: (a) V, time constant RC (b) i, time constant L/R (c) v_C, time constant 500 μs (d) i_L, time constant 2μs

Exercise 10.9 In the circuit in Figure 10.23, $v(t) = 5$mV for $0 < t < 1$ seconds, and zero otherwise. At time $t = 4$ seconds, $i(t) = 7$A. What is $i(t)$ at time $t = -1$ second?

Solution:

When $0 < t < 1$,

$$v_L = L \cdot \frac{di}{dt}$$

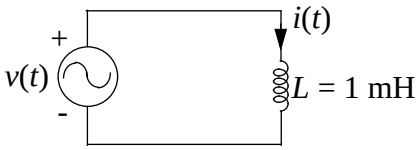


Figure 10.23:

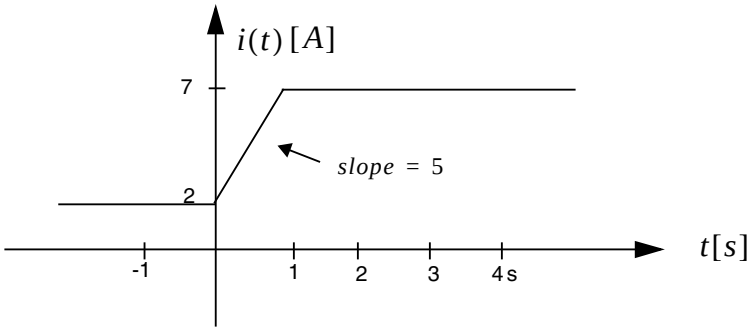


Figure 10.24:

$$i = \int \frac{v_L}{L} = 5 \cdot t$$

Graphically,

$$i(-1) = 2A$$

ANS:: 2A

Exercise 10.10 Identify appropriate state variables for the network in Figure 10.25 and write the state equations.

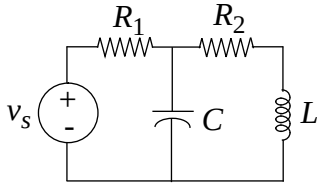


Figure 10.25:

Solution:

State variables: i_L, v_C

$$\frac{V_S - v_C}{R_1} + \frac{v_L - v_C}{R_2} - C\,\frac{dv_C}{dt} = 0$$

$$v_C - i_L\, R_2 - v_L = 0$$
$$\frac{dv_C}{dt} - v_L \cdot \frac{R_2}{L} - \frac{dv_L}{dt} = 0$$

ANS:: State variables i_L, v_C. State equations: $\frac{V_S - v_C}{R_1} + \frac{v_L - v_C}{R_2} - C\ \frac{dv_C}{dt} = 0$, and $\frac{dv_C}{dt} - v_L \cdot \frac{R_2}{L} - \frac{dv_L}{dt} = 0$

Exercise 10.11 In Figure 10.26, $R_1 = 1k\Omega$, $R_2 = 2k\Omega$, $C = 10\mu F$. The driving voltage $v_S = 0$ for $t < 0$. Assume v_S is a 3-volt step at $t = 0$. Make a sketch of $v_C(t)$ for $t > 0$. Be sure to label the dimensions of the voltage and time axes and identify characteristic waveform shapes with suitable expressions.

$$v_S = \begin{cases} 0, (t < 0) \\ 3\ \text{V}, (t \geq 0) \end{cases}$$

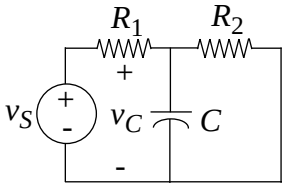


Figure 10.26:

Solution:

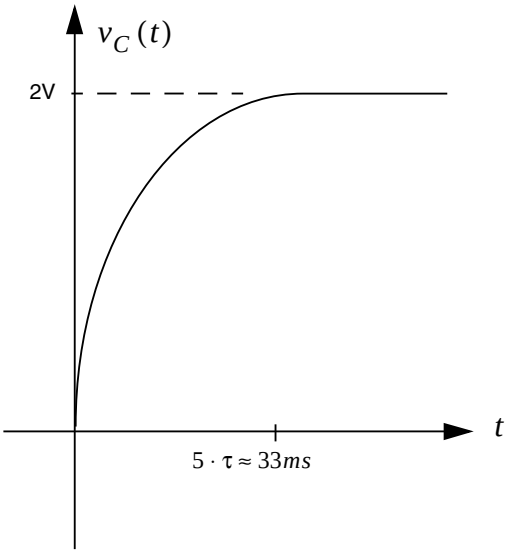


Figure 10.27:

$$\tau = [R_1 \,||\, R_2] \cdot C = \frac{20}{3} ms$$

v_C: final value

$$v_C = 3 \cdot \frac{R_2}{R_1 + R_2} = 2V$$

Initial value $= 0$

$$v_C = 2\left(1 - e^{-t/\tau}\right)$$

$$\tau = \frac{20}{3} ms$$

ANS:: $v_C = 2\left(1 - e^{-t/\tau}\right)$, for $\tau = \frac{20}{3}$ms

Exercise 10.12 Identify state variables and write appropriate state equations for the circuit in Figure 10.28.

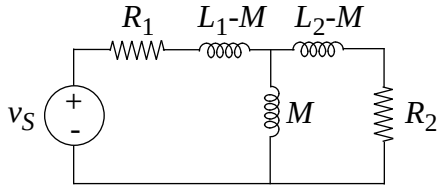


Figure 10.28:

Solution:

State variables: i_{L1}, i_{L2}, i_M

(1)

$$i_{L1} + i_{L2} = i_M$$

(2)

$$V_M = V_{L1} + i_{L1} \cdot R_1 - V_S = 0$$

$$M\frac{di_M}{dt} = (L_1 - M)\frac{di_{L1}}{dt} + i_{L1} \cdot R_1 - V_S = 0$$

(3)

$$V_M = V_{L2} + i_{L2} \cdot R_2 = 0$$

$$M\frac{di_M}{dt} = (L_2 - M)\frac{di_{L2}}{dt} + i_{L2} \cdot R_2 = 0$$

ANS:: State variables: i_{L1}, i_{L2}, i_M. State equations: (1) $i_{L1} + i_{L2} = i_M$, (2) $M\frac{di_M}{dt} = (L_1 - M)\frac{di_{L1}}{dt} + i_{L1} \cdot R_1 - V_S = 0$, (3) $M\frac{di_M}{dt} = (L_2 - M)\frac{di_{L2}}{dt} + i_{L2} \cdot R_2 = 0$

Exercise 10.13 Referring to Figure 10.29, before the switch is closed, the capacitor is charged to a voltage $v_C = 2$ volts. The switch is closed at $t = 0$. Find an expression for $v_C(t)$ for $t > 0$. Sketch $v_C(t)$.

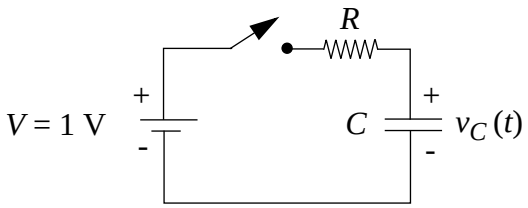


Figure 10.29:

Solution:

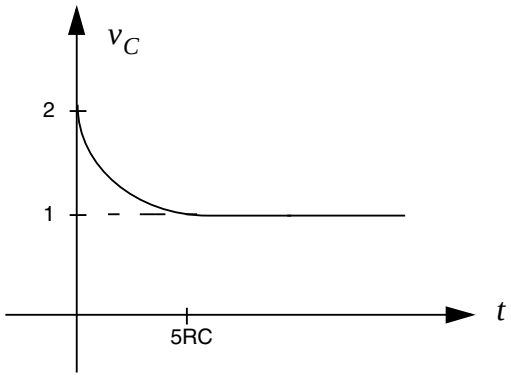


Figure 10.30:

$$\tau = R \cdot C$$

v_C:

$$initial\ value = 2V$$

$$final\ value = 1V$$

$$v_C = final\ value + (initial\ value - final\ value)\ e^{-t/\tau} = 1 + e^{-t/\tau}$$

ANS:: $v_C = 1 + e^{-t/\tau}$

Exercise 10.14 Find the time constant of the circuit shown in Figure 10.31.

Solution:

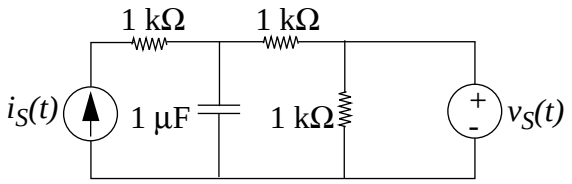


Figure 10.31:

Use the Thévenin Equivalent taken about the capacitor terminals to find R_{TH}.

Time constant $= \tau = R_{TH} \cdot C$

$$R_{TH} = 1000$$

$$\tau = 1000 \cdot C$$

$$\tau = 1ms$$

ANS:: $\tau = 1ms$

Exercise 10.15 A two-input RC circuit is shown in Figure 10.32. (Parts a, b, and c are independent questions).

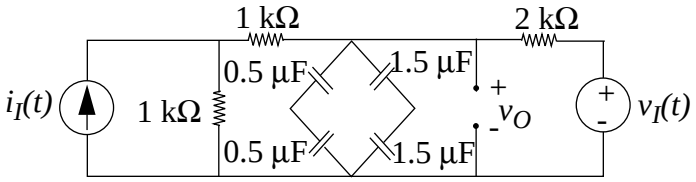


Figure 10.32:

a) You should realize that the "bridge" of capacitors can be replaced by a single capacitor in this problem. What is the value of the single equivalent capacitor?

b) Consider operation with $i_I(t) = 0$ and $v_I(t) = 0$ for $t \geq 0$. The voltage $v_O(t)$ is known to be 1 volt at a time $t = 0$. Determine $v_O(t)$ for all $t > 0$.

c) A different constraint is that sources $i_I(t)$ and $v_I(t)$ are zero for $t < 0$ and that $v_O(0) = 0$. Sources $i_I(t)$ and $v_I(t)$ undergo step transitions of +1 mA and +1 volt respectively at time $t = 0$. Determine $v_O(t)$ for all time.

Solution:

a) $C_{EQ} = 1/4\ \mu F + 3/4\ \mu F = 1\mu F$

b) $v_0(t) = 1 \cdot e^{-t/\tau}$

$\tau = 1ms$

c) $v_0(t) = 0$ for $t < 0$

$v_0(t) = 1mA\ \left(\frac{1}{4}\right)(2k\Omega) + 1V\left(\frac{1}{2}\right) = 1Volt$, final value

$v_0(t) = (1 - e^{-t/\tau})$; $\tau = 1ms$, for $t > 0$

ANS:: (a) $C_{EQ} = 1\mu F$ (b) $\tau = 1ms$, $v_0(t) = 1 \cdot e^{-t/\tau}$ (c) $v_0(t) = (1 - e^{-t/\tau})$; $\tau = 1ms$, for $t > 0$

Exercise 10.16 In the circuit in Figure 10.33, $R_1 = 1k\Omega$, $R_2 = 2k\Omega$, and $C = 3\mu F$. Assume initial rest conditions (zero initial state), and assume that v_1 has a 6-volt step at $t = 0$. Find $v_2(t)$ for $t > 0$. Sketch and label.

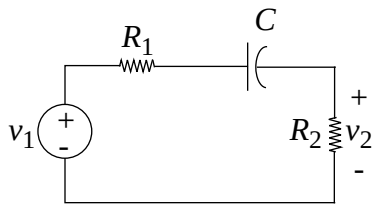


Figure 10.33:

Solution:

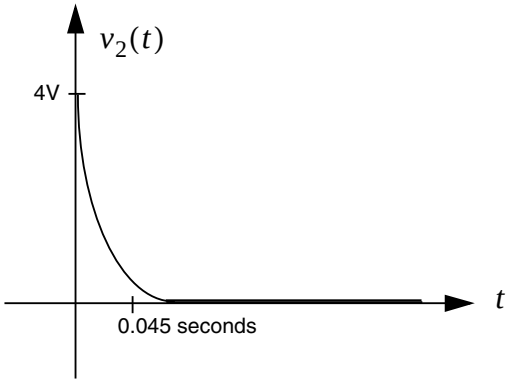


Figure 10.34:

v_2: initially $= \frac{R_2}{R_1+R_2} \cdot 6V = 4V$

finally $= 0$

$\tau = (2k + 1k)\ 3\mu F = 9ms$

$v_2(t) = 4\ e^{-t/\tau}\ ;\ \tau = 9ms\ ,\ t > 0$

ANS:: $v_2(t) = 4\ e^{-t/\tau}\ ;\ \tau = 9ms\ ,\ t > 0$

Exercise 10.17 Consider the circuit shown in Figure 10.35. Sketch and label $v_O(t)$ for $i_1(t)$ a step as shown in Figure 10.36. Assume $v_O = 0$ for $t < 0$.

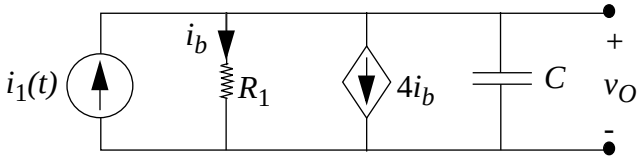


Figure 10.35:

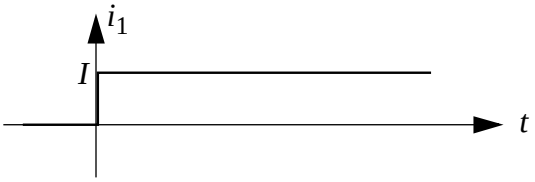


Figure 10.36:

Solution:

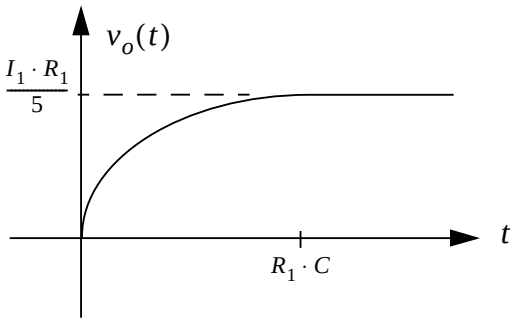


Figure 10.37:

v_0: initially $= 0$

finally $= i_0 \cdot R_1 = \frac{I_1 R_1}{5}$

$v_0(t) = \frac{I_1 R_1}{5}(1 - e^{-t/\tau})$

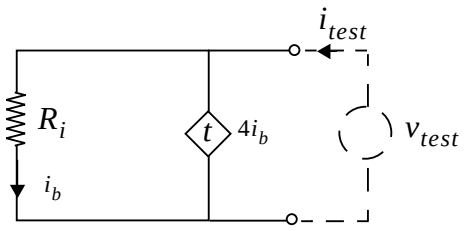


Figure 10.38:

$\tau = R_{EQ} \cdot C = \frac{R_1 C}{5}$
$R_{EQ} = \frac{V_{test}}{i_{test}} \Rightarrow$
$i_b = \frac{V_{test}}{R_1}$
$i_{test} - 4\left(\frac{V_{test}}{R_1}\right) - \frac{V_{test}}{R_1} = 0$
$R_{EQ} = \frac{R_1}{5}$

ANS:: $v_0(t) = \frac{I_1 R_1}{5}(1 - e^{-t/\tau})$, $\tau = \frac{R_1 C}{5}$

Exercise 10.18 For the circuit shown in Figure 10.39, find the characteristic equation and the zero-input response assuming that the capacitor was initially charged to 1 volt. Label your graph.

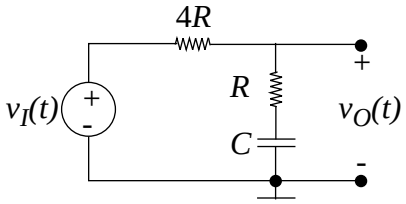


Figure 10.39:

Solution:

*Characteristic equation:

$$v_i = v_C + 5RC \cdot \frac{dv_C}{dt}$$

*zero input

$v_0(t)$: initially $= 1Volt$

finally $= 0$

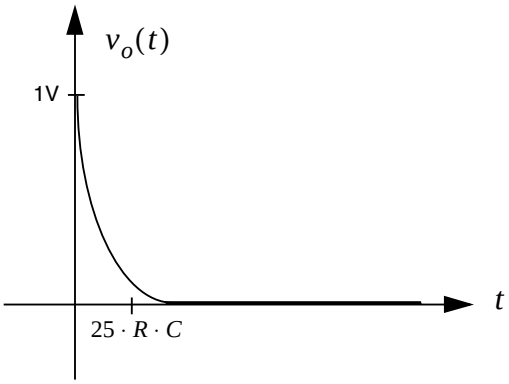


Figure 10.40:

$\tau = 5RC$

ANS:: $v_i = v_C + 5RC \cdot \frac{dv_C}{dt}$, $v_0(t)$ initially 1V, finally 0V, time constant $5RC$

Exercise 10.19 The excitation function for all four of the circuits shown in Figure 10.41 is:

$$\begin{array}{rcll} v_S(t) & = & 0, & t < 0 \\ v_S(t) & = & 10 \text{ volts}, & t \geq 0 \end{array}$$

For each of the circuits, select the time function on the right that corresponds in magnitude and shape to the output, $v_O(t)$. Assume that all capacitors and inductors have zero initial states, (the appropriate state variable is zero for t less than zero). In no matching response exists, say so and explain briefly. All responses are made up of "straight lines" and "exponentials". You may choose a time function more than once. (Note that part (d) shows an op-amp circuit. Op-amps will be covered in later chapters).

Solution:

(A) $\rightarrow$ $v_0(t) = 10V(1 - e^{-t/\tau})$; $\tau = R \cdot C$

(B) $\rightarrow$ $v_0(t) = 10V\left(\frac{R}{R+R}\right)(1 - e^{-}t/\tau)$; $\tau = R \cdot C$

(C) $\rightarrow$ $v_0(t)$: finally $= 10V$; initially $= 0$

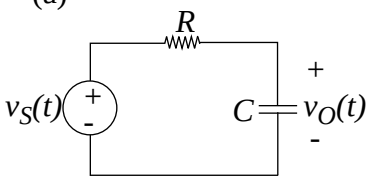
$v_0(t) = 10(1 - e^{-t/\tau})$; $\tau = L/R$

(D) $\rightarrow$ $\frac{V_S}{R} + C\,\frac{dV_0}{dt} = 0 \;\Rightarrow\; V_0 = \frac{-10}{RC} \cdot t$, within the linear region of the op. amp.

Therefore,

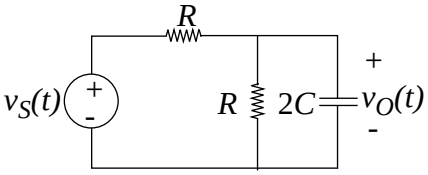
(A) 3

(a)



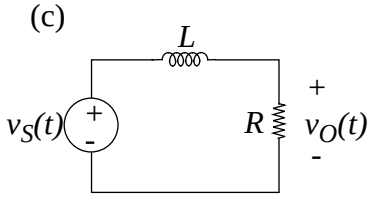
Response number _____

(b)



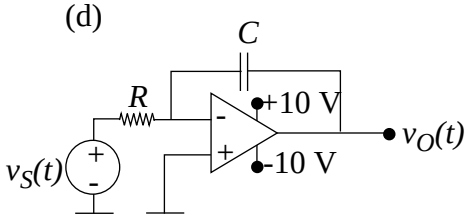
Response number _____

(c)



Response number _____

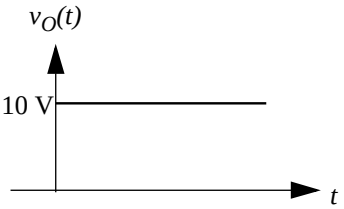
(d)



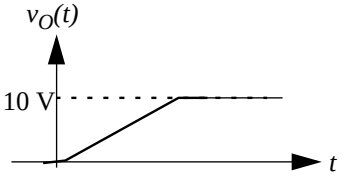
Op-amp saturation at ±10 V

Response number _____

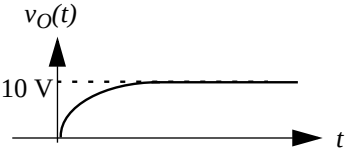
(1)



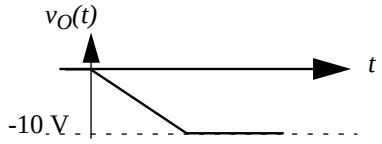
(2)



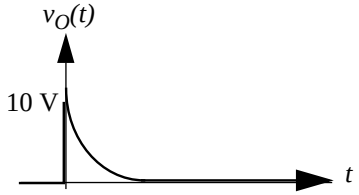
(3)



(4)



(5)



(6)

(7)

(8)

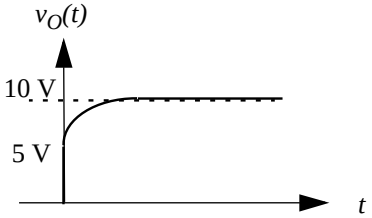


Figure 10.41:

(B) 7

(C) 3

(D) 4

ANS:: (A) $v_0(t) = 10V(1 - e^{-t/\tau})$; $\tau = R \cdot C$, (B) $v_0(t) = 10V\left(\frac{R}{R+R}\right)(1 - e^{-}t/\tau)$; $\tau = R \cdot C$, (C) $v_0(t) = 10(1 - e^{-t/\tau})$; $\tau = L/R$, (D) $v_0 = \frac{-10}{RC}t$

Exercise 10.20 An RC network is shown in Figure 10.42. The voltage v and the current i are constant for all time. Prior to $t = 0$, the circuit is in equilibrium with the switch closed. At time $t = 0$, the switch is opened, and it is then closed some time later. The waveform in Figure 10.43 is observed for $v_C(t)$.

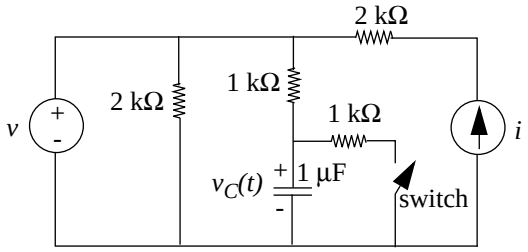


Figure 10.42:

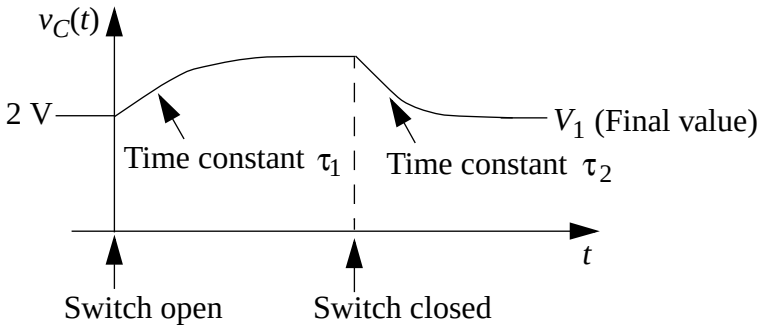


Figure 10.43:

What are the value of τ_1, τ_2, and the final value V_1? NOTE: The figure may not be to scale.

Solution:

$\tau_1 = 1ms$

$\tau_2 = 1/2ms$

$V_1(final\ value) = 2Volts$

ANS:: $\tau_1 = 1ms$, $\tau_2 = 1/2ms$, $V_1(final\ value) = 2Volts$

Exercise 10.21 In the two following cases in Figure 10.44 the input $v_{IN}(t) = 10u_{-1}(t)$, a 10 volt step[1] starting at time $t = 0$. Give for each case

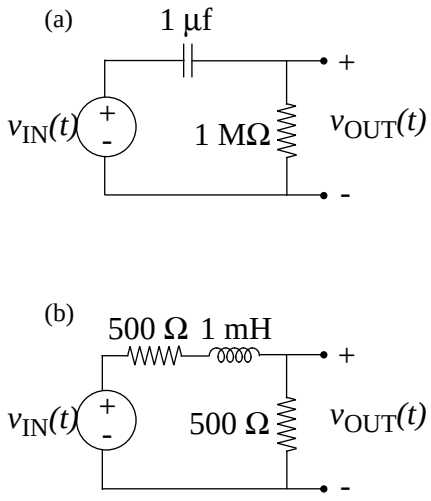


Figure 10.44:

a) The time constant of the circuit.

b) an analytic expression for the signal $v_{OUT}(t)$ as a function of time.

c) A labeled sketch of the output signal $v_{OUT}(t)$ as a function of time. Be sure to label the time and voltage scales.

Solution:

a) (i) $\tau = (1M\Omega)(1\mu F) = 1second$
(ii) $v_0 = 10\ e^{-t/\tau}$; $\tau = 1second$

b) (i) $\tau = 1\mu s$
(ii) $v_{out}(t) = 5\ (1 - e^{-t/\tau})$; $\tau = 1\mu s$

c) See Figures 10.45 and 10.46.

[1] Recall that the notation $u_0(t)$ represents an impulse at time t. The notation $u_n(t)$ represents the function that results from differentiating the impulse n times, and the notation $u_{-n}(t)$ represents the function that results from integrating the impulse n times. Thus $u_{-1}(t)$ represents the unit step at time t, $u_{-2}(t)$ the ramp, and $u_1(t)$ the doublet at time t. The unit step $u_{-1}(t)$ is also commonly represented as $u(t)$, and the unit impulse $u_0(t)$ as $\delta(t)$.

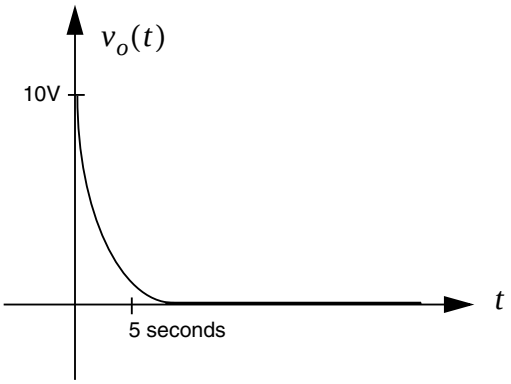


Figure 10.45:

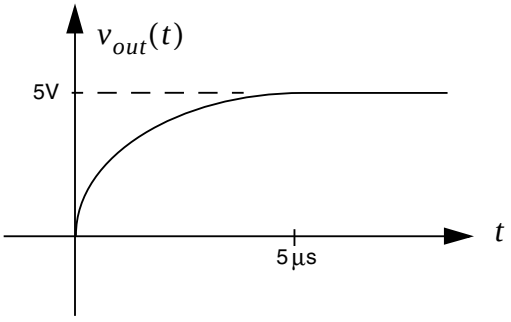


Figure 10.46:

ANS:: (a) (i) $\tau = 1second$ (ii) $v_0 = 10e^{-t/\tau}$; $\tau = 1second$ (b) (i) $\tau = 1\mu s$ (ii) $v_0(t) = 5\ (1 - e^{-t/\tau})$; $\tau = 1\mu s$

Exercise 10.22 In each of the following cases, find by inspection and give

i) an expression for the time constant τ,

ii) a sketch of the signal versus time,

iii) an analytic expression for the signal in terms of τ and any other necessary parameters.

a) Referring to Figure 10.47, find $v(t)$ for $t > 0$ given $i(t = 0) = I_0$.

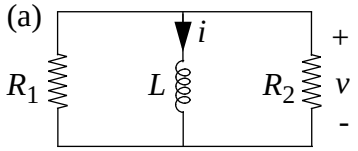


Figure 10.47:

b) Referring to Figure 10.48, find $i_2(t)$ given $i_1(t = 0) = I_0/2$.

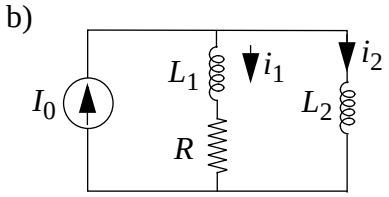


Figure 10.48:

c) Referring to Figure 10.49, find $v(t)$ for $t > 0$ given that the switch is moved from 1 to 2 at $t = 0$.

Solution:

a) $v_0(t) = -\frac{R_1 R_2 I_0}{R_1 + R_2}(e^{-t/\tau})$

$\tau = \frac{L}{R_1 \,||\, R_2}$

c)

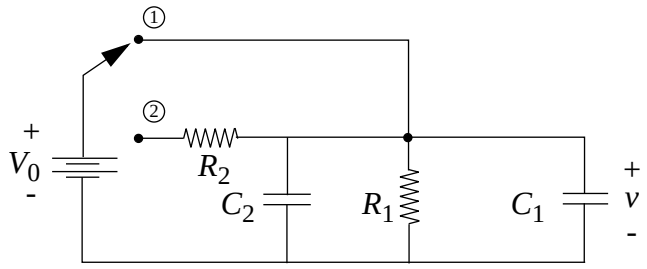


Figure 10.49:

b) (1) $I_o = i_1 + i_2$

(2) $i_1 R + L_1 \frac{di_1}{dt} = L_2 \frac{di_2}{dt}$

So, $i_1(t) = \frac{I_o}{2} e^{-\frac{R}{L_1+L_2}t}$, since $i_1(t=0) = \frac{I_o}{2}$.

From (1), $i_2 = I_o - i_1 \qquad \rightarrow \qquad i_2 I_o - \frac{I_o}{2} e^{-\frac{R}{L_1+L_2}t}$

$$\tau = \frac{L_1 + L_2}{R}$$

c) $\frac{V-V_o}{R_2} + \frac{v}{R_1} + C_1 \frac{dv}{dt} + C_2 \frac{dv}{dt} = 0$

Homogeneous solution:

$$v_H = Ae^{-t/\tau}, \quad \tau = \frac{R_1 + R_2}{(C_1 + C_2) R_1 R_2}$$

Particular solution:

$$v_P = \frac{V_o R_1}{R_1 + R_2}$$

Apply initial condition: $v(t=0) = V_o,$ then

$$v = v_H + v_P = \frac{V_o}{R_1 + R_2} \left(R_1 + R_2 e^{-t/\tau} \right); \quad \tau = \frac{R_1 + R_2}{(C_1 + C_2) R_1 R_2}$$

ANS:: (a) $v_0(t) = -\frac{R_1 R_2 I_0}{R_1 + R_2}(e^{-t/\tau}), \tau = \frac{L}{R_1 \,||\, R_2}$ (b) $i_2 = I_o - \frac{I_o}{2} e^{-\frac{R}{L_1+L_2}t}, \tau = \frac{L_1+L_2}{R}$
(c) $v = \frac{V_o}{R_1+R_2} \left(R_1 + R_2 e^{-t/\tau} \right); \quad \tau = \frac{R_1+R_2}{(C_1+C_2)R_1 R_2}$

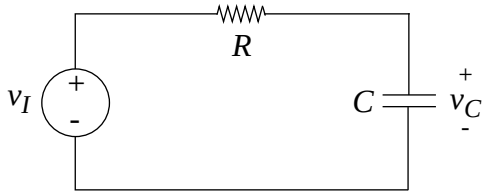


Figure 10.50:

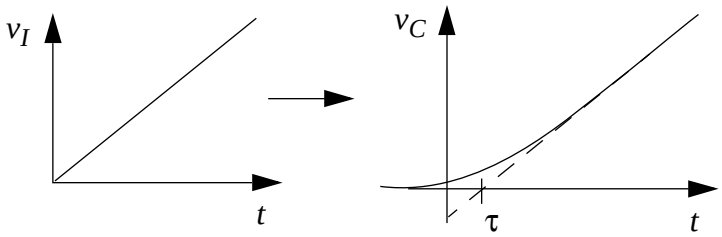


Figure 10.51:

Exercise 10.23 For the circuit in Figure 10.50, with no charge on the capacitor at $t = 0$, given that if $v_I = Atu_{-1}(t)$ then $v_C = \left[A(t-\tau) + A\tau e^{-t/\tau}\right] u_{-1}(t)$. Note that $u_{-1}(t)$ represents a unit step at $t = 0$.

Find:

a) $v_C(t)$ when the input is the same as above but $v_C(t = 0) = V_0$.

b) $v_C(t)$ when $v_C(0) = 0$ and $v_I(t) = Bu_{-1}(t)$. Note that $u_{-1}(t)$ represents a unit step at $t = 0$.

c) $v_C(t)$ for $t \geq T$ when $v_C(0) = 0$ and

$$v_I(t) = \begin{cases} 0 & t \leq 0 \\ At & 0 \leq t \leq T \\ AT & T \leq t \end{cases}$$

Solution:

a)

$$\frac{v_c}{RC} + \frac{dv_c}{dt} = \frac{v_i}{RC} \quad \Rightarrow \quad \text{Homogeneous solution: } v_c = A\ e^{-t/RC}$$

For (a), assume a trial particular solution in the form $v_c = C_1 t + C_2$, since the input is $v_i = At \cdot u_1(t)$. Note that $\underline{A}$ in the homogeneous solution above is different from A in the expression for v_i.

Plug into equation to find:

$$C_1 = A \quad C_2 = -RCA \quad \Rightarrow \quad \text{particular solution is } v_c = A \cdot t - RCA$$

Now apply the initial condition to complete the solution

$$v_c = A\ e^{-t/RC} + At - RCA$$

to find $\underline{A}$.

$$v_c(t = 0) = V_0$$

$$\text{therefore } \underline{A} = V_0 + RCA$$

$$v_c = (V_0 + RCA)e^{-t/RC} + At - RCA$$

$$\text{or, } v_c = [A\ (t - RC) + (V_0 + A \cdot RC)e^{-t/RC}] \cdot u_{-1}(t) \quad \text{(a)}$$

b) Here the particular solution is $v_c = B$, so applying the initial condition, we find:

$$v_c = B(1 - e^{-t/RC}) \quad \text{(b)}$$

c) $v_c(t = 0) = 0$

$v_c(t = T) = A(T - RC) + ARCe^{-T/RC}$, "initial value" for $t \geq T$

$v_c(t \to \infty) = AT$, "final value," for $t \geq T$

Therefore, for $t \geq T$,

$$v_c(t) = AT + [(AT - ARC + ARCe^{-T/RC}) - AT]\ e^{-(t-T)/RC}$$

$$v_c(t) = AT + [ARC(e^{-T/RC} - 1)]\ e^{-(t-T)/RC} \quad \text{(c)}$$

ANS:: (a) $v_c = [A(t - RC) + (V_0 + ARC)e^{-t/RC}]u_{-1}(t)$ (b) $v_c = B(1 - e^{-t/RC})$ (c) $v_c(t) = AT + [ARC(e^{-T/RC} - 1)]e^{-(t-T)/RC}$

Exercise 10.24 A digital memory element is implemented as illustrated in Figure 10.52. Sketch the waveform at the output of the memory element for the input signals shown in Figure 10.53. Assume that the switch is ideal and that the memory element has a 0 stored in it initially.

Solution:

See Figure 10.54

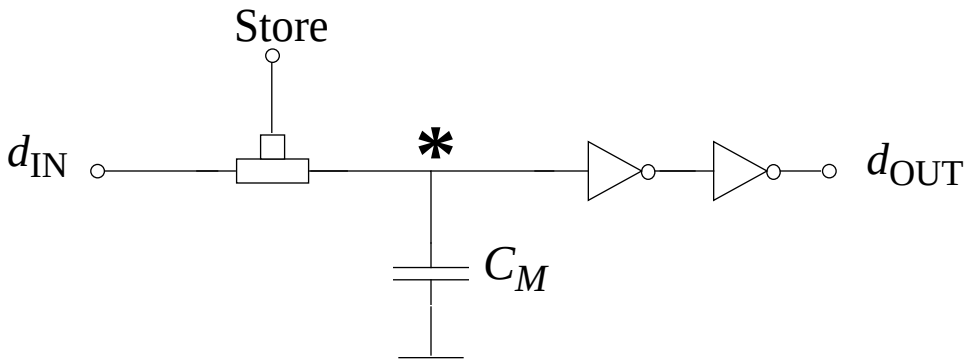


Figure 10.52:

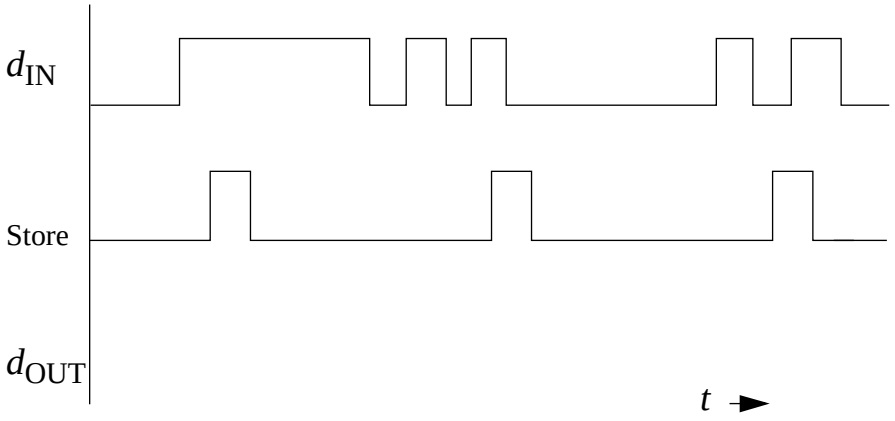


Figure 10.53:

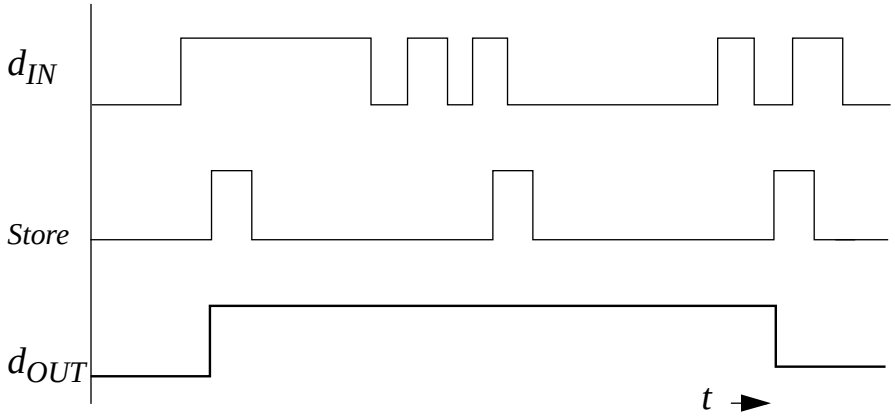


Figure 10.54:

Problems

Problem 10.1 Figure 10.55a illustrates an inverter $INV1$ driving another inverter $INV2$. The corresponding equivalent circuit for the inverter pair is illustrated in Figure 10.55b. A, B, and C represent logical values, and v_A, v_B, and v_C represent voltage levels. The equivalent circuit model for an inverter based on the SRC model of the MOSFET is depicted in Figure 10.56.

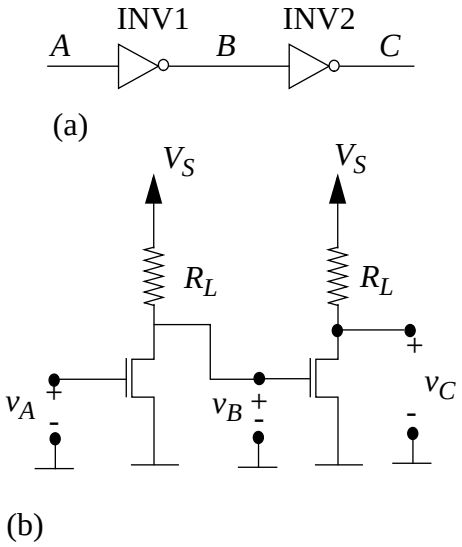


Figure 10.55:

a) Write expressions for the rise and fall times of $INV1$ for the circuit configuration shown in Figure 10.55. Assume that the inverters satisfy the static discipline with voltage thresholds $V_{IL} = V_{OL=V_L}$ and $V_{IH} = V_{OH} = V_H$.

   Hint: The rise time of $INV1$ is the time v_B requires to transition from the lowest voltage reached by v_B (given by the voltage divider action of R_L and R_{ON}) to V_H for a V_S to 0V step transition at the input v_A. Similarly, the fall time of $INV1$ is the time v_B requires to transition from the highest voltage reached by v_B (that is, V_S) to V_L for a 0V to V_S step transition at the input v_A.

b) What is the propagation delay t_{pd} of $INV1$ in the circuit configuration shown in Figure 10.55, for $R_{ON} = 1k$, $R_L = 10R_{ON}$, $C_{GS} = 1nF$, $V_S = 5V$, $V_L = 1V$, and $V_H = 3V$?

Solution:

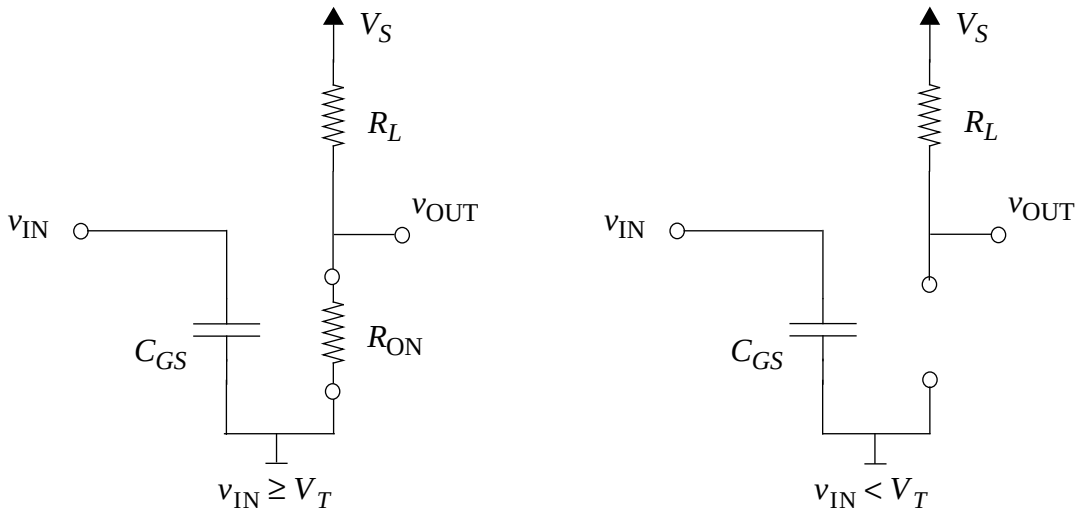


Figure 10.56:

a) For v_B going from low to high:

$v_B = V_S + (V_S \frac{R_{ON}}{R_{ON}+R_L} - V_S)e^{-t/\tau}$

$t_{rise} = -\tau \ln \left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}} \right) \quad \tau = R_L C_{GS}$

For v_B going from high to low:

$v_B = V_S \frac{R_{ON}}{R_{ON}+R_L} + (V_S - V_S \frac{R_{ON}}{R_{ON}+R_L})\, e^{-t/\tau}$

$t_{fall} = -\tau \ln \left(\frac{V_L - V_S \frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}} \right) \quad \tau = C_{GS} \frac{R_{ON} R_L}{R_{ON}+R_L}$

$t_{rise} = -\tau \ln \left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}} \right) \quad \tau = R_L C_{GS}$ $t_{fall} = -\tau \ln \left(\frac{V_L - V_S \frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}} \right)$

$\tau = C_{GS} \frac{R_{ON} R_L}{R_{ON}+R_L}$

b) $t_{pd} = t_{rise} = 8.2 \ \mu s$

ANS:: (a) $t_{rise} = -\tau \ln \left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}} \right) \quad \tau = R_L C_{GS}, \ t_{fall} = -\tau \ln \left(\frac{V_L - V_S \frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}} \right) \quad \tau = C_{GS} \frac{R_{ON} R_L}{R_{ON}+R_L}$ (b) $t_{pd} = 8.2 \ \mu s$

Problem 10.2 The inverter-pair comprising $INV1$ and $INV2$ studied in Problem 10.1 (see Figure 10.55) drives another inverter $INV3$ as illustrated in Figure 10.57a. Logically, the series connected pair of inverters $INV1$ and $INV2$ function as a buffer, as depicted

in Figure 10.57b. The equivalent circuit of the buffer circuit driving $INV3$ is illustrated in Figure 10.57c. For this problem, use the equivalent circuit model for an inverter based on the SRC model of the MOSFET as depicted in Figure 10.56. Assume further that each of the inverters satisfies the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. Assume further that the MOSFET threshold voltage is V_T. (Note that to satisfy the static discipline, the following is true: $V_L < V_T < V_H$).

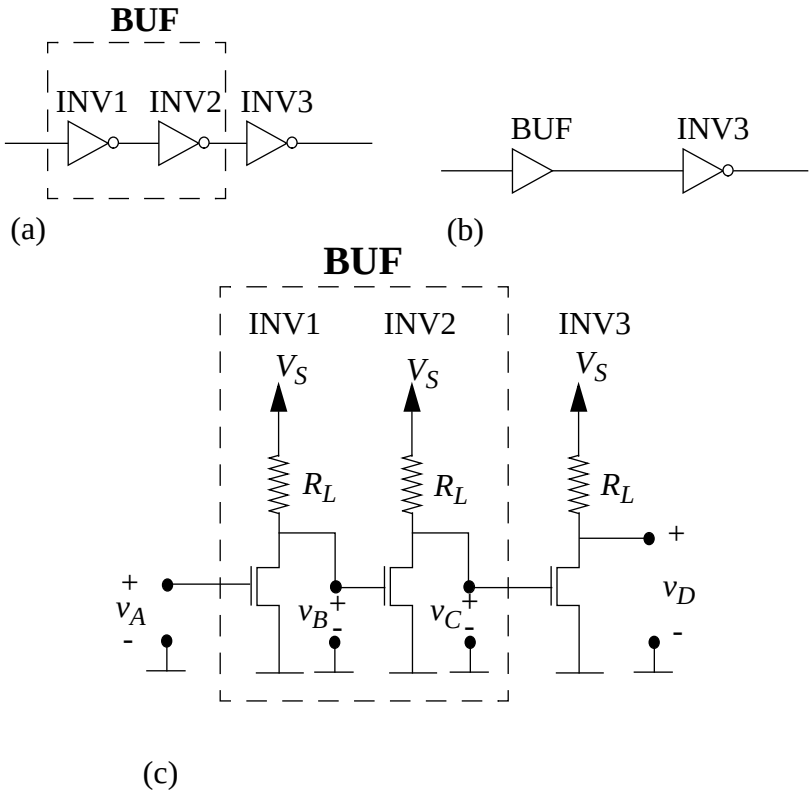


Figure 10.57:

a) Referring to Figure 10.57c, assume that the input to the buffer v_A undergoes a step transition from 0V to V_S at time $t = 0$. Write an expression for $v_B(t)$ for $t \geq 0$ for the step transition in v_A. (Hint: See the fall time calculation in Problem 10.1a). Sketch the form of v_B for $t \geq 0$.

b) Referring to Figure 10.57c, assume that the input to the buffer v_A undergoes a step transition from 0V to V_S at time $t = 0$. Write an expression for $v_C(t)$ for $t \geq 0$ for the step transition in v_A. (Hint: Refer to the sketch of v_B drawn in part (a). The MOSFET in $INV2$ stays on for $v_B \geq V_T$, and turns off when $v_B < V_T$). Sketch the form of $v_C(t)$ for $t \geq 0$.

c) Write an expression for the rise time of the buffer for the circuit configuration shown in Figure 10.57c. (Hint: Refer to the sketch of v_C from part (b). The rise time of the buffer is the time v_C requires to transition from the lowest voltage reached by v_C to V_H from the time the input v_A makes a step transition from 0V to V_S. Note that the rise time of the buffer includes the internal buffer fall delay, which is the time v_B takes to transition from V_S to V_T, and the additional time v_C takes to transition from its lowest voltage to V_H).

d) Referring to Figure 10.57c, assume that the input to the buffer v_A undergoes a step transition from V_S to 0V at time $t = 0$. Write an expression for $v_B(t)$ for $t \geq 0$ for the step transition in v_A. Sketch the form of v_B for $t \geq 0$.

e) Referring to Figure 10.57c, assume that the input to the buffer v_A undergoes a step transition from V_S to 0V at time $t = 0$. Write an expression for $v_C(t)$ for $t \geq 0$ for the step transition in v_A. (Hint: Refer to the sketch of v_B drawn in part (d). The MOSFET in $INV2$ stays off for $v_B < V_T$, and turns on when $v_B \geq V_T$). Sketch the form of $v_C(t)$ for $t \geq 0$.

f) Write an expression for the fall time of the buffer for the circuit configuration shown in Figure 10.57c. (Hint: Refer to the sketch of v_C from part (e). The fall time of the buffer is the time v_C requires to transition from V_S to V_L from the time the input v_A makes a step transition from V_S to 0V. Note that the fall time of the buffer is the sum of two components: (1) the internal buffer rise delay, or the time v_B takes to transition from its lowest voltage to V_T and (2) the additional time v_C takes to transition from V_S to V_L).

g) Compute the rise time and the fall time for the buffer assuming that $R_{ON} = 1k$, $R_L = 10R_{ON}$, $C_{GS} = 1nF$, $V_S = 5V$, $V_L = 1V$, $V_T = 2V$, and $V_H = 3V$.

h) What is the propagation delay t_{pd} of the buffer when the buffer output is connected to a single inverter using an ideal wire as shown in Figure 10.57c?

i) Notice that unlike the delay calculation in Problem 10.1, we needed the value of V_T to obtain the buffer delay. Why was it necessary in the case of the buffer?

j) An approximate value for the buffer delay can be obtained by doubling the individual inverter delay. Estimate the buffer delay by using the inverter delay computed in Problem 10.1b. What is the percentage error in the value of this estimated delay as compared to the accurate buffer delay computed in part (i) of this problem?

Solution:

a) $v_B = V_S \frac{R_{ON}}{R_{ON}+R_L} + (V_S - V_S \frac{R_{ON}}{R_{ON}+R_L})\, e^{-t/\tau} \quad \tau = C_{GS} \frac{R_{ON} R_L}{R_{ON}+R_L}$
See Figure 10.58.

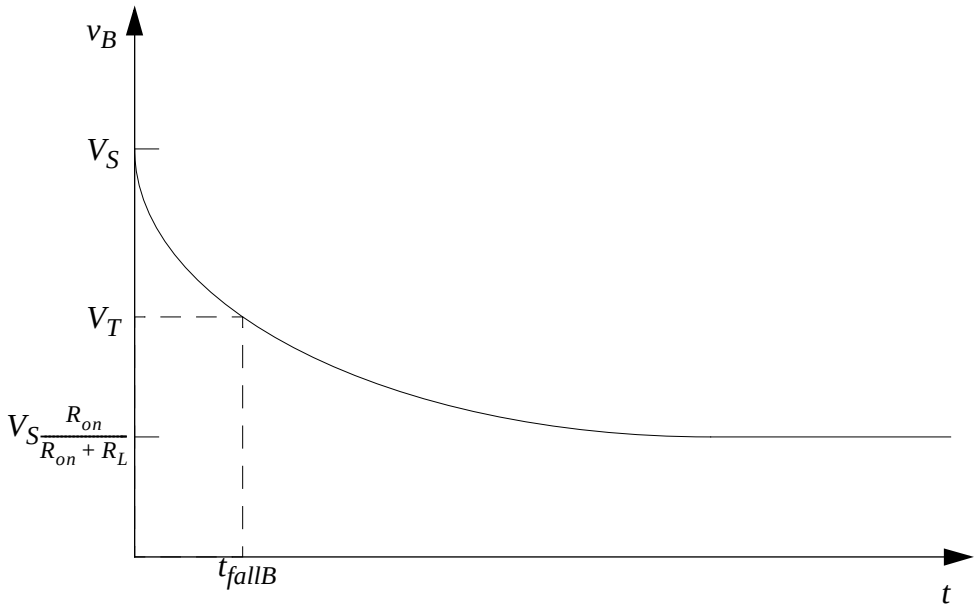


Figure 10.58:

b) The MOSFET in $INV2$ stays on for $v_B \geq V_T$, and turns off when $v_B < V_T$. We will call t_{fallB} the time it takes for v_B to reach V_T.

$$t_{fallB} = -\tau_{fall} \ln\left(\frac{V_T - V_S\,\frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S\,\frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau_{fall} = C_{GS}\frac{R_{ON}R_L}{R_{ON}+R_L}$$

$t < t_{fallB}$: $v_C = V_S\frac{R_{ON}}{R_{ON}+R_L}$

$t > t_{fallB}$: $v_C = V_S + (V_S\frac{R_{ON}}{R_{ON}+R_L} - V_S)\; e^{-(t-t_{fallB})/\tau_{rise}} \quad \tau_{rise} = R_L C_{GS}$

See Figure 10.59.

c) $v_H = V_S + (V_S\frac{R_{ON}}{R_{ON}+R_L} - V_S)e^{-(t-t_{fallB})/\tau_{rise}}$

$$t_{riseC} = t_{fallB} - \tau_{rise} \ln\left(\frac{V_S - V_H}{V_S - V_S\,\frac{R_{ON}}{R_{ON}+R_L}}\right)$$

d) $v_B = V_S + (V_S\frac{R_{ON}}{R_{ON}+R_L} - V_S)e^{-t/\tau_{rise}}$

See Figure 10.60.

e) We will call t_{riseB} the time it takes for v_B to reach V_T.

$$t_{riseB} = -\tau_{rise} \ln\left(\frac{V_S - V_T}{V_S - V_S\,\frac{R_{ON}}{R_{ON}+R_L}}\right)$$

$$v_C = V_S\frac{R_{ON}}{R_{ON}+R_L} + (V_S - V_S\frac{R_{ON}}{R_{ON}+R_L})\; e^{-(t-t_{riseB})/\tau_{fall}}$$

See Figure 10.61.

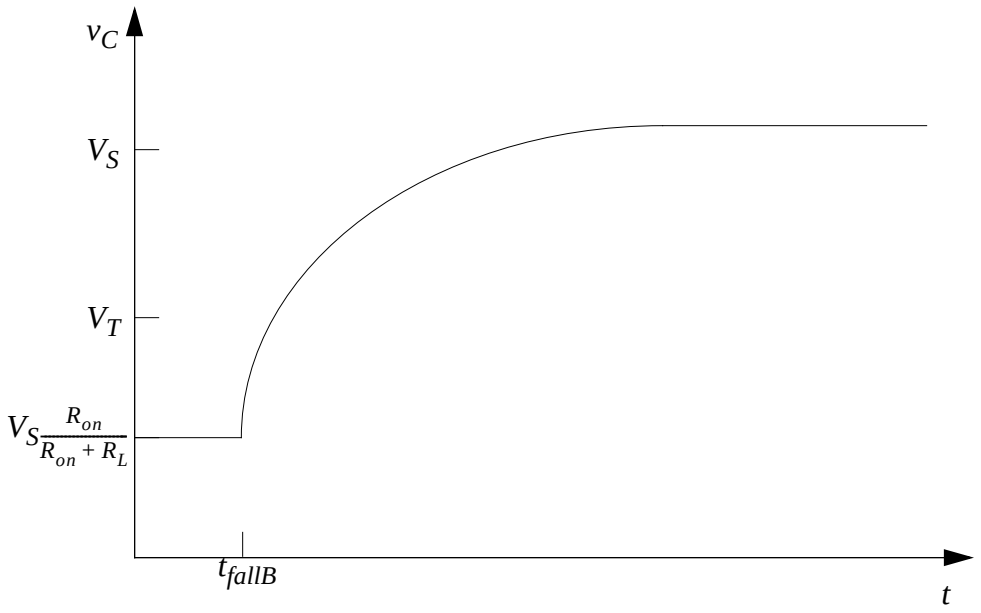


Figure 10.59:

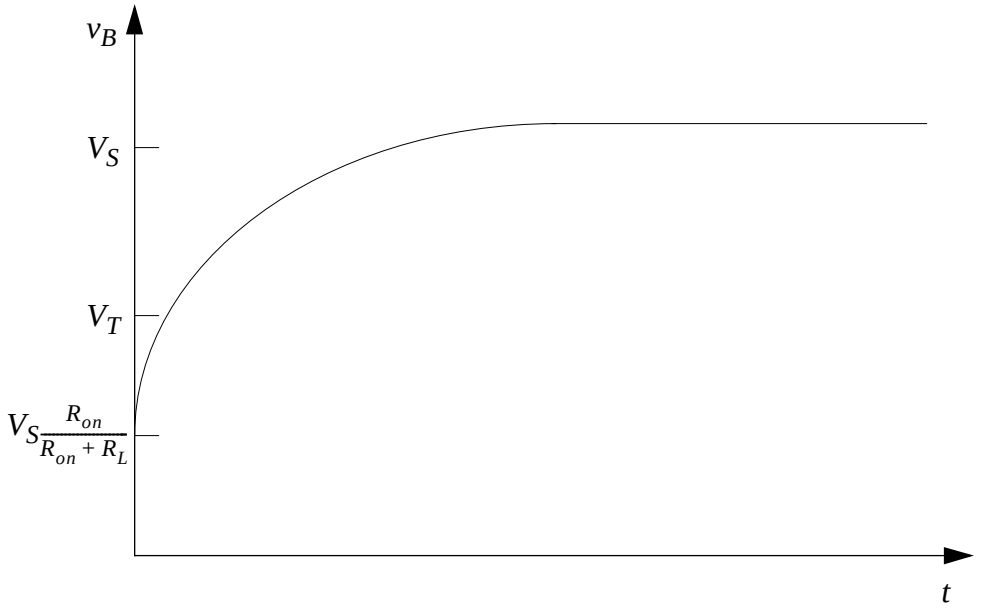


Figure 10.60:

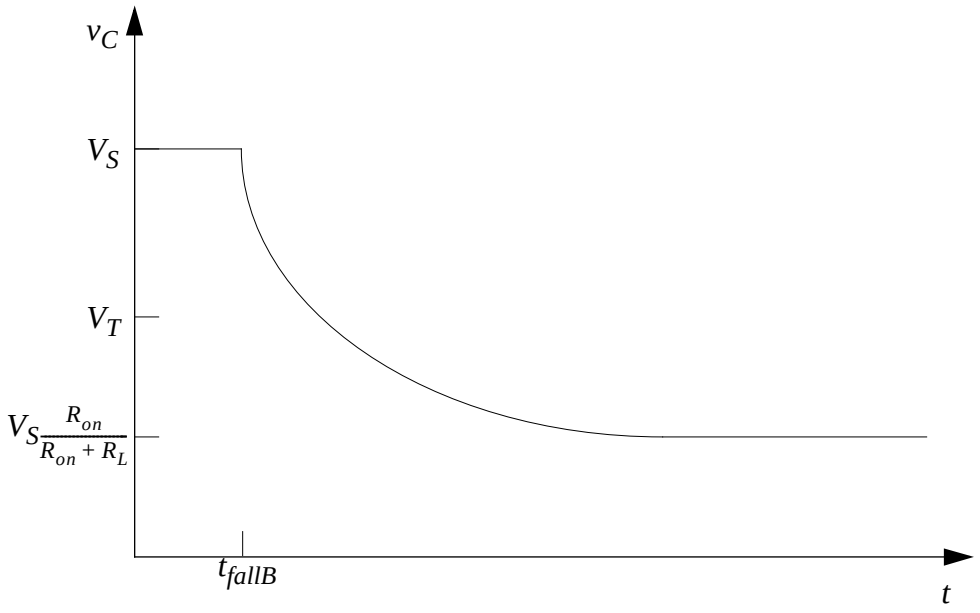


Figure 10.61:

f) $t_{fallC} = t_{riseB} - \tau_{fall} \ln\left(\frac{V_L - V_S\ \frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S\ \frac{R_{ON}}{R_{ON}+R_L}}\right)$

g) $t_{riseC} = 9.19\ \mu s$
$t_{fallC} = 6.08\ \mu s$

h) $t_{pd} = t_{riseC} = 9.19\ \mu s$

i) $INV2$ switches when v_B rises above or falls below V_T. Therefore the output of the buffer is dependant on V_T.

j) $Approximate\ delay = 16.2\ \mu s$
$\%error = \frac{16.2-9.19}{9.19} = 76\%$

ANS:: (a) $v_B = V_S\frac{R_{ON}}{R_{ON}+R_L} + (V_S - V_S\frac{R_{ON}}{R_{ON}+R_L})e^{-t/\tau}$ $\tau = C_{GS}\frac{R_{ON}R_L}{R_{ON}+R_L}$ (b) $t < t_{fallB}$: $v_C = V_S\frac{R_{ON}}{R_{ON}+R_L}$, $t > t_{fallB}$: $v_C = V_S + (V_S\frac{R_{ON}}{R_{ON}+R_L} - V_S)e^{-(t-t_{fallB})/\tau_{rise}}$ $\tau_{rise} = R_L C_{GS}$, $t_{fallB} = -\tau_{fall}\ln\left(\frac{V_T - V_S\frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right)$ $\tau_{fall} = C_{GS}\frac{R_{ON}R_L}{R_{ON}+R_L}$ (c) $t_{riseC} = t_{fallB} - \tau_{rise}\ln\left(\frac{V_S - V_H}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right)$ (d) $v_B = V_S + (V_S\frac{R_{ON}}{R_{ON}+R_L} - V_S)e^{-t/\tau_{rise}}$ (e) $v_C = V_S\frac{R_{ON}}{R_{ON}+R_L} + (V_S - V_S\frac{R_{ON}}{R_{ON}+R_L})e^{-(t-t_{riseB})/\tau_{fall}}$, $t_{riseB} = -\tau_{rise}\ln\left(\frac{V_S - V_T}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right)$ (f)

$t_{fallC} = t_{riseB} - \tau_{fall} \ln\left(\frac{V_L - V_S\frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right)$ (g) $t_{riseC} = 9.19\ \ \mu s$, $t_{fallC} = 6.08\ \ \mu s$ (h) $t_{pd} = 9.19\ \ \mu s$ (j) $delay = 16.2\ \ \mu s$, $\%error = 76\%$

Problem 10.3 The circuit depicted in Figure 10.62 implements the logic function $Z = \overline{(ABC + D)E}$. Suppose the output of this circuit drives an inverter with a gate capacitance of C_{GS}. Assume that the MOSFETs in the circuit have on resistance R_{ON}, and that the high and low voltage thresholds are $V_{IH} = V_{OH} = V_H$ and $V_{IL} = V_{OL} = V_L$ respectively.

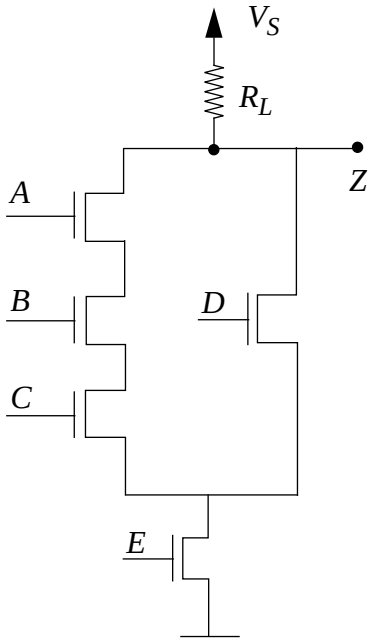


Figure 10.62:

a) What combination of logical inputs will result in the worst-case fall time for the circuit?

b) Derive an expression for the worst case fall time in terms of V_S, R_L, R_{ON}, V_L and V_H. Not all variables need appear in your answer.

c) Derive an expression for the worst case rise time.

Solution:

a) To make the rise time longest τ must be its largest possible value. To achieve this, A, B, C, and E must all be high and D must be low.

b) $Z = V_S \frac{4R_{ON}}{4R_{ON}+R_L} + (V_S - V_S \frac{4R_{ON}}{4R_{ON}+R_L})\, e^{-t/\tau_{fall}}$

$$t_{fall} = -\tau_{fall} \ln \left(\frac{V_L - V_S \frac{4R_{ON}}{4R_{ON}+R_L}}{V_S - V_S \frac{4R_{ON}}{4R_{ON}+R_L}} \right) \quad \tau_{fall} = C_{GS} \frac{4R_{ON}R_L}{4R_{ON}+R_L}$$

c) τ_{rise} is always $C_{GS}R_L$ and the maximum voltage is always V_S, so the rise time is based only on the minimum voltage level when low. The lowest low results when A, B, and C are high, while D and E are low.

$$t_{rise} = -\tau_{rise} \ln \left(\frac{V_S - V_H}{V_S - V_S \frac{2R_{ON}}{2R_{ON}+R_L}} \right)$$

ANS:: (a) A, B, C, and E must all be high and D must be low (b) $t_{fall} = -\tau_{fall} \ln \left(\frac{V_L - V_S \frac{4R_{ON}}{4R_{ON}+R_L}}{V_S - V_S \frac{4R_{ON}}{4R_{ON}+R_L}} \right) \quad \tau_{fall} = C_{GS} \frac{4R_{ON}R_L}{4R_{ON}+R_L}$ (c) $t_{rise} = -\tau_{rise} \ln \left(\frac{V_S - V_H}{V_S - V_S \frac{2R_{ON}}{2R_{ON}+R_L}} \right)$

Problem 10.4 Figure 10.63 illustrates an inverter $INVA$ connected to another inverter $INVB$ by a wire of length l on a VLSI chip.

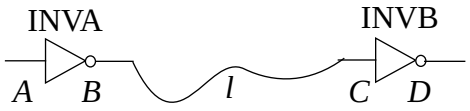


Figure 10.63:

Figure 10.64 shows a lumped circuit model for the (nonideal) wire of length l in a VLSI chip, and Figure 10.65 shows the equivalent circuit model for the inverter pair connected by the nonideal wire based on the SRC model for the MOSFET. Assume that the logic devices satisfy a static discipline with voltage thresholds given by $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$, and that the supply voltage is V_S.

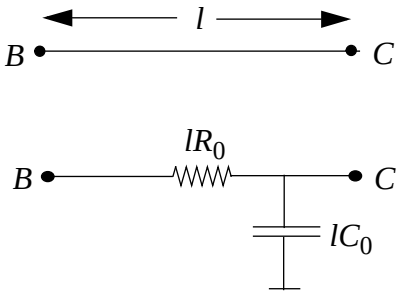


Figure 10.64:

Suppose $INVA$ is driven by a 0 to 1 transition at its input (denoted v_{INA}) at time $t = 0$. Determine $t_{pd,0\to1}$, the propagation delay through $INVA$ for a 0 to 1 transition at

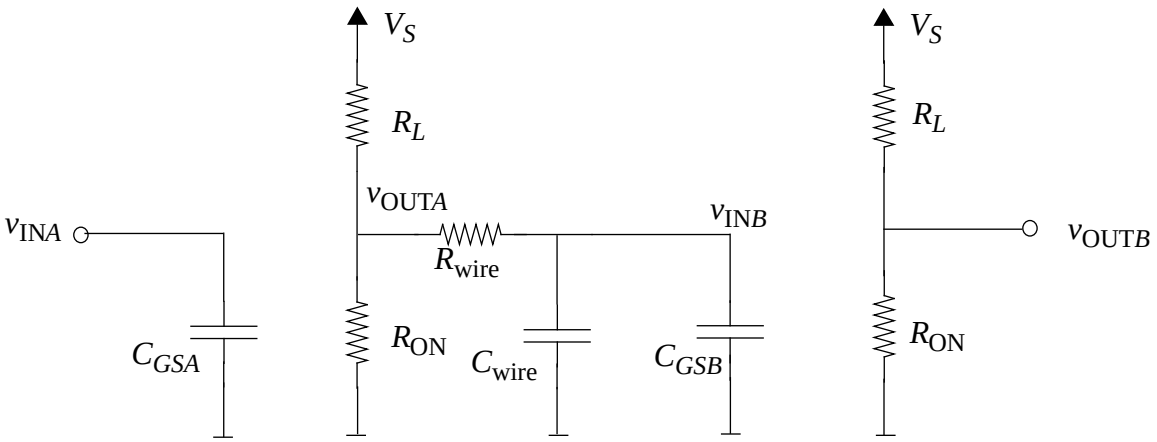


Figure 10.65:

its input. Recall that by our definition $t_{pd,0\to1}$ is the time taken by the input to $INVB$, namely v_{INB}, to fall from V_S to V_L following the 0 to 1 transition at the input of $INVA$. Express your answer in terms of V_S, V_L, R_{ON}, C_{GS}, the wire length l, and the wire model parameters. By what factor does the delay increase for a $2\times$ increase in the wire length l?

Solution:

$v_{INB} = V_S \frac{R_{ON}}{R_{ON}+R_L} + (V_S - V_S \frac{R_{ON}}{R_{ON}+R_L})e^{-t/\tau}$

$t_{pd,0\to1} = -\tau \ln\left(\frac{V_L - V_S \frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (lC_o + C_{GS})(lR_o + \frac{R_{ON}R_L}{R_{ON}+R_L})$

Assuming the wiring terms dominate, a 2x increase in the wire length yields a 4x increase in the delay.

ANS:: $t_{pd,0\to1} = -\tau \ln\left(\frac{V_L - V_S \frac{R_{ON}}{R_{ON}+R_L}}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (lC_o + C_{GS})(lR_o + \frac{R_{ON}R_L}{R_{ON}+R_L})$

Problem 10.5 Figure 10.66 illustrates an inverter $INVA$ driving n other inverters $INV1$ through $INVn$. As in Problem 10.1, each of the inverters is constructed using a MOSFET and a resistor R_L, and the inverters satisfy the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. Model the MOSFETs using the SRC model with MOSFET on resistance R_{ON} and gate capacitance C_{GS} as in Problem 10.1 (see Figure 10.56).

a) What are the rise and fall times for $INVA$? (Hint: Sum the input capacitances of each of the inverters into a single lumped value, and use your answer from Problem 10.1 to solve this part). How does the rise time increase as the number of driven inverters n increases?

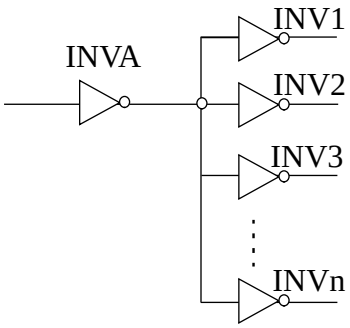


Figure 10.66:

b) What is the propagation delay t_{pd} of $INVA$ in the circuit configuration shown in Figure 10.66, for $R_{ON} = 1k$, $R_L = 10R_{ON}$, $C_{GS} = 1nF$, $V_S = 5V$, $V_L = 1V$, and $V_H = 3V$.

c) Now, assume that each of the wires connecting the output of $INVA$ to each of the inverters $INV1$ through $INVn$ is nonideal as depicted in Figure 10.67. Model each of the wires using the model shown in Figure 10.68. Assuming that the input of $INVA$ makes a step transition from 1 to 0, find the rise time at the input of any one of the inverters $INVi$ driven by $INVA$.

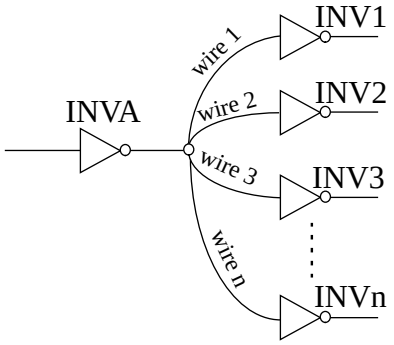


Figure 10.67:

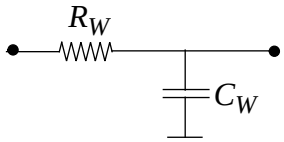


Figure 10.68:

d) Compute the value of the rise time determined in part (c) for the following parameters: $R_{ON} = 1k$, $R_L = 10R_{ON}$, $C_{GS} = 1nF$, $R_W = 100\Omega$, $C_W = 10nF$,

$V_S = 5V$, $V_L = 1V$, and $V_H = 3V$.

Solution:

a) $t_{rise} = -\tau \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = nC_{GS}R_L$

The rise time increases linearly with n.

b) $t_{rise} = n8.2 \ \mu s$

c) Refer to Figure 10.69.

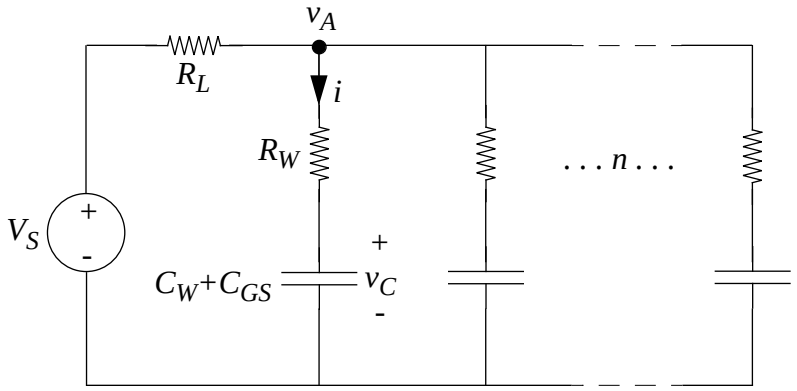


Figure 10.69:

$\frac{V_S - V_A}{R_L} = ni_C = nC_{eq}\frac{dv_C}{dt} \quad C_{eq} = C_W + C_{GS}$

$V_A = i_C R_W + v_C = R_W C_{eq}\frac{dv_C}{dt} + v_C$

Combining we have $V_S = C_{eq}(nR_L + R_W) + v_C \quad v_C(0) = V_S \frac{R_{ON}}{R_{ON}+R_L}$

Solving this differential equation yeilds:

$v_C = V_S + (V_S \frac{R_{ON}}{R_{ON}+R_L} - V_S)e^{-t/\tau} \quad \tau = (C_W + C_{GS})(nR_L + R_W)$

$t_{rise} = -\tau \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right)$

d) $t_{rise} = (0.9 + n90.3) \ \mu s$

ANS:: (a) $t_{rise} = -\tau \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = nC_{GS}R_L$ (b) $t_{rise} = n8.2 \ \mu s$ (c) $t_{rise} = -\tau \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (C_W + CGS)(nR_L + R_W)$ (d) $t_{rise} = (0.9 + n90.3) \ \mu s$

Problem 10.6 As can be seen from the answer to Problem 10.4, long wires have a serious negative impact on the delay. One way to alleviate the wire delay problem is to introduce buffers when driving long wires, as illustrated in Figure 10.70. Assume that the buffer is constructed as depicted in Figure 10.57c using a pair of inverters identical to the inverters in this problem. In other words, the input of a buffer has a capacitance C_{GS} to ground, and the output of a buffer has the same drive characteristics as an inverter output. For this problem, you will ignore the internal delay of the buffer. (See Problem 10.2c and f for a definition of the internal buffer delay). In other words, assume that a buffer driving zero output capacitance has zero delay.

By introducing a buffer, the effective length of wire driven by either the inverter $INVA$ or the buffer is $l/2$. For large l, given the nonlinear relationship between wire length and delay, the sum of the delays in driving the two $l/2$ wire segments is smaller than driving a single wire segment of length l.

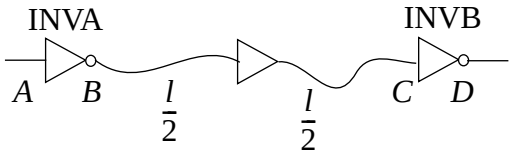


Figure 10.70:

a) Compute the propagation delay between the input of $INVA$ and the input of $INVB$ for the circuit in Figure 10.70. Assume that rising transitions are longer than falling transitions at the output of either the inverters or the buffers.

   Hint: The total delay from the input of $INVA$ to the output of $INVB$ is the sum of the following two quantities: (1) the propagation delay of $INVA$ driving the wire segment of length $l/2$ and a capacitance C_{GS} corresponding to the gate capacitance of the buffer and (2) the propagation delay of the buffer driving the second wire segment of length $l/2$ and a capacitance C_{GS} corresponding to the gate capacitance of $INVB$. (Remember, the buffer has zero delay when it is driving zero output capacitance).

b) Figure 10.71 shows a circuit in which $n-1$ buffers are introduced between $INVA$ and $INVB$. $INVA$ and each of the buffers drives a segment of wire of length l/n. Compute the propagation delay between the input of $INVA$ and the input of $INVB$ for this case.

c) Determine the number of buffers for which the propagation delay for the circuit in Figure 10.71 is minimized.

Solution:

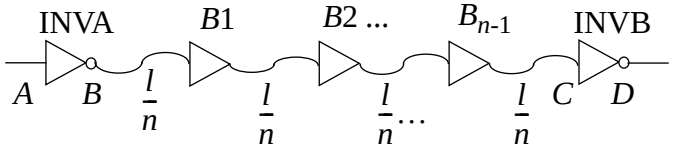


Figure 10.71:

a) The delay is equivalent for each length of wire, so the total delay is twice that of a single wire of length $l/2$. Using the result from Problem 4 we can easily see the following.

$$t_{pd} = -2\tau \ln\left(\frac{V_S - V_H}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (\tfrac{l}{2}C_o + C_{GS})(\tfrac{l}{2}R_o + R_L)$$

b) $t_{pd} = -n\tau \ln\left(\frac{V_S - V_H}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (\frac{l}{n}C_o + C_{GS})(\frac{l}{n}R_o + R_L)$

c) The n that minimizes t_{pd} we must also minimize $n\tau = n(\frac{l}{n}C_o + C_{GS})(\frac{l}{n}R_o + R_L)$.
$\frac{d}{dn}n(\frac{l}{n}C_o + C_{GS})(\frac{l}{n}R_o + R_L) = 0$
Solving for $n \;\Rightarrow\; n = \sqrt{\frac{lR_oC_o}{C_{GS}R_L}}$

ANS:: (a) $t_{pd} = -2\tau \ln\left(\frac{V_S - V_H}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (\frac{l}{2}C_o + C_{GS})(\frac{l}{2}R_o + R_L)$ (b) $t_{pd} = -n\tau \ln\left(\frac{V_S - V_H}{V_S - V_S\frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = (\frac{l}{n}C_o + C_{GS})(\frac{l}{n}R_o + R_L)$ (c) $n = \sqrt{\frac{lR_oC_o}{C_{GS}R_L}}$

Problem 10.7 Figure 10.72 shows a buffer $BUF1$ driving a large load capacitor C_L. The buffer is built using an inverter pair as in Figure 10.57c. The width to length ratio of each NMOS transistor in the buffer is W/L and the resistors have a value R_L. Accordingly, the gate capacitance seen at the input of the buffer is given by $(W/L)C_{GS}$. The buffer satisfies a static discipline with voltage thresholds given by $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. The supply voltage is V_S. Assume that the internal buffer delay (as defined in Problem 10.2c) is zero. Assume that there is a 0 to 1 transition at the input A at time $t = 0$.

a) Compute the propagation delay for the buffer $BUF1$ driving the load C_L for the rising transition at the input A.

b) Now consider Figure 10.73. This figure shows the use of a second buffer with larger transistors and smaller valued load resistors ($x > 1$) interposed between the first buffer and the load capacitor. Compute the propagation delay for the buffer

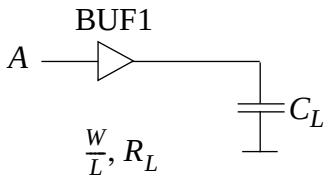


Figure 10.72:

$BUF1$ in series with $BUF2$ driving the load C_L for the rising transition at the input A. Assuming that C_L is much larger than the input gate capacitances of the two buffers, and that $x > 1$, is the delay computed in part (b) greater than or less than the delay computed in part (a)?

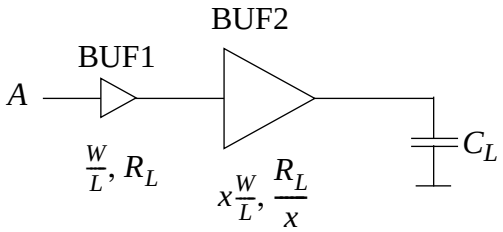


Figure 10.73:

c) Consider Figure 10.74. This figure shows the use of a series of n buffers in which $BUFi$ has transistors that have a width x times that of $BUFi-1$ and resistors that are a factor x smaller than that of $BUFi-1$. n is chosen such that C_L is x times the gate capacitance of $BUFn$. In other words, n satisfies the equation:

$$C_L = x^n \frac{W}{L} C_{GS}$$

Compute the propagation delay for the sequence of n buffers driving the load C_L for the rising transition at the input A. As before, assume that C_L is larger than the input gate capacitances of each of the buffers and that $x > 1$.

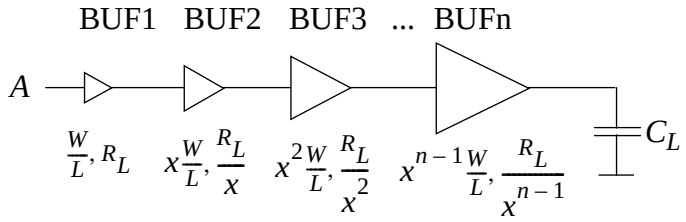


Figure 10.74:

c) Determine the value of x for which the propagation delay computed in part (b) is minimized.

Solution:

a) $t_{pd} = -\tau \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = R_L C_L$

b) $t_{pd} = (x\frac{W}{L}C_{GS}R_L + C_L\frac{R_L}{x})\ \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right)$

Since $C_L \ll x\frac{W}{L}C_{GS}$ the first term in negligible. Since $x > 1$ the delay computed in part (b) is smaller than the delay computed in part (a).

c) The result will be a sum of terms similar to those found in part (b).

$$t_{pd} = -\sum_{k=1}^{n} x^k \frac{W}{L} C_{GS} \frac{R_L}{x^k}\ \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{x^k R_{ON}}{x^k R_{ON}+R_L}}\right)$$

d) The limitation on x is the maximum value such that the buffer can still achieve a valid low.

$V_L = \frac{R_{ON}}{R_{ON}+R_L/x} \Rightarrow x = \frac{R_L \frac{V_L}{V_S}}{R_{ON}(1-\frac{V_L}{V_S})}$

ANS:: (a) $t_{pd} = -\tau \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right) \quad \tau = R_L C_L$ (b) $t_{pd} = (x\frac{W}{L}C_{GS}R_L + C_L\frac{R_L}{x}) \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{R_{ON}}{R_{ON}+R_L}}\right)$ (c) $t_{pd} = -\sum_{k=1}^{n} x^k \frac{W}{L} C_{GS} \frac{R_L}{x^k} \ln\left(\frac{V_S - V_H}{V_S - V_S \frac{x^k R_{ON}}{x^k R_{ON}+R_L}}\right)$ (d) $x = \frac{R_L \frac{V_L}{V_S}}{R_{ON}(1-\frac{V_L}{V_S})}$

Problem 10.8 In this problem, you will study the affect of parasitic inductances in VLSI packages. VLSI chips are sealed inside plastic or ceramic packages and connections to certain nodes of their internal circuitry (for example, power supply, ground, input and output nodes) need to be extended outside the package. These extensions are commonly accomplished by first connecting the internal node to a metallic "pad" on the VLSI chip. In turn, the pad is connected to one end of a package "pin" using a wire that is bonded to the pad at one end and the pin at the other. The package pin, which extends outside the package, is commonly connected to external connections using a PC board.

Together the package pin, the bond wire, and the internal chip wire are associated with a non zero parasitic inductance. In this problem, we will study the effect of the parasitic inductance associated with power supply connections. Figure 10.75 shows a model of our situation. Two inverters with load resistors R_1 and R_2 and MOSFETs with width to length ratios W_1/L_1 and W_2/L_2 respectively are connected to the same power supply node on the chip that is labeled with a voltage v_P. Ideally this chip-level power supply node would be extended with an ideal wire outside the chip to the external power supply V_S shown in the figure. However, notice the parasitic inductance L_P interposed between the power supply node on the chip (marked with voltage v_P) and the external power supply node (marked with voltage V_S).

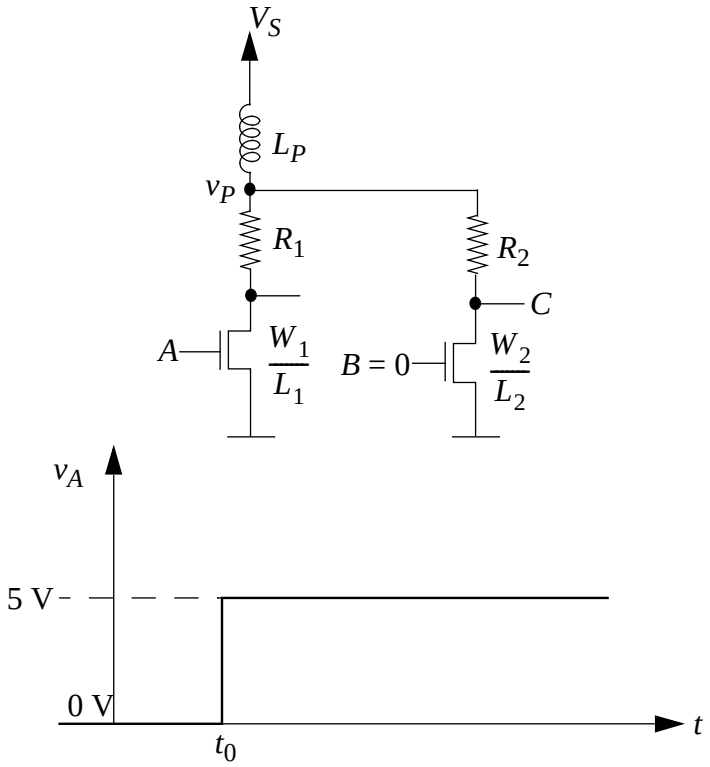


Figure 10.75:

Assume that the input B is 0V at all times. Assume further that the input A has 0V applied to it initially. At time $t = t_0$, a 5V step is applied at the input A. Plot the form of v_P as a function of time. Clearly show the value of v_P just prior to t_0 and just after t_0. Assume that the on resistance of a MOSFET is given by the relation $\frac{W}{L}R_n$ and that MOSFET's threshold voltage is $V_T < V_S$. Also assume that $V_T < 5V$.

Solution:

i_P will be used to refer to the current through the inductor, from V_S to v_P. For $t < t_0$,

$v_P = V_S$. The following applies for $t < t_0$.

$i_P(t = 0^-) = i_P(t = 0^+) = 0.$

$i_P(t \gg t_0) = \frac{V_S}{R_1 + \frac{W_1}{L_1} R_n}$

$\tau = \frac{L_P}{R_1 + \frac{W_1}{L_1} R_n}$

$i_P = \frac{V_S}{R_1 + \frac{W_1}{L_1} R_n}(1 - e^{-(t-t_0)/\tau})$

$v_P = (R_1 + \frac{W_1}{L_1} R_n) i_P = V_S(1 - e^{-(t-t_0)/\tau})$

See Figure 10.76.

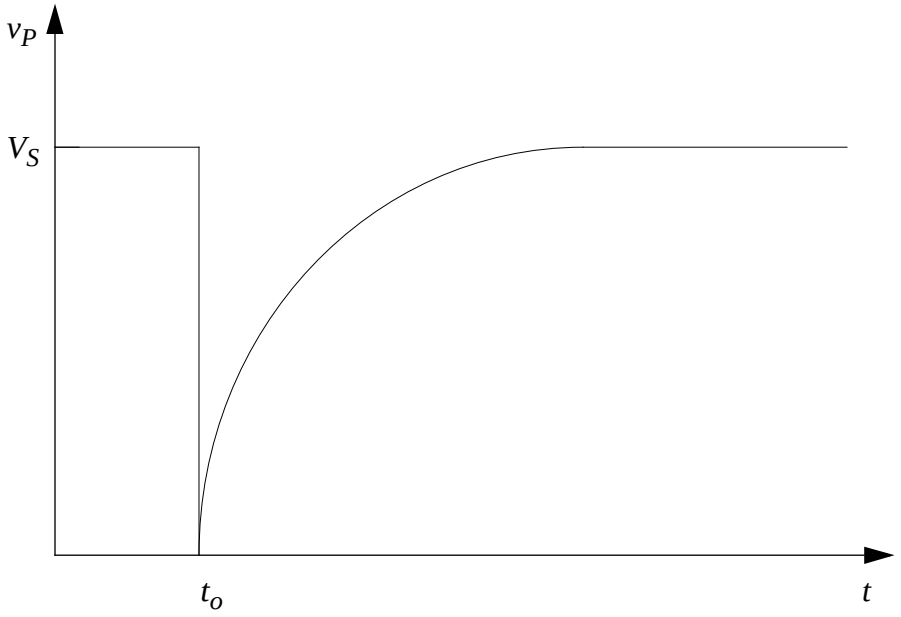


Figure 10.76:

Problem 10.9 A certain box, known to contain only linear elements (and no independent sources), is connected as shown in Figure 10.77.

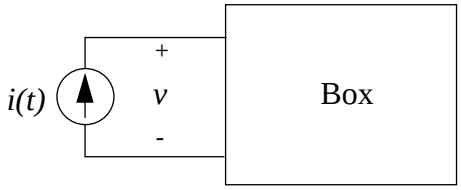


Figure 10.77:

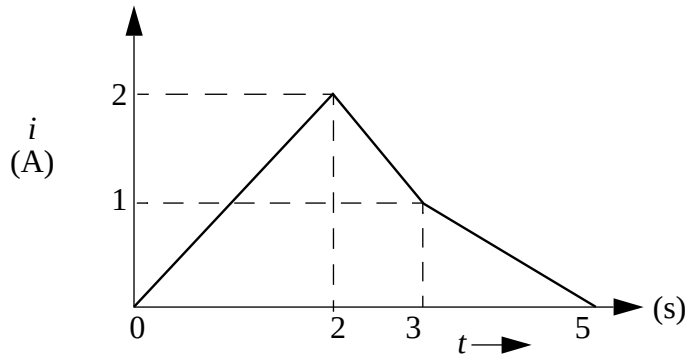


Figure 10.78:

The current waveform $i(t)$ has the form shown in Figure 10.78.

The voltage v is zero for all $t < 0$, and is 1 volt for $0 < t < 2$. What is v during the interval from $t = 2$ to $t = 5$? Show one simple possibility for the circuit in the box.

Solution:

From $0 < t < 2$ we see that $v = \frac{di}{dt} = 1$ V. Keeping this relation we have $v = -1$ V for $2 < t < 3$ and $v = -1/2$ V for $3 < t < 5$.

See Figure 10.79.

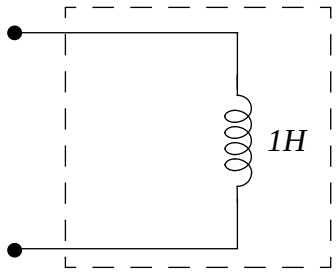


Figure 10.79:

ANS:: $v = -1volt$ for $2 < t < 3$ and $v = -1/2volt$ for $3 < t < 5$

Problem 10.10 As illustrated in Figure 10.80, a capacitor and resistor can be used to filter or smooth the waveforms we derived from a half-wave rectifier, to get something closer to a DC voltage at the output, for use in a power supply for example.

For simplicity, assume the voltage from source v_S is a square wave. Assume that at $t = 0$, $v_O = 0$, i.e., the circuit is at rest. Now assuming that R is small enough to make the circuit time constant much smaller than t_1 or t_2, calculate the voltage waveforms for each half cycle of the input wave. Find the average value of the output voltage v_O for

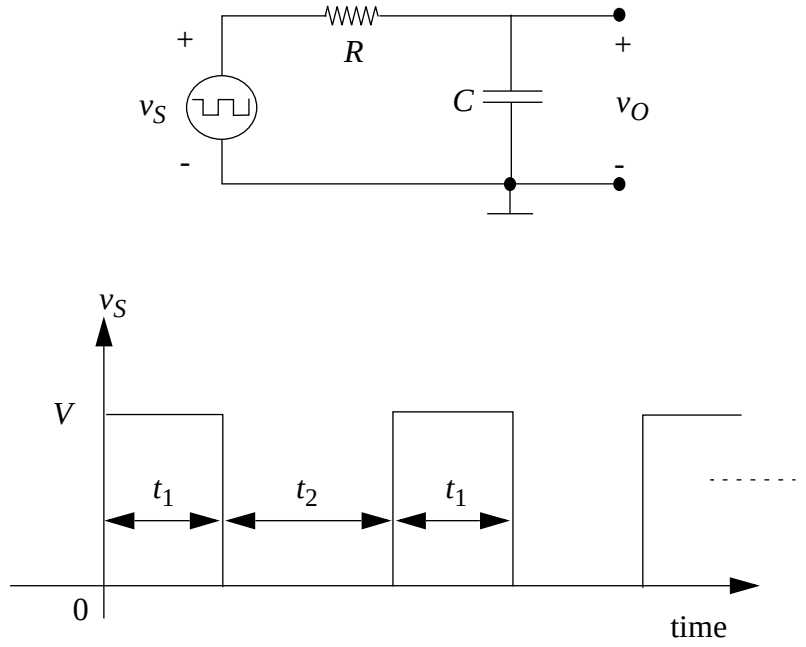


Figure 10.80:

$t_1 = t_2$. Sketch the waveforms carefully. For this choice of R, it should be clear that no useful smoothing has been accomplished.

Solution:

$0 < t < t_1$: $v_O = V(1 - e^{-\frac{t}{RC}})$

$t_1 < t < t_1 + t_2$: $v_O = Ve^{-\frac{(t-t_1)}{RC}}$

The average value of v_O is $V/2$.

See Figure 10.81.

ANS:: $0 < t < t_1$: $v_O = V(1 - e^{-\frac{t}{RC}})$, $t_1 < t < t_1 + t_2$: $v_O = Ve^{-\frac{(t-t_1)}{RC}}$

Problem 10.11 For R much larger than the value used in Problem 10.10, so that the circuit time constant is much larger than t_1 or t_2, (so that the exponentials can be approximated by straight lines) calculate v_O for the *first* half cycle of v_S, and the *second* half cycle. Sketch the result. Note that the solution does not return to the initial point of $v_O = 0$ after one cycle, so is not in the "steady state" yet.

Solution:

$0 < t < t_1$: $v_O = V(1 - e^{-\frac{t}{RC}})$

For $RC \gg t_2$ we can approximate v_O as a straight line through the origin with slope $\frac{V}{RC}$, so

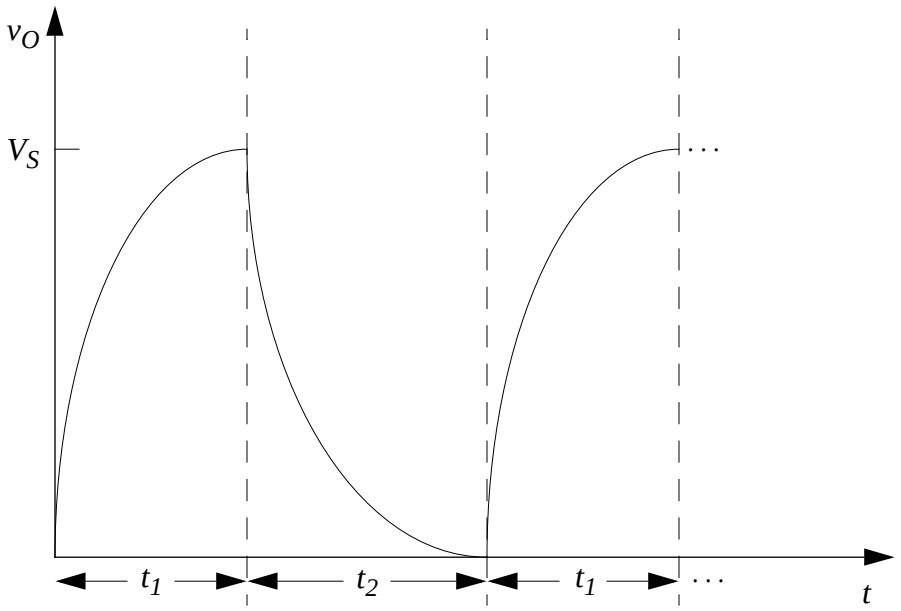


Figure 10.81:

$v_O(t) = \frac{V}{RC}t$

Note that $v_O(t_1) = \frac{Vt_1}{RC}$.

$t_1 < t < t_1 + t_2$: $v_O = \frac{Vt_1}{RC}e^{-\frac{(t-t_1)}{RC}}$

Again, since $RC \gg t_1$ we can approximate v_O as a straight line with slope $-\frac{Vt_1}{RC}\frac{1}{RC} = \frac{Vt_1}{(RC)^2}$, so

$v_O(t) = \frac{Vt_1}{RC} - \frac{Vt_1}{(RC)^2}(t - t_1)$

See Figure 10.82.

ANS:: $0 < t < t_1$: $v_O(t) = \frac{V}{RC}t$, $t_1 < t < t_1 + t_2$: $v_O(t) = \frac{Vt_1}{RC} - \frac{Vt_1}{(RC)^2}(t - t_1)$

Problem 10.12 You can see from Problem 10.10 that for circuit time constant $\tau >> t_1$ and t_2 the capacitor voltage starts from some value V_{min} and increases when v_S is positive; then when v_S is zero, v_O starts at some value V_max and decreases. By definition, the "steady state" of the circuit is when v_O charges from V_{min} to V_{max}, then discharges from V_{max} to the same V_{min}. Assuming $t_1 = t_2$, sketch the v_O waveform in the steady state.

Find the average value of the voltage v_O. Problem 10.11 may give you a hint. Explain your answer. It may help to consider the waveform v_S to be made up of a DC voltage $V/2$ and a symmetrical square wave whose values alternate between $+V/2$ and $-V/2$.

Solution:

See Figure 12-12-a.

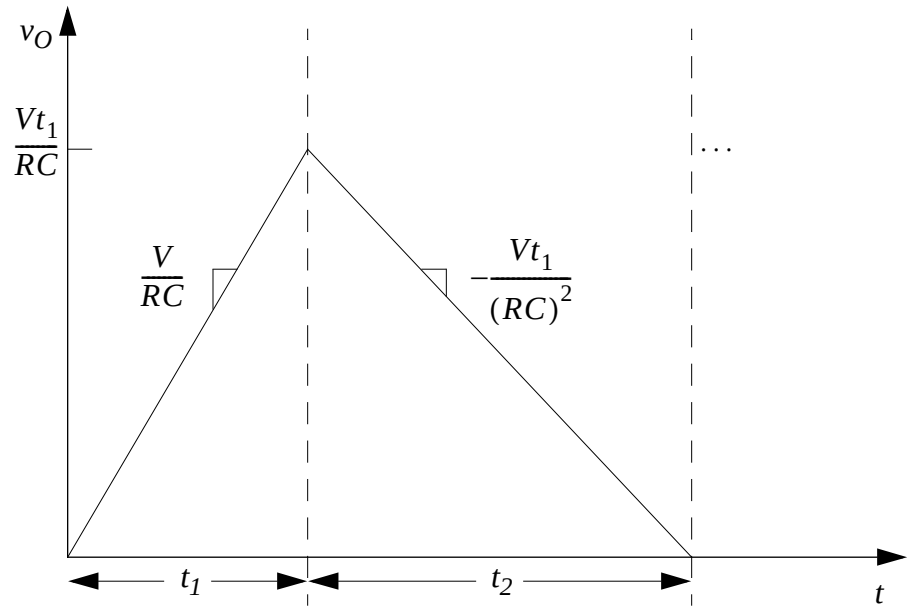


Figure 10.82:

Let's use the hint and think of v_S as the sum of a DC term and a symmetric square wave. For the DC voltage of $V/2$ the capacitor acts like an open and $v_O = V/2$. The symmetric square wave will charge and discharge the capacitor equally as the wave alternates between $V/2$ and $-V/2$, so the average value of v_O from the square wave term is 0. Therefore the average value of v_O for the total v_S is $V/2$.

ANS:: $V/2$

Problem 10.13 This problem (see Figure 10.83) involves a capacitor and two switches. The switches are periodically driven by external clock controls at frequency f_0 such that first S_1 is closed and S_2 is open for the $\frac{1}{2}f_0$, and then S_2 is closed and S_1 open for time $\frac{1}{2}f_0$.

You can assume that the clock drives are *non-overlapping*, that is, S_1 and S_2 are never both closed at the same instant. S_1 opens just before S_2 closes, and S_2 opens just before S_1 closes.

a) Find an effective average current i_A by determining the average rate of charge transfer over several clock cycles. Suppose $v_A = A\cos\omega t$ where $\omega << 2\pi f_0$. Sketch i_A and v_A on the same axes.

b) Examine your results for i_A and v_A from part a). They should be in phase, and the amplitude of i_A should be proportional to the amplitude of v_A. This is a funny form

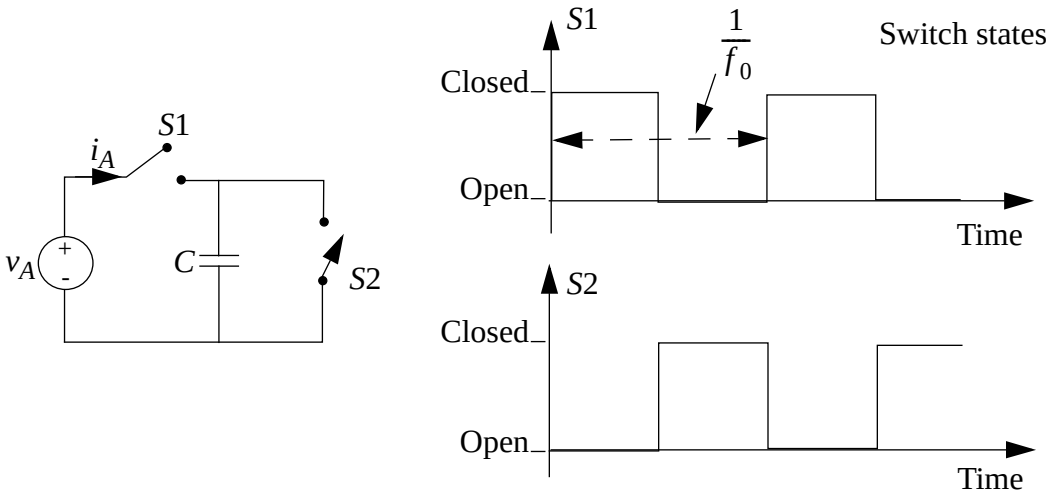


Figure 10.83:

of "resistor". What is the "resistor" value? Where does the energy supplied by v_A actually go?

COMMENT: Circuits of this type are now commonly used in a type of MOS integrated circuit to make elements that simulate resistors with precisely controlled values. The value of such elements is that precise control of capacitor sizes and clock frequencies is easy in MOS integrated circuits, but precise control of resistor values is hard.

Solution:

a) When S_1 is closed and S_2 is open an amount of charge Q is dumped onto the capacitor and when the switches change the charge is removed.

$i_{AVG} = \frac{\Delta Q}{\Delta t} = \frac{CV_A}{1/f_0} \;\Rightarrow\; i_{AVG} = CV_A f_0$

For $v_A = A\cos\omega t$ where $\omega << 2\pi f_0$ we can assume that the average current found above is the actual current i_A. $\Rightarrow\; i_A = ACf_0\cos\omega t$.

See Figure 10.84.

b) $R = \frac{v_A}{i_A} = \frac{1}{Cf_0}$

The energy supplied by v_A goes to charging the capacitor.

ANS:: (a) $i_{AVG} = CV_A f_0$ (b) $R = \frac{v_A}{i_A} = \frac{1}{Cf_0}$

Problem 10.14 State variables can be used to describe the behavior of a wide range of physical systems. For each of the examples below, try to determine:

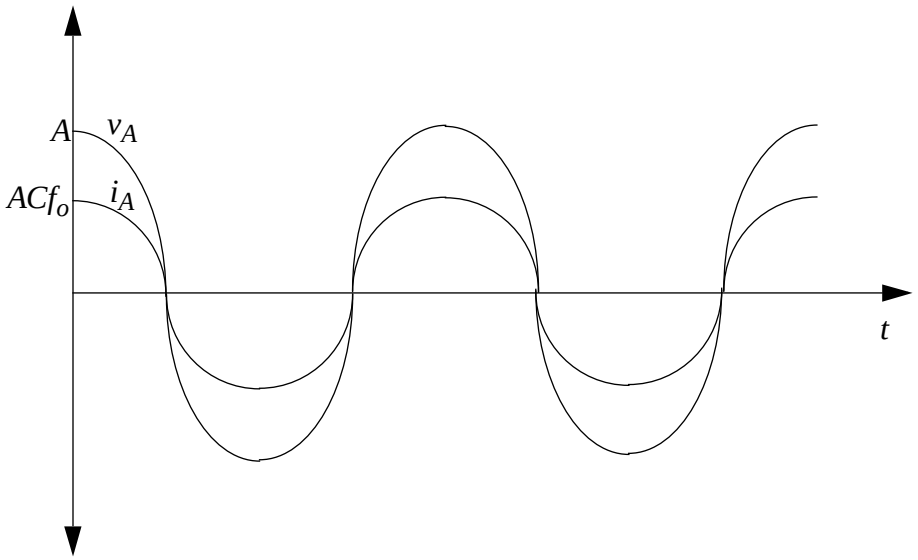


Figure 10.84:

i) the *number* of state variables that are needed to describe the system, i.e., how many state variables.

ii) Which physical variables can serve as state variables.

iii) The form of the state equations, including the identification of inputs.

iv) A simple circuit that can represent the system (an electrical analog).

Here are the examples:

a) A hockey puck leaves a hockey player's stick with velocity v_0 and slides along the ice until it comes to rest (assume a very large hockey rink, or a very weak shot).

b) Halfway through your shower each morning, the water temperature suddenly plunges toward freezing, presumably because your roommates were up earlier and showered first.

c) A simple pendulum starts from rest with an initial angular displacement Δ_0, and rocks back and forth until it eventually comes to rest.

(COMMENT: Part (a) is easy if you concentrate only on the velocity, and is more difficult in terms of the circuit analogy if you include the position as well. Parts (b) and (c) lend themselves to excellent descriptions with circuit analogs.)

Solution:

a) i) 1

ii) velocity of the puck (v)

iii) $\frac{dv}{dt} = kv$ (no inputs, only an initial velocity)

iv) See Figure 10.85.

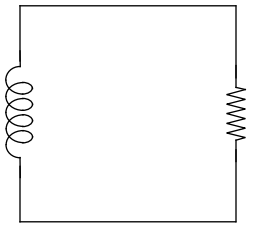


Figure 10.85:

b) i) 1

ii) volume of hot water left in the tank (V)

iii) $\frac{dV}{dt} = -Q$, where Q is a constant input (with units of volume/time) draining the hot water from the tank.

iv) See Figure 10.86.

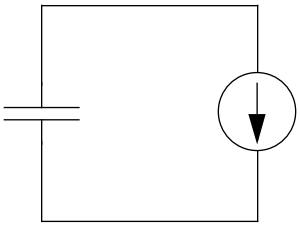


Figure 10.86:

See Figure 10.86.

c) i) 2

ii) angular displacement (θ_1) and its derivative (θ_2)

iii) $\frac{d\theta_1}{dt} = \theta_2$
$\frac{d\theta_2}{dt} = k_1\theta_1 + k_2\theta_2$
There are no inputs, only the initial angular displacement of the pendulum.

iv) See Figure 10.87.

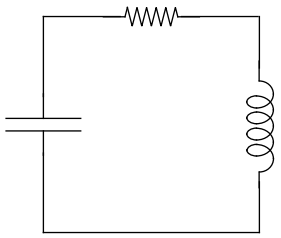


Figure 10.87:

ANS:: (a) (i) 1 (ii) v (iii) $\frac{dv}{dt} = kv$ (b) (i) 1 (ii) V (iii) $\frac{dV}{dt} = -Q$ (c) (i) 2 (ii) $theta$ and its derivative (iii) $\frac{d\theta_1}{dt} = \theta_2$, $\frac{d\theta_2}{dt} = k_1\theta_1 + k_2\theta_2$

Problem 10.15 Figure 10.88 shows the use of a filter choke.

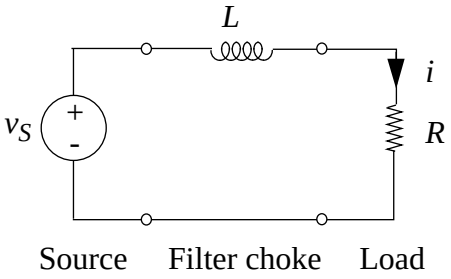


Figure 10.88:

Assume that the waveform for v_S for parts a) and b) is a series of square pulses starting at $t = 0$ as shown in Figure 10.89.

Assume that the waveform for v_S for parts c) and d) is a half-rectified sine wave as shown in Figure 10.90.

a) Assume initial rest conditions at $t = 0^-$, and assume that both t_1 and t_2 are long compared to the time constant of the network. Determine each of the following:

   i) Calculate the current waveform for the first cycle ($0 \leq t < t_1 + t_2$), the second cycle [$(t_1 + t_2) \leq t < 2(t_1 + t_2)$], and a typical cycle after stead-state periodic conditions have been reached.

   ii) How many cycles are required to go from initial rest to steady-state conditions?

   iii) In steady state, determine the average load current, the amplitude of the variations in load current through one cycle, the average energy stored in the inductor, and the ratio of this stored energy to the energy dissipated in the load during one complete cycle.

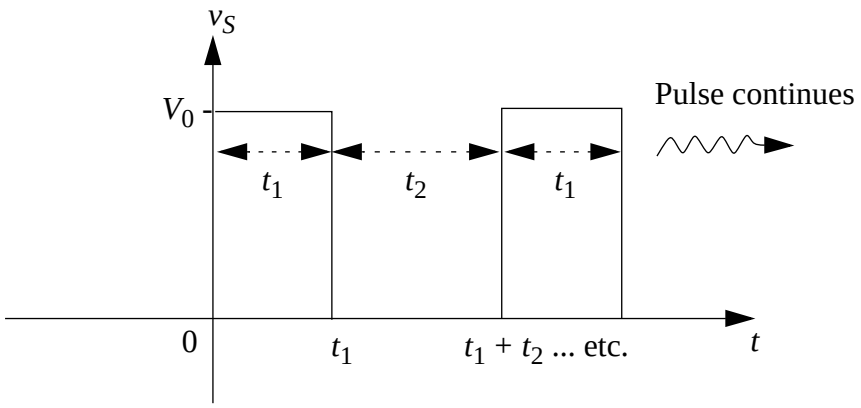


Figure 10.89:

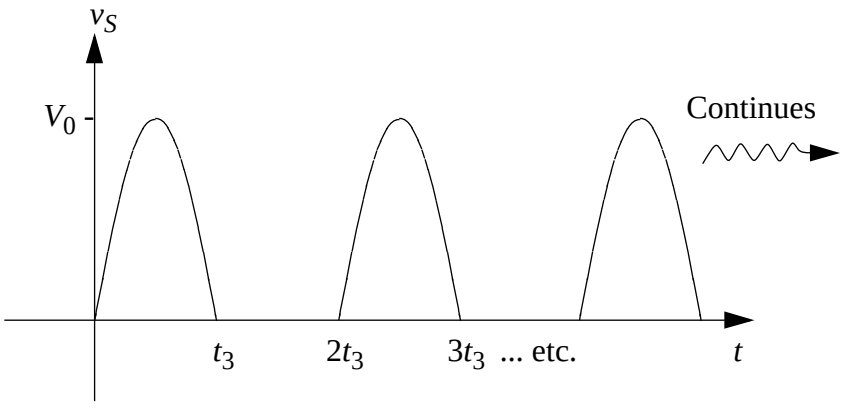


Figure 10.90:

b) Repeat part a) for the case where both t_1 and t_2 are short compared to the time constant of the network.

c) Now assume that as a filter designer, you are faced with the problem of selecting the inductor value to produce relatively smooth, ripple-free current in a load from a voltage source with a strongly pulsating value, such as the half-wave rectified sine wave shown. What method would you use to specify the inductor value with which to achieve a specified maximum variation in load current? Why might the specifications of a huge L value, much larger than might be needed, be a poor design?

d) Try your hand at a design: assume that the source waveform is half-wave rectified 60 hz 115 V AC, the load resistor is 16.2 Ohms, and it is desired to have a load current ripple of 5% of the average load current. Make reasonable approximations.

Solution:

For this entire problem, $\tau = L/R$.

a) Since both t_1 and t_2 are long compared to the time constant, the circuit will reach steady state during every cycle.

i) $0 < t \leq t_1$: $i(t) = \frac{V_0}{R}(1 - e^{-t/\tau})$
$t_1 < t \leq t_1 + t_2$: $i(t) = \frac{V_0}{R}e^{-(t-t_1)/\tau}$
Every other cycle will be identical to the first.

ii) It will only take one cycle to reach steady state. It will only take one cycle to reach steady state.

iii) We will assume that for the majority of each cycle, i(t) is either 0 Amps or $\frac{V_0}{R}$ Amps. In this case:
$i_{avg}(t) = \frac{V_0}{R}\frac{t_1}{t_1+t_2}$
The amplitude of the variations is V/R
$E_{L,avg} = \frac{1}{2}Li^2_{avg} = \frac{1}{2}L[\frac{V_0 t_1}{R(t_1+t_2)}]^2$
$E_{R_avg} = Ri^2_{avg} \Rightarrow \frac{E_{L,avg}}{E_{R,avg}} = \frac{L}{2R}$

b) For this section we will approximate each exponential rise and decay as a straight line, with a slope equal to the initial slope of the exponential.

i) $0 < t \leq t_1$: $i(t) = \frac{V_0}{R}\frac{1}{\tau}t = \frac{V_0 t}{L}$
$t_1 < t \leq t_1 + t_2$: $i(t) = \frac{V_0 t_1}{L} - \frac{V_0 t_1}{L\tau}t = \frac{V_0 t_1}{L}(1 - \frac{t-t_1}{\tau})$
$t_1 + t_2 < t \leq 2t_1 + t_2$:

$i(t) = \frac{1}{\tau}[\frac{V_0}{R} - \frac{V_0 t_1}{L}(1 - \frac{t_2}{\tau})]\ [t - (t_1 + t_2)]$
$= [\frac{V_0}{L} - \frac{V_0 t_1}{L\tau}(1 - \frac{t_2}{\tau})]\ [t - (t_1 + t_2)]$
$= \frac{V_0}{L}[1 - \frac{t_1}{\tau} + \frac{t_1 t_2}{\tau^2}]\ [t - (t_1 + t_2)]$

$2t_1 + t_2 < t \leq 2(t_1 + t_2)$:

As a shorthand, lets say $A = \frac{V_0}{L}[1 - \frac{t_1}{\tau} + \frac{t_1 t_2}{\tau^2}]$

$i(t) = At_1 - \frac{At_1}{\tau}[t - (2t_1 + t_2)]\ = At_1[1 - \frac{[t-(2t_1+t_2)}{\tau}]$

For steady state:

Once the circuit reaches steady state, the value of the current will oscillate between a high value (i_H) and a low value (i_L). Expressions for these two values follow.

$i_H = \frac{V_0/R - i_L}{\tau} t_1 + i_L$

$i_L = i_H - \frac{i_H}{\tau} t_2$

We now have two equations and two unknowns. Solving yields:

$i_H = \frac{\frac{V_0}{R} t_1 \tau}{\tau(t_1+t_2) - t_1 t_2}$

$i_L = \frac{\frac{V_0}{R} t_1 (\tau - t_2)}{\tau(t_1+t_2) - t_1 t_2}$

So in steady state $i(t)$ rises and falls linearly between i_H and i_L.

ii) Notice in the expression labeled A in part b) i) a pattern begins to emerge: $1 - \frac{t_1}{\tau} + \frac{t_1 t_2}{\tau^2}$. Since t_1 and t_2 are approximately equal when compared with τ, we can approximate the final term in this expression as $[\frac{nt_1}{\tau}]^n$, where n is the cycle number. The circuit has reached steady state when this term is reasonably close to zero. This is a subjective decision and is based on the values of t_1 and τ.

The circuit has reached steady state when $[\frac{nt_1}{\tau}]^n$ is approximately zero, where n is the cycle number.

iii) $i_{avg}(t) = \frac{i_H + i_L}{2} = \frac{\frac{V_0}{R} t_1 (\tau - \frac{t_2}{2})}{\tau(t_1+t_2) - t_1 t_2}$

The amplitude of variations is $i_H - i_L = \frac{\frac{V_0}{R} t_1 t_2}{\tau(t_1+t_2) - t_1 t_2}$

$E_{L,avg} = \frac{1}{2} L i_{avg}^2$ where i_{avg} is given above.

$E_{R_avg} = R i_{avg}^2 \Rightarrow \frac{E_{L,avg}}{E_{R,avg}} = \frac{L}{2R}$

c) We will approximate the sine wave as a square wave of decreased height, and so all previous calculations apply.

For the difference seen between parts a) and b), we much choose L such that the time constant is much larger that t_3. From the calculation of variations in $i(t)$ from part b) iii) we see that the ripple is inversely proportional to τ. We should choose L such that τ is large enough to achieve the minimum ripple. If L is chosen to be

larger than necessary, the current will take longer than necessary to reach steady state.

d) $t_3 = \frac{1}{60Hz} = 16.7ms$

$\frac{i_{ripple}}{i_{avg}} = 0.05 = = \frac{\frac{V_0}{R}t_3^2}{\frac{V_0}{R}t_3(\tau - \frac{t_3}{2})} = \frac{t_3}{\tau - \frac{t_3}{2}}$

$\tau = \frac{t_3}{0.05} + \frac{t_3}{2} = 342ms$

$L = \tau R = (342ms)(16.2\Omega) = 5.535H$

$L = 5.535H$

ANS:: (a) (i) $0 < t \leq t_1$: $i(t) = \frac{V_0}{R}(1 - e^{-t/\tau})$, $0 < t \leq t_1$: $i(t) = \frac{V_0}{R}(1 - e^{-t/\tau})$, $t_1 < t \leq t_1 + t_2$: $i(t) = \frac{V_0}{R}e^{-(t-t_1)/\tau}$ (ii) 1 (iii) $i_{avg}(t) = \frac{V_0}{R}\frac{t_1}{t_1+t_2}$, $E_{L,avg} = \frac{1}{2}L[\frac{V_0 t_1}{R(t_1+t_2)}]^2$, $\frac{E_{L,avg}}{E_{R,avg}} = \frac{L}{2R}$ (d) $L = 5.535H$

Problem 10.16 Consider the circuit shown in Figure 10.91.

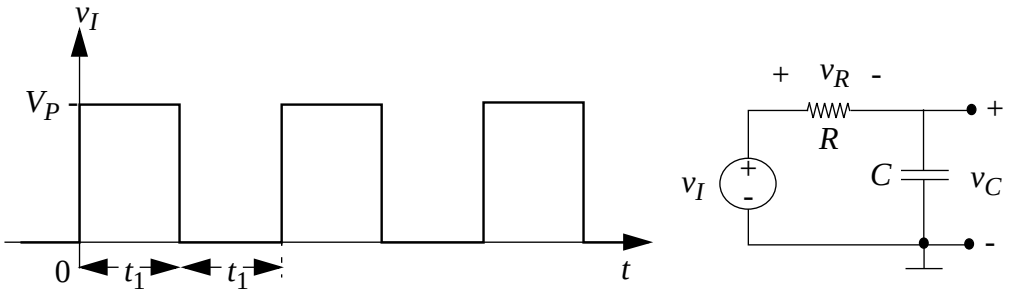


Figure 10.91:

a) Plot v_R and v_C for several cycles of the indicated input waveform. Assume the RC time constant is $10t_1$.

b) During the first several cycles, the v_C waveform does not repeat, but after some time, v_C is cyclic. Find and sketch this cyclic waveform. Dimension key values.

Solution:

a) Since $\tau \gg t_1$ we can approximate v_C as a series of straight lines. We will define these lines by their values at $t = t_1, 2t_1, 3t_1, \ldots$.

$v_C(t_1) = \frac{V_P}{10t_1}t_1 = 0.1V_P$

$v_C(2t_1) = 0.1V_P - \frac{0.1V_P}{10t_1}t_1 = 0.09V_P$

$v_C(3t_1) = 0.09V_P + \frac{V_P - 0.09V_P}{10t_1} t_1 = 0.181V_P$

A pattern appears.

For even n, $v_C[nt_1] = 0.9v_C[(n-1)t_1]V_P$

For odd n, $v_C[nt_1] = \{0.9v_C[(n-1)t_1] + 0.1\}V_P$

Using this pattern, we can easily graph v_C, as seen in Figure 10.92. $v_R = v_I - v_C$ as graphed in Figure 10.92.

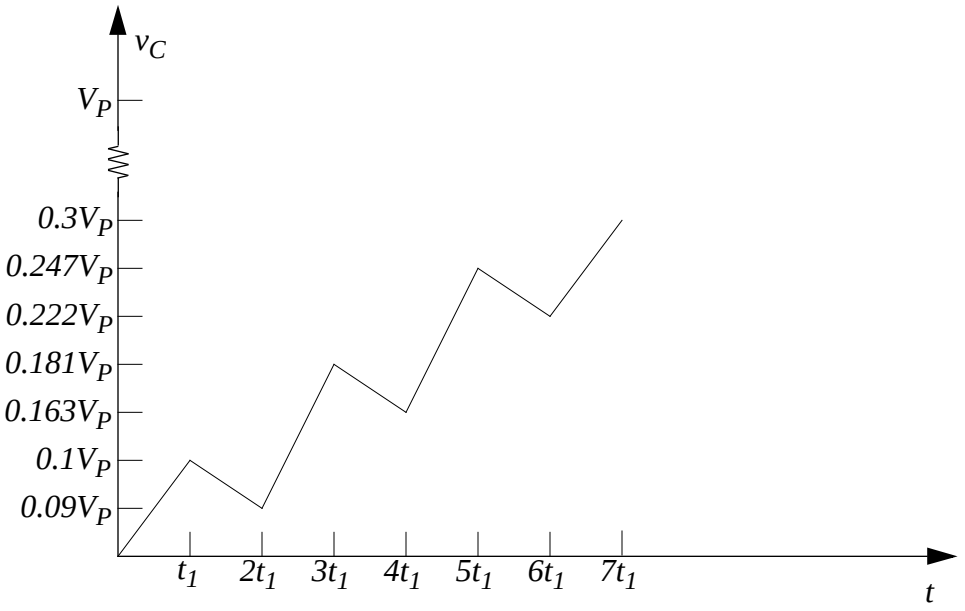


Figure 10.92:

See Figure 10.92. See Figure 10.93.

b) Once v_C becomes cyclic it will have some minimum value v_{MIN} and some maximum value v_{MAX}. From the pattern noted above, $v_{MIN} = 0.9v_{MAX}$. We also know that the average value of v_C is $V_P/2$ (see Problem 12).

$\frac{v_{MAX} + v_{MIN}}{2} = \frac{V_P}{2}$

$v_{MAX} + v_{MIN} = V_P$

$v_{MAX} + 0.9v_{MAX} = V_P$

$\Rightarrow v_{MAX} = 0.526V_P$ and $v_{MIN} = 0.474V_P$

See Figure 10.94.

Problem 10.17 Referring to Figure 10.95, for $v_I = Kt$, a ramp starting at $t = 0$, find expressions for v_R and v_L. Plot the waveforms.

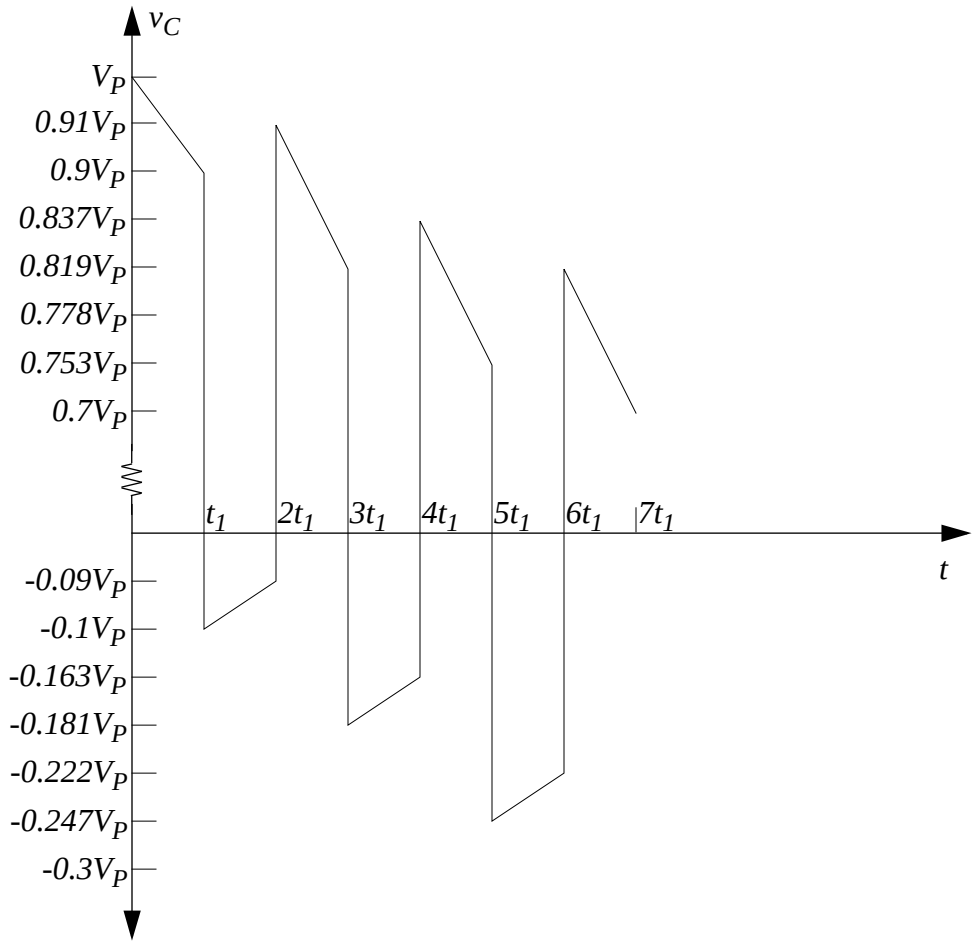

v_C
V_P
$0.91V_P$
$0.9V_P$
$0.837V_P$
$0.819V_P$
$0.778V_P$
$0.753V_P$
$0.7V_P$
t_1
$2t_1$
$3t_1$
$4t_1$
$5t_1$
$6t_1$
$7t_1$
t
$-0.09V_P$
$-0.1V_P$
$-0.163V_P$
$-0.181V_P$
$-0.222V_P$
$-0.247V_P$
$-0.3V_P$

Figure 10.93:

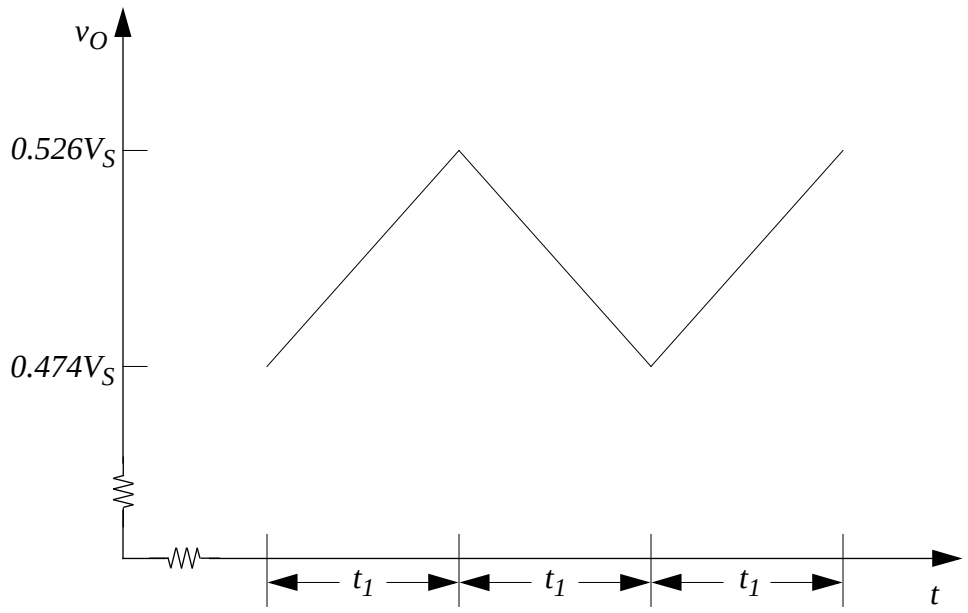


Figure 10.94:

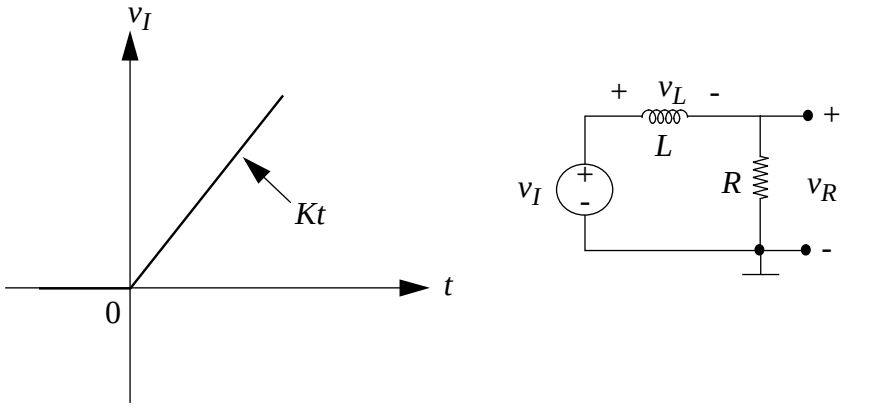


Figure 10.95:

Solution:

v_L is the integral of the inductor voltage in response to a step.

$v_L = K \int e^{-t/\tau} \quad \tau = L/R$

$v_L = -\tau K e^{-t/\tau} + \tau K$

Note that a constant of integration was added, whose value was determined using the initial condition of $v_L(0) = 0$.

$v_L = \tau K(1 - e^{-t/\tau})$

$v_R = v_I - v_L = Kt - \tau K(1 - e^{-t/\tau})$

See Figure 10.96 and Figure 10.97.

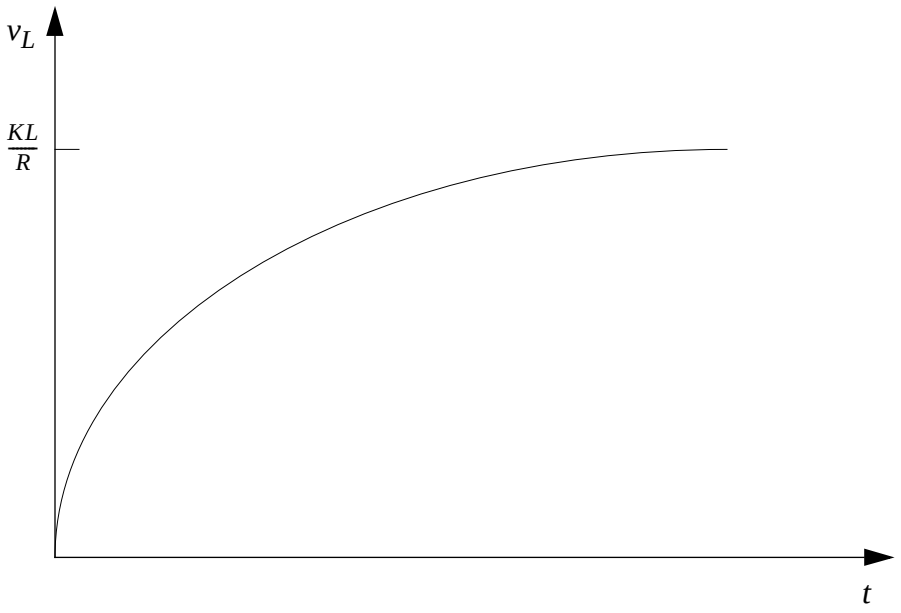


Figure 10.96:

ANS:: $v_L = \tau K(1 - e^{-t/\tau})$, $v_R = Kt - \tau K(1 - e^{-t/\tau}) \quad \tau = L/R$

Problem 10.18 Referring to Figure 10.98, given an initial inductor current $i_L(0) = 1mA$, find the expression for v_R and v_L. Plot the waveforms.

Solution:

We will solve this problem using superposition, treating the initial current through the inductor to be a third independant source. For the entire problem, $\tau = \frac{L}{2R}$.

Contribution from V_S:

$v_{L1}(0) = 0$

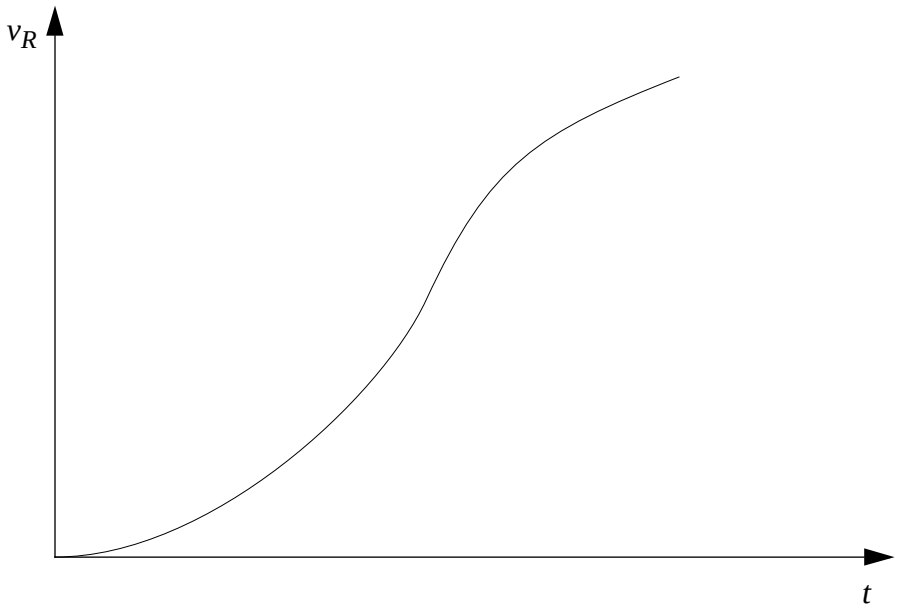


Figure 10.97:

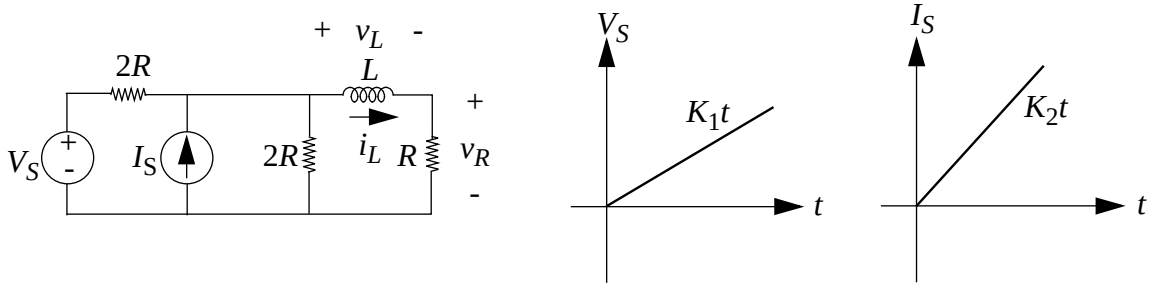


Figure 10.98:

$v_{L1} = \int \frac{K_1}{2} e^{-t/\tau} dt \; = -\frac{K_1 \tau}{2} e^{-t/\tau} + \frac{K_1 \tau}{2} \; = \frac{K_1 \tau}{2}(1 - e^{-t/\tau})$

Contribution from I_S:

$v_{L2}(0) = 0$

$v_{L2} = \int K_2 R e^{-t/\tau} dt \; = -K_2 \tau R e^{-t/\tau} + K_2 \tau R \; = K_2 \tau R(1 - e^{-t/\tau})$

Contribution from initial condition ($i_L(0) = 1mA$):

$i_L = 10^{-3} e^{-t/\tau}$

$v_{L3} = L\frac{di_L}{dt} = -\frac{L}{\tau} 10^{-3} e^{-t/\tau}$

$v_L = v_{L1} + v_{L2} + v_{L3} \; = (\frac{K_1 \tau}{2} + K_2 \tau R)(1 - e^{-t/\tau}) + \; -\frac{L}{\tau} 10^{-3} e^{-t/\tau}$

To find v_R we will first find the Thevenin equivalent of everything to left of the inductor and resistor of interest. The Thevenin voltage is $V_S/2 + I_S R$. The Thevenin resistance is R. See Figure 10.99.

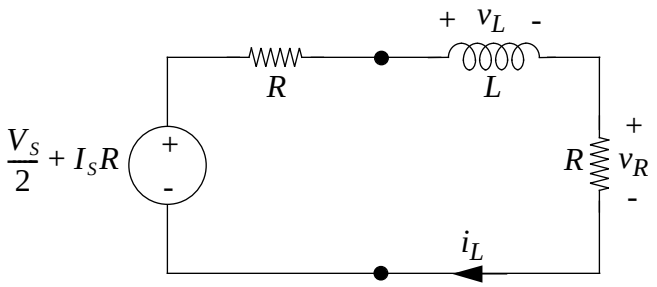


Figure 10.99:

From this we can see the following relation for v_R.

$v_R = \frac{1}{2}(V_S/2 + I_S R - v_{L_S}) + i_L R$ where v_{L_S} is the inductor voltage due only to the sources and i_L is the inductor current due only to the initial conditions.

$v_R = (\frac{K_1}{4} + \frac{K_2 R}{2})t - \; (\frac{K_1 \tau}{4} + \frac{K_2 \tau R}{2})(1 - e^{-t/\tau}) + \; 10^{-3} R e^{-t/\tau}$

See Figure 10.100 and Figure 10.101.

ANS:: $v_L = (\frac{K_1 \tau}{2} + K_2 \tau R)(1 - e^{-t/\tau}) + -\frac{L}{\tau} 10^{-3} e^{-t/\tau}$, $v_R = (\frac{K_1}{4} + \frac{K_2 R}{2})t - (\frac{K_1 \tau}{4} + \frac{K_2 \tau R}{2})(1 - e^{-t/\tau}) + 10^{-3} R e^{-t/\tau}$

Problem 10.19 The purpose of this problem is to illustrate the important fact that although the *zero-state response* of a linear circuit is a linear function of its input, the complete response is not. Consider the linear circuit shown in Figure 10.102.

a) Let $i(0) = 2mA$. Let i_1 and i_2 be the responses resulting from voltages e_1 and e_2 applied one at a time, where

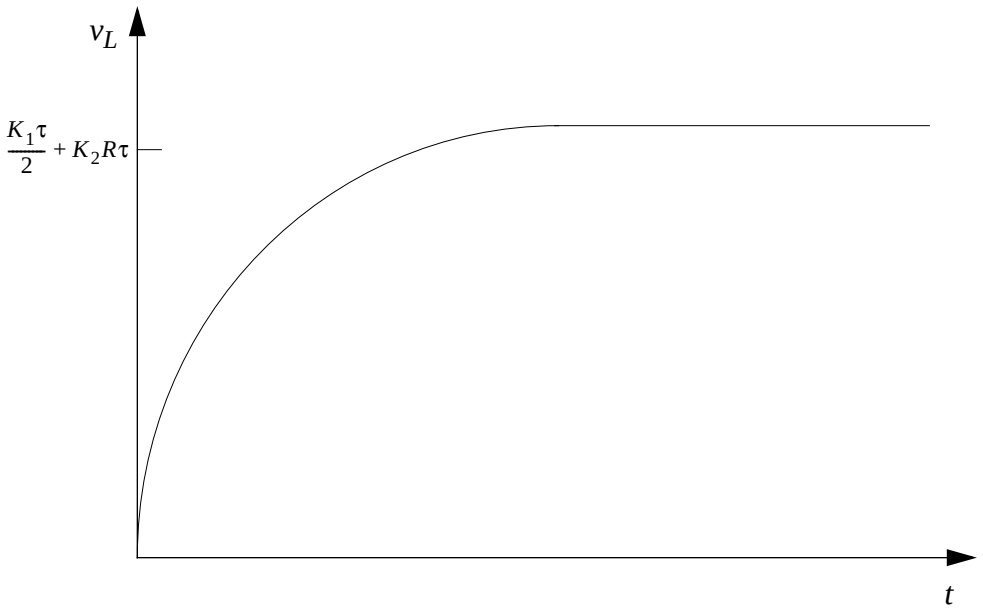


Figure 10.100:

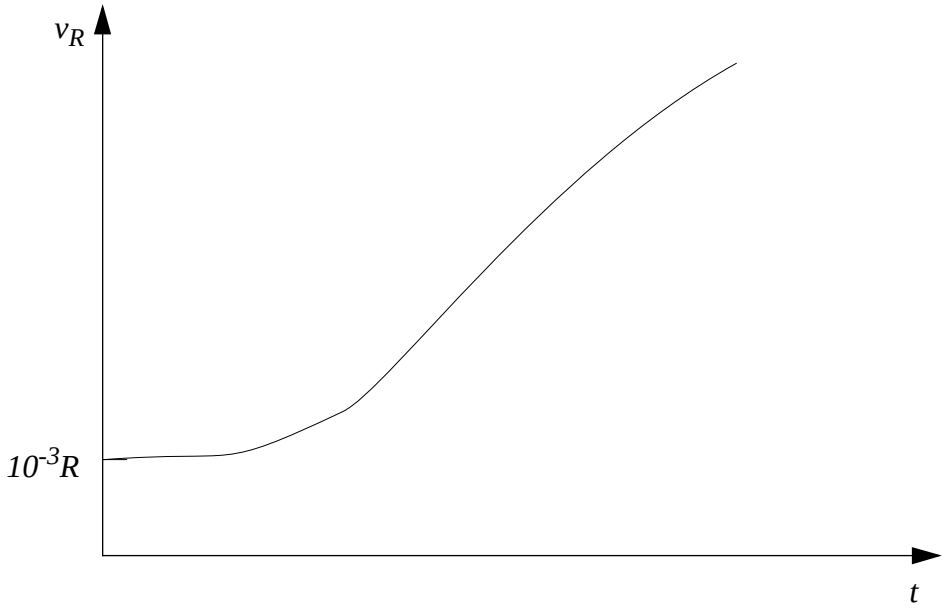


Figure 10.101:

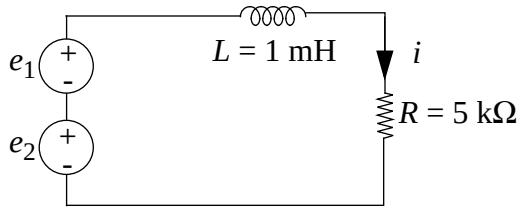


Figure 10.102:

$$e_1 = \begin{cases} 0, & t < 0 \\ 10\ volts, & t \geq 0 \end{cases} \tag{10.1}$$

$$e_2 = \begin{cases} 0, & t < 0 \\ 20\ volts, & t \geq 0 \end{cases} \tag{10.2}$$

Plot i_1 and i_2 as functions of t. Is it true that $i_2(t) = 2i_1(t)$ for all $t \geq 0$?

b) Consider now the zero-state responses due to e_1 and e_2; call them $i_1'(t)$ and $i_2'(t)$. Plot i_1' and i_2' as functions of t. Is it true that $i_2'(t) = 2i_1'(t)$ for all $t \geq 0$?

Solution:

For the entire problem $\tau = L/R = 0.2s$.

a) See Figure 10.103 and Figure 10.104.

It is not true that $i_2(t) = 2i_1(t)$ for all $t \geq 0$.

b) See Figure 10.105 and Figure 10.106.

It is true that $i_2'(t) = 2i_1'(t)$ for all $t \geq 0$.

ANS:: (a) not true (b) true

Problem 10.20 In the circuit shown in Figure 10.107, the switch opens at $t = 0$. Sketch and label $i_L(t)$ and $v_L(t)$.

$v_1 = 5V \quad v_2 = 3V, \quad R_1 = 2k, \quad R_2 = 3k, \quad L = 4mH$

Solution:

$\tau = \frac{L}{R_1 \| R_2} = 3.33s.$

$i_L(0^-) = V_1/R_1 + V_2/R_2 = 2.5mA + 1mA = 3.5mA$

$i_L(t \to \infty) = V_1/R_1 = 2.5mA$

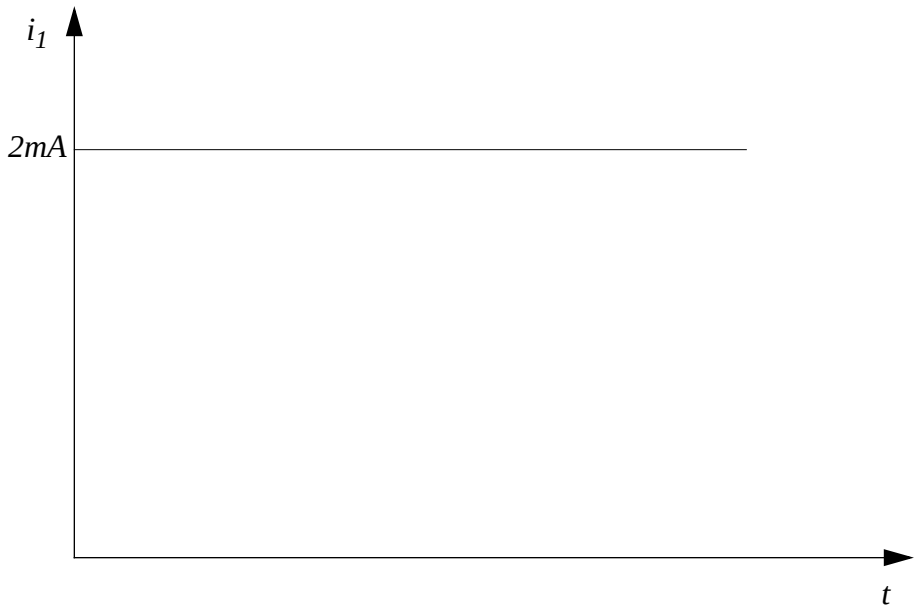


Figure 10.103:

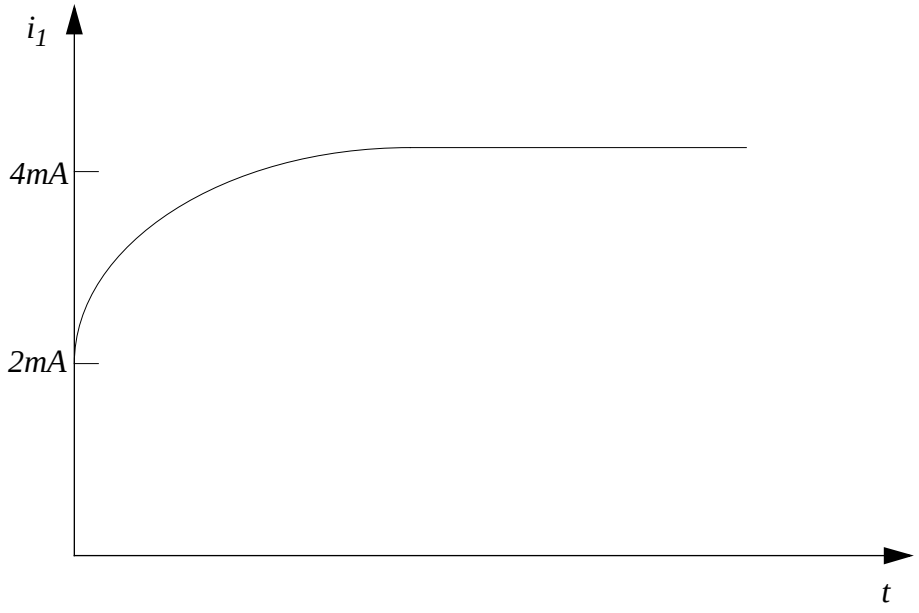


Figure 10.104:

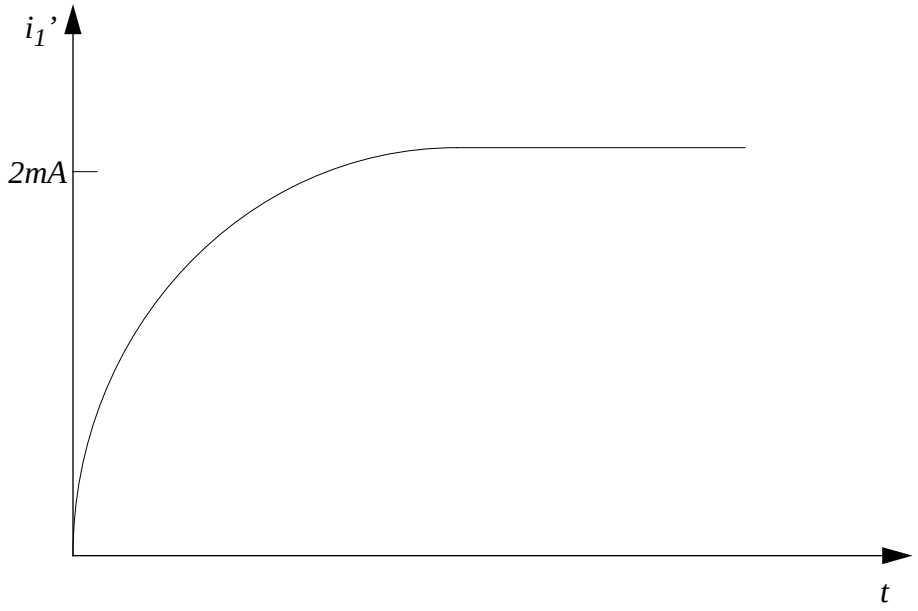


Figure 10.105:

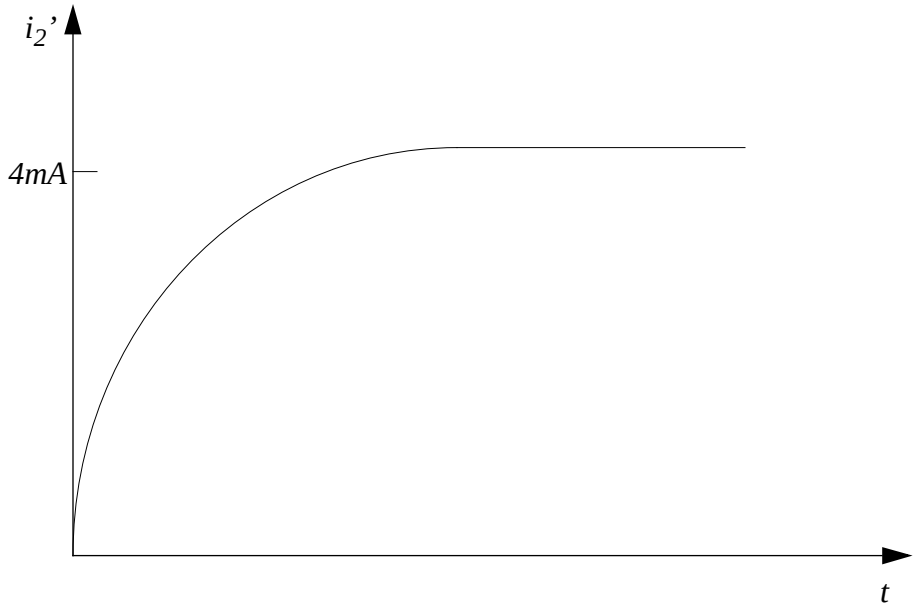


Figure 10.106:

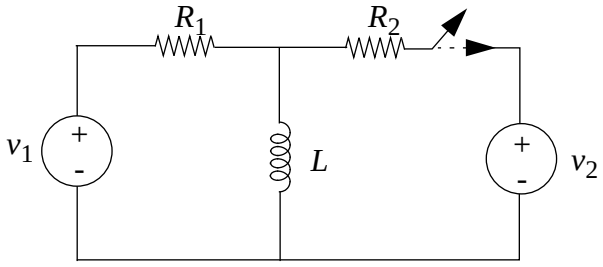


Figure 10.107:

$i_L(t) = 2.5 + e^{-t/\tau}[mA]$

$v_L(t) = L\frac{di_L}{dt} = \frac{L}{\tau}e^{-t/\tau}[mV] \ = -R_1 \parallel R_2 e^{-t/\tau}[mV] \ = -1.2e^{-t/\tau}[V]$

See Figure 10.108 and Figure 10.109.

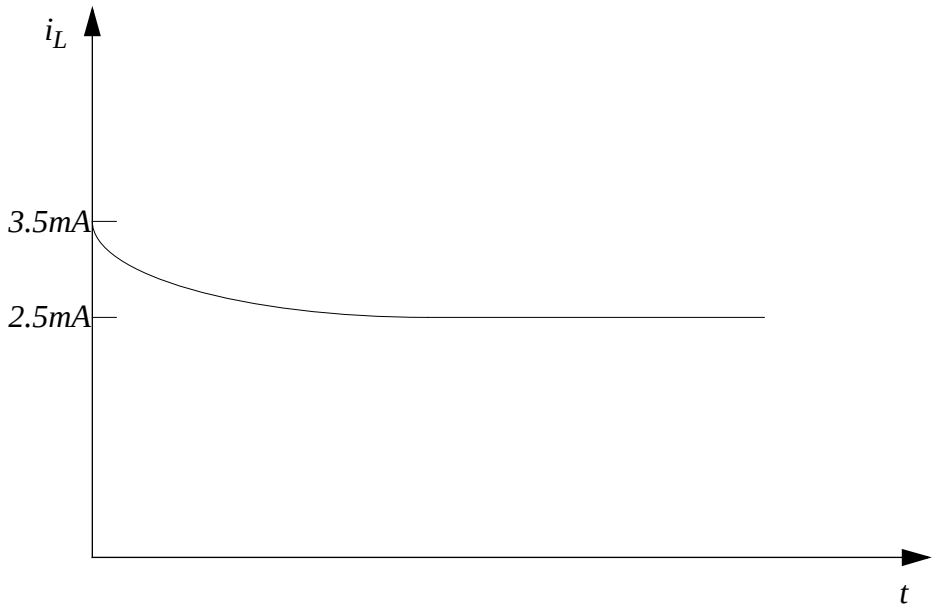


Figure 10.108:

It is not true that $i_2(t) = 2i_1(t)$ for all $t \geq 0$.

Problem 10.21 A two-input RC circuit is shown in Figure 10.110.

Consider operation with $i_I(t) = 0$, $v_I(t) = 0$ for $t \geq 0$. The voltage $v_O(t)$ is known to be 1 volt at time $t = 0$. Determine $v_O(t)$ for all $t > 0$.

A different constraint is that sources $i_I(t)$ and $v_I(t)$ are zero for $t < 0$ and that $v_O(0) = 0$. Sources $i_I(t)$ and $v_I(t)$ undergo step transitions of +1 mA and +1 volt respectively at time $t = 0$. Determine $v_O(t)$ for all time.

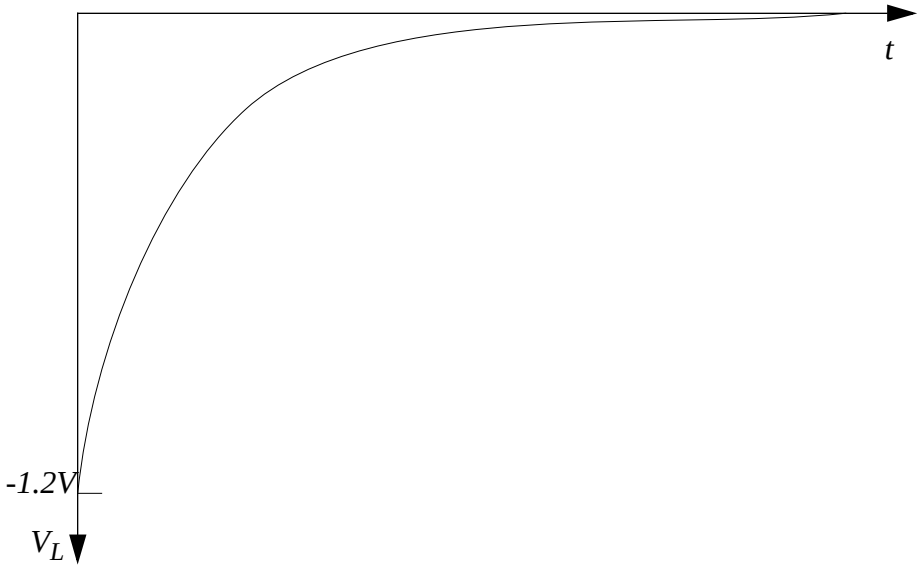


Figure 10.109:

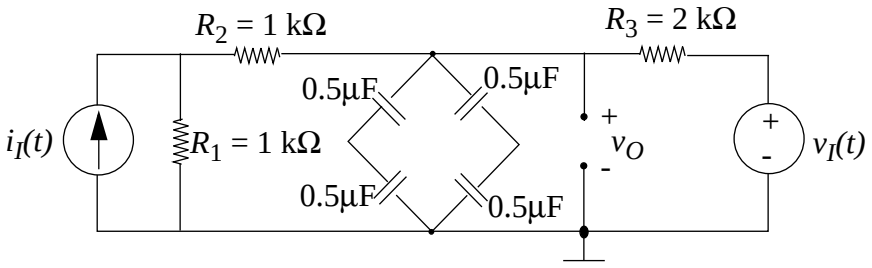


Figure 10.110:

Solution:

The four $0.5\mu F$ capacitors can be combined into one $0.5\mu F$ capacitor, which will be called C.

For the whole problem $\tau = R_{th}C = 0.5ms$.

First constraint (initial condition and no sources):

$v_O = e^{-t/\tau}$

Second Constraint (sources and no initial condition):

$v_O = 1mA\frac{1k}{1k+3k}2k(1 - e^{-t/\tau}) + \frac{1}{2}(1 - e^{-t/\tau}) = 1 - e^{-t/\tau}$

ANS:: First: $v_O = e^{-t/\tau}$, Second: $v_O = 1 - e^{-t/\tau}$ $\tau = 0.5$ ms.

Problem 10.22 The neon bulb in the circuit shown in Figure 10.111 has the following behavior: the bulb remains off and acts as an open circuit until the bulb voltage v reaches a threshold voltage $V_T = 65V$. Once v reaches V_T, a discharge occurs and the bulb acts like a simple resistor of value $R_N = 1k\Omega$; the discharge is maintained as long as the bulb current i remains above the value $I_S = 10mA$ needed to sustain the discharge (even if the voltage v drops below V_T). As soon as i drops below 10 mA, the bulb again becomes an open circuit.

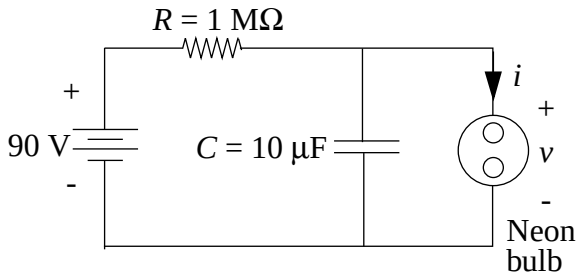


Figure 10.111:

a) Sketch and dimension $v(t)$ and $i(t)$, showing the first and second charging intervals.

b) Estimate the flashing rate.

Solution:

a) Charging ($v < 60V$):

$\tau_c = RC = (1M\Omega)(10\mu F) = 10s.$

$v_{charging} = 90(1 - e^{-t/\tau_c})$

Discharging ($i > 10mA$):

$\tau_d = R_{eq}C = \frac{1M\Omega \cdot 1k\Omega}{1M\Omega + 1k\Omega}\ 10\mu F = 10ms$

Note that when discharging v approaches $90\frac{1k\Omega}{1M\Omega+1k\Omega} \cong 0$. Also note that $\tau_c \gg \tau_d$ so the charging time is much longer than the discharging time.

$v_{discharge} = 65e^{-t/\tau_d}$

The minimum v when discharging is $v_{min} = i_{min}/R = 10mA/1k\Omega = 10V$.

See Figure 10.112.

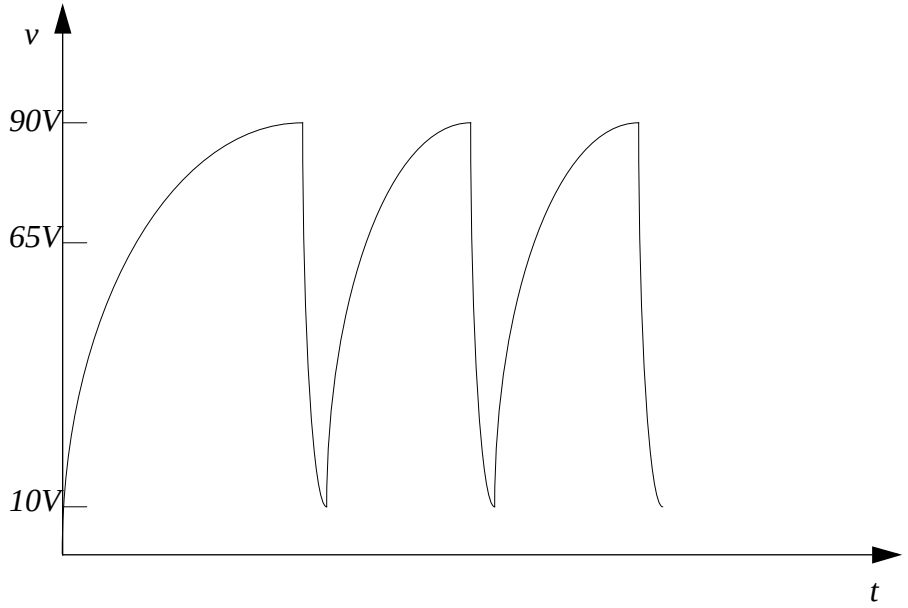


Figure 10.112:

b) Since the discharge time is so small in comparison to the charge time, we will only consider the charge time.

After the first charging cycle, $v_{charging} = 90 + (10 - 90)e^{-t/\tau_c}$. The charging time, t_c is the amount of time it takes for $v_{charging}$ to reach 65 V.

$t_c = -\tau_c \ln\left(\frac{90-65}{80}\right) = 11.63s.$

Therefore the flashing rate is once every 11.63 s.

ANS:: (b) $1/11.63sec$

Problem 10.23 Because of the input resistance and capacitance of an oscilloscope, laboratory observations of transients, such as the step response of the $R_1 - C_1$ circuit in Figure 10.113 may have errors in them.

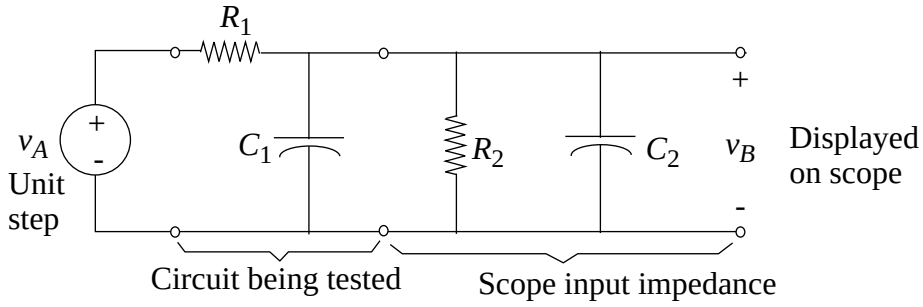


Figure 10.113:

a) Assuming that the effect of connecting the oscilloscope to the circuit under test is to add R_2 and C_2 as shown in Figure 10.113, find and sketch the step response that will be observed at v_B in the above circuit. Discuss the errors introduced by the scope by comparing your result to what would be observed if the scope were ideal ($R_2 \to \infty, C_2 \to 0$). Assume zero initial state.

b) A common method of coping with the errors of part a) is to use a compensated attenuator in series with the scope (see in Figure 10.114). For simplicity, we examine what the compensated scope displays when it is connected directly to the unit step *without* the $R_1 - C_1$ circuit of part a). Assume zero initial state before the step is applied.

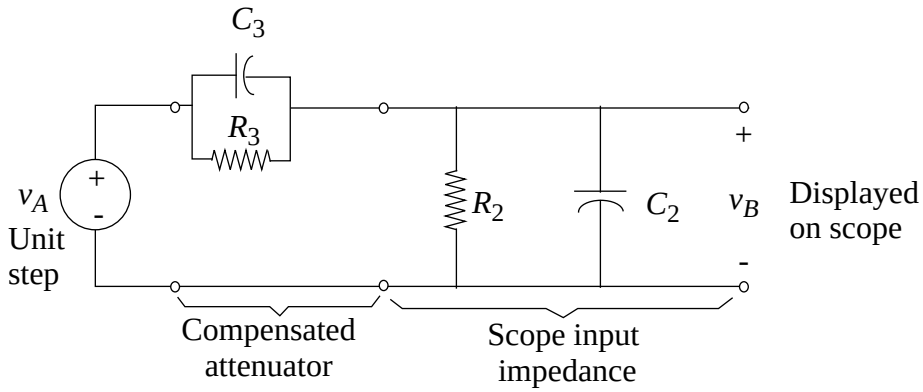


Figure 10.114:

i) What is v_B immediately after the step is applied, i.e. at $t = 0^+$?

ii) What is v_B as $t \to \infty$?

iii) Using your results, find $v_B(t)$ for all t.

iv) What conditions on R_2, C_2, R_3 and C_3 must be satisfied in order that there be no natural response component, i.e. no transient, in $v_B(t)$? What is $v_B(t)$ in this case?

Solution:

a) $\tau = (C_1 + C_2)(R_1 \parallel R_2)$
$v_B = v_A \frac{R_2}{R_1+R_2}(1 - e^{-t/\tau})$
See Figure 10.115.

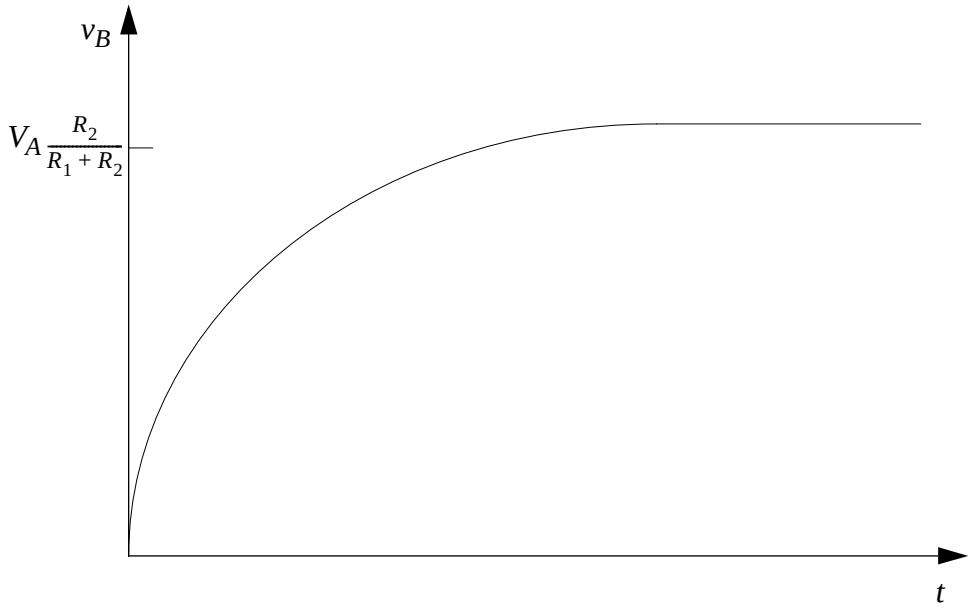


Figure 10.115:

b) i) $v_B(0^-) = 0$
ii) $v_B(t \to \infty) = v_A \frac{R_2}{R_3+R_2}$
iii) $v_B(t) = v_A \frac{R_2}{R_1+R_2}(1 - e^{-t/\tau})$
$\tau = (C_2 \parallel C_3)(R_2 \parallel R_3) = (C_2 + C_3)\frac{R_1 R_2}{R_1+R_2}$
iv) There will be no transients if $C_2 R_2 = C_3 R_3$. In this case, $v_B(t) = v_A \frac{R_2}{R_1+R_2}$

ANS:: (a) $v_B = v_A \frac{R_2}{R_1+R_2}(1 - e^{-t/\tau})$, $\tau = (C_2 + C_3)\frac{R_1 R_2}{R_1+R_2}$ (b) (i) $v_B(0^-) = 0$ (ii) $v_B(t \to \infty) = v_A \frac{R_2}{R_3+R_2}$ (iii) $v_B(t) = v_A \frac{R_2}{R_1+R_2}(1 - e^{-t/\tau})$ $\tau = (C_2 + C_3)\frac{R_1 R_2}{R_1+R_2}$ (iv) $v_B(t) = v_A \frac{R_2}{R_1+R_2}$

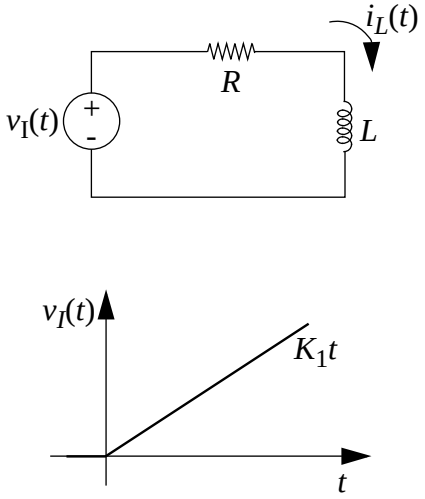


Figure 10.116:

Problem 10.24 The RL circuit shown in Figure 10.116 is driven with the ramp $v_I(t) = K_1t$, for t greater than zero, and $v_I(t) = 0, t < 0$.

a) Assuming $i_L(0^-) = 0$, sketch the current $i_L(t)$. Also find an analytic expression for $i_L(t)$.

b) In some applications, such as generating a linear sweep for a magnetically deflected cathode-ray tube, we want to make $i_L(t)$ a linear ramp as shown in Figure 10.117.

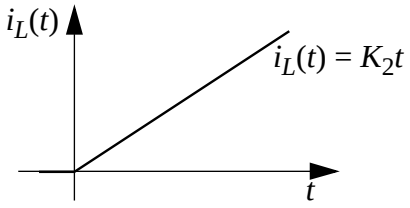


Figure 10.117:

Find a new input waveform $v_I(t)$ such that $i_L(t) = K_2t, t > 0$. Plot $v_I(t)$. Label all values and slopes.

Solution:

a) $\tau = L/R$

$i_L(0^+) = 0$

$i_L(t) = \int \frac{K_1}{R}(1 - e^{-t/\tau})dt \; = \frac{K_1t}{R} + \frac{K_1\tau}{R}e^{-t/\tau} - \frac{K_1\tau}{R}$

$i_L(t) = \frac{K_1 t}{R} - \frac{K_1 \tau}{R}(1 - e^{-t/\tau})$

See Figure 10.118.

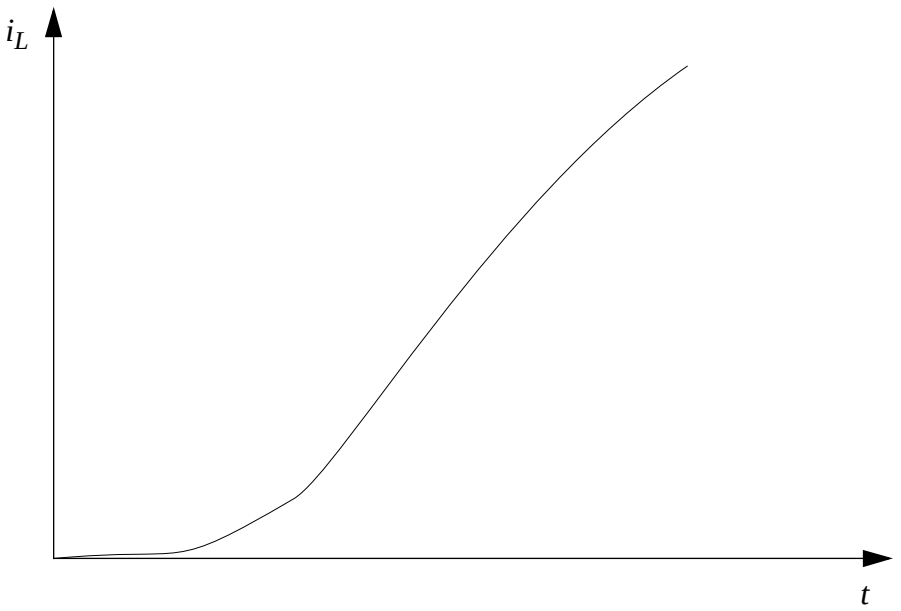


Figure 10.118:

b) $i_L = K_2 t$

$v_L = L\frac{di_L}{dt} = LK_2$

$v_R = Ri_L = RK_2 t$

$v_I = v_L + v_R = LK_2 + RK_2 t$

See Figure 10.119.

ANS:: (a) $i_L(t) = \frac{K_1 t}{R} - \frac{K_1 \tau}{R}(1 - e^{-t/\tau}) \quad \tau = L/R$ (b) $v_I = v_L + v_R = LK_2 + RK_2 t$

Problem 10.25 For the RL circuit shown in Figure 10.120, sketch and label v_R versus time for $t > 0$. Assume $i_L(t < 0) = 0$, and that T_1 is five times as long as the circuit time constant.

Solution:

The until $t = T_1$ the input can be treated as a step of height A/T_1. During this time v_R simply rises exponentially to A/T_1. The short pulse after $t = T_1$ will be treated as an impulse of area A. Taking $t = T_1$ to be our new $t = 0$ and no initial state we have the following.

$v_R = -A\frac{d}{dt}(1 - e^{-t/\tau}) = -\frac{A}{\tau}e^{-t/\tau}) \; = -\frac{5A}{T_1}e^{-t/\tau}$

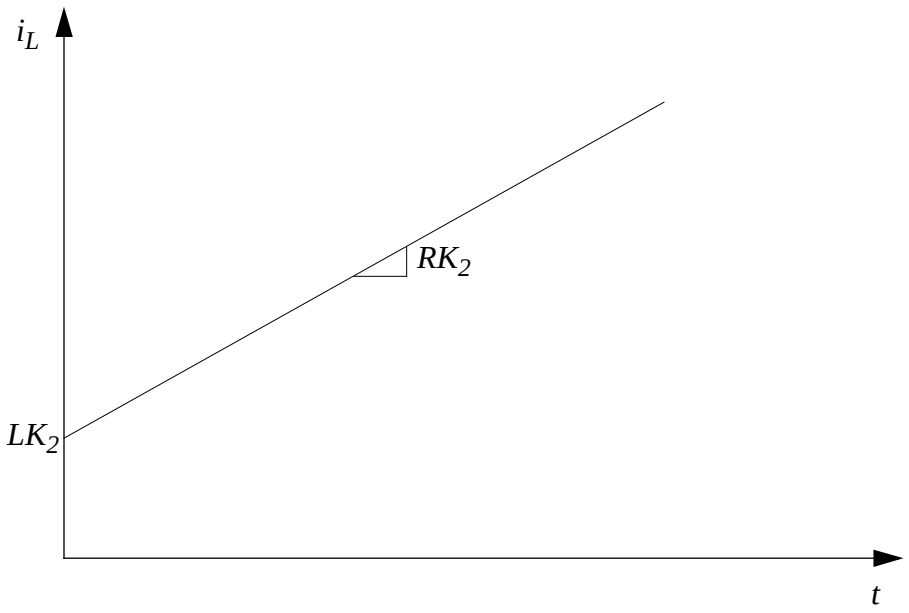


Figure 10.119:

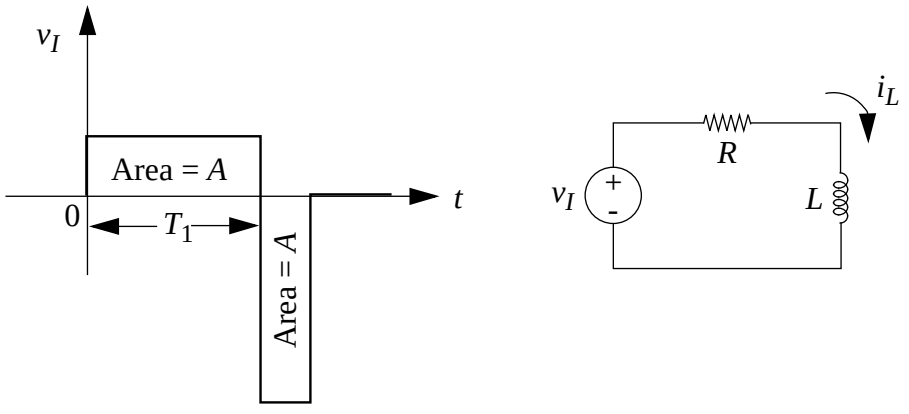


Figure 10.120:

Add to this the initial condion that $v_R(0) = \frac{A}{T_1}$ and we have $v_R = -\frac{4A}{T_1}e^{-t/\tau}$.

See Figure 10.121.

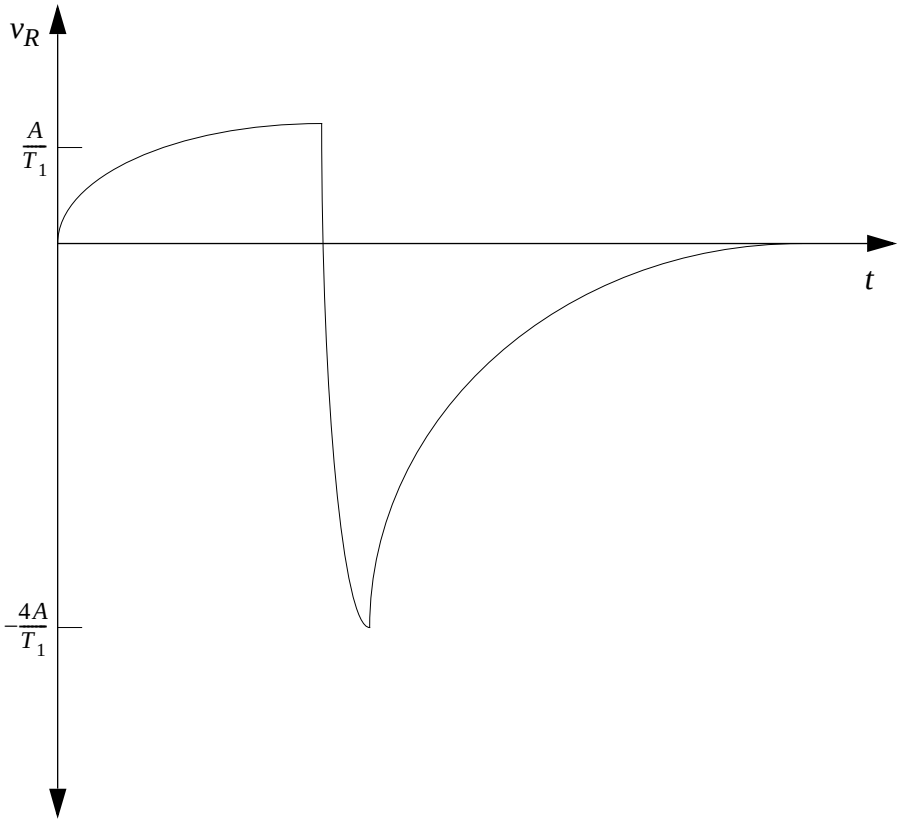


Figure 10.121:

Problem 10.26 With the capacitor initially at rest ($v_C(0) = 0$) and disconnected, the switch is closed to position (1) at time $t = 0$ in Figure 10.122.

a) Sketch the waveform $v_C(t)$ for $t > 0$. Label all relevant points on the figure and calculate the time constant.

b) At a time $T > 0$ (at least five time constants later), the switch is thrown (instantaneously) to position (2). Sketch $v_C(t)$ for $t > T$ and label all relevant points on the figure.

c) With $R_1 = R_2 = R_3$, is the time constant in part (a) greater than, less than or equal to the time constant in part (b)?

Solution:

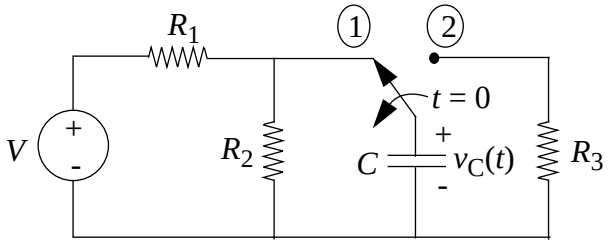


Figure 10.122:

a) $v_C(t) = V\frac{R_2}{R_1+R_2}(1 - e^{-t/\tau})$

$\tau = C\frac{R_1R_2}{R_1+R_2}$

See Figure 10.123.

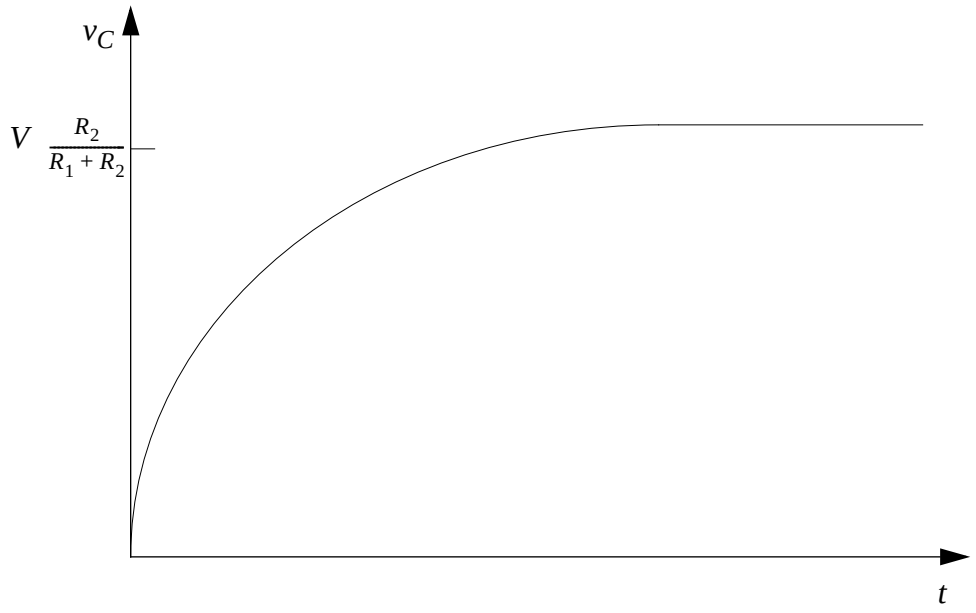


Figure 10.123:

b) $v_C(t) = V\frac{R_2}{R_1+R_2}e^{-t/\tau}$

$\tau = CR_3$

See Figure 10.124.

c) The time constant in part (a) is greater than the time constant in part (b).

Problem 10.27 For the circuit shown in Figure 10.125, sketch and label v_R versus time. Assume that $v_I = K_1$ for a long time prior to $t = 0$ as illustrated in the figure.

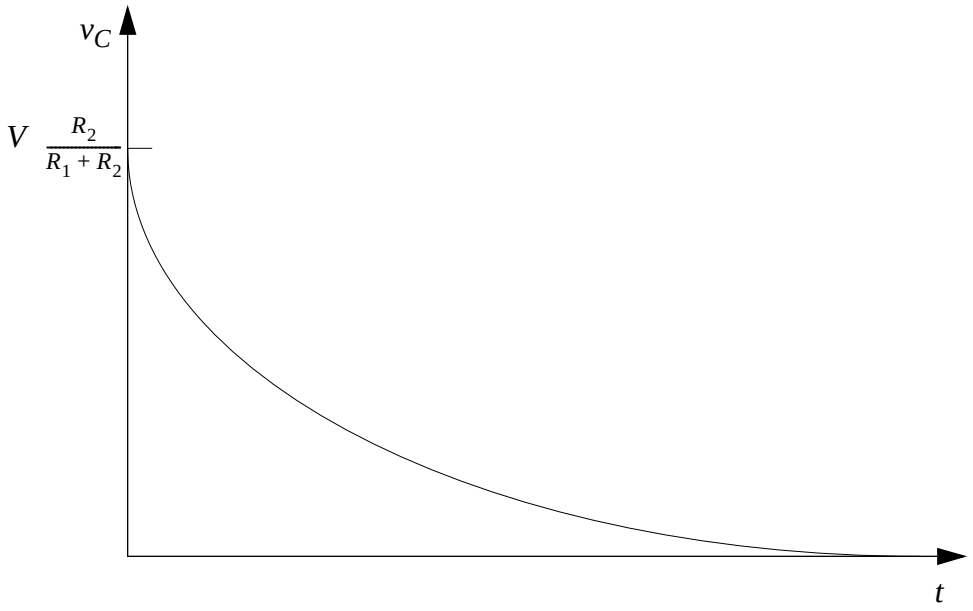


Figure 10.124:

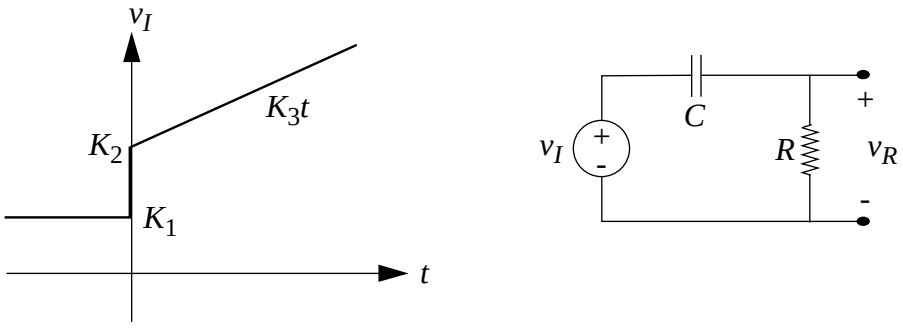


Figure 10.125:

Note that this problem can be solved in a number of simple steps by breaking the problem down into parts and solving each part. There are several ways to do this breakdown, all of roughly equal ease.

Solution:

For $t > 0$, v_I consists of a step of height K_2 plus a ramp of slope K_3. We will use superposition to solve this problem, treating the step, the ramp, and the initial condition as three seperate inputs. Forthe entire problem, $\tau = RC$.

Initial Condition:

$v_{R1} = -v_C = -K_1 e^{-t/\tau}$

Step:

$v_{R2} = K_2 e^{-t/\tau}$

Ramp:

$v_{R3}(0) = 0$

$v_{R3} = \int K_3 e^{-t/\tau} dt = -K_3\tau e^{-t/\tau} + K_3\tau \ = K_3\tau(1 - e^{-t/\tau})$

Total:

$v_R = (K_2 - K_1)e^{-t/\tau} + K_3\tau(1 - e^{-t/\tau})$

See Figure 10.126.

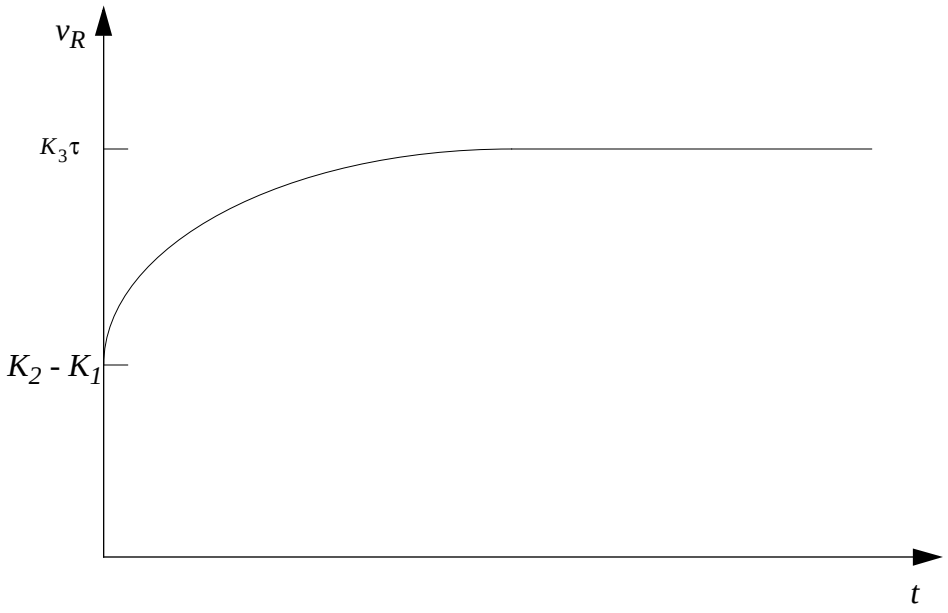


Figure 10.126:

ANS:: $v_R = (K_2 - K_1)e^{-t/\tau} + K_3\tau(1 - e^{-t/\tau})$

Problem 10.28 You are given the RC circuit shown in Figure 10.127.

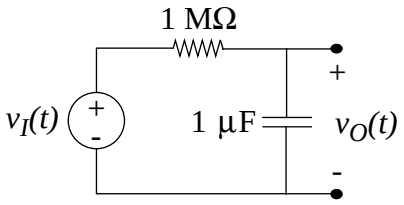


Figure 10.127:

a) Suppose you observe that $v_O(t)$ is a triangular pulse, as shown in the sketch in Figure 10.128. Find and draw the waveform $v_I(t)$ which must be applied to produce this output signal. Label times and magnitudes, and significant parameters of the function.

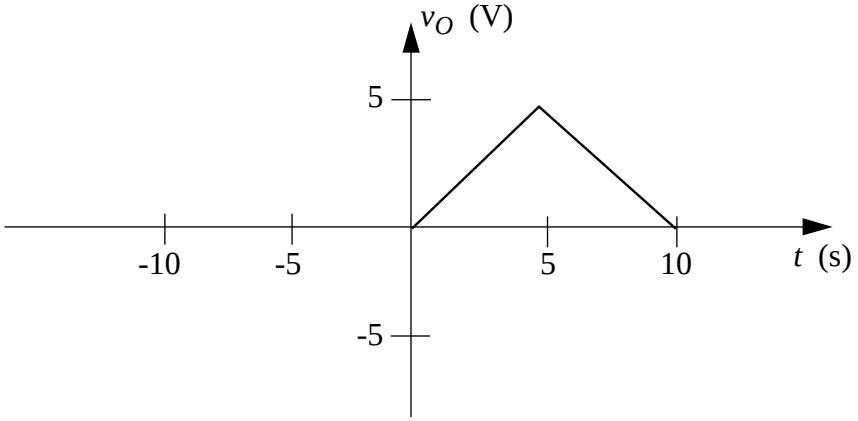


Figure 10.128:

b) Now the input signal is changed. You apply a ramp starting at $t = 0, v_I(t) = tu_{-1}(t)$, as the input signal $v_I(t)$. (Note that $u_{-1}(t)$ represents a unit step at $t = 0$.) Sketch and label the output signal $v_O(t)$ for $0 < t < 5$.

c) Give an analytic expression for the output signal $v_O(t)$ you sketched in (b).

Solution:

a) $v_I = RC\frac{dv_O}{dt} + v_O$

$0 < t < 5$: $v_O = 1 + t$

$5 < t < 10$: $v_O = -1 + (10 - t) = 9 - t$

See Figure 10.129.

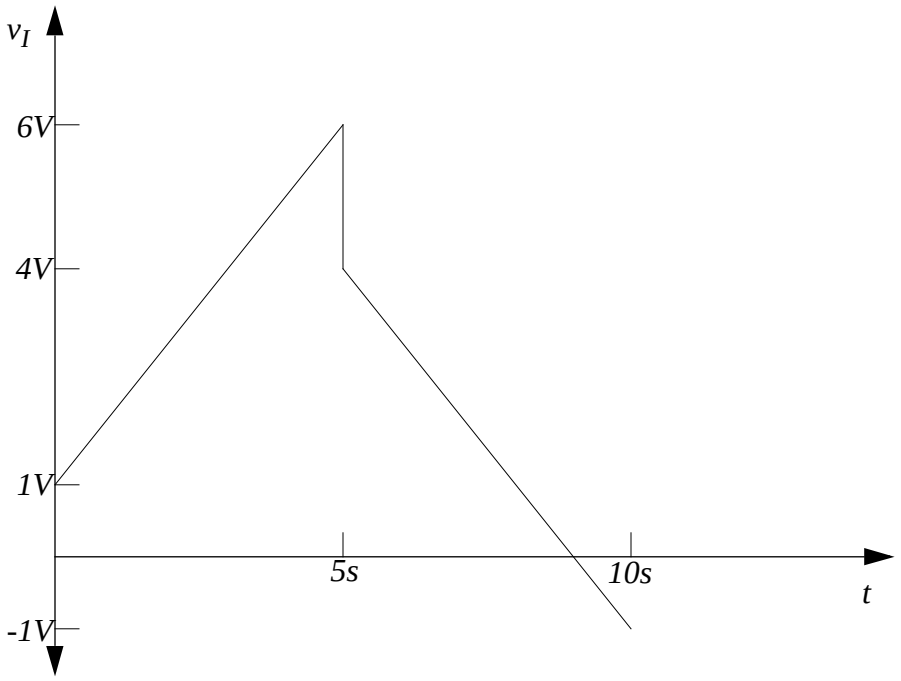


Figure 10.129:

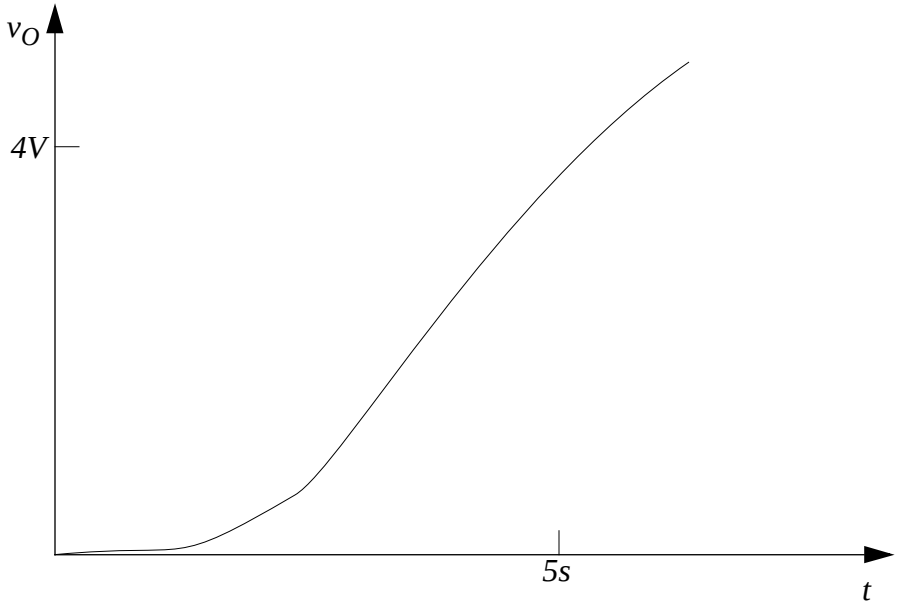


Figure 10.130:

b) See Figure 10.130.

c) $v_O(t) = \int (1 - e^{-t/\tau})dt = t + \tau e^{-t/\tau} - \tau \ = t - \tau(1 - e^{-t/\tau})$
$\tau = RC = 1s$
$v_O(t) = t - 1 + e^{-t}$

ANS:: (a) $0 < t < 5$: $v_O = 1 + t$, $5 < t < 10$: $v_O = -1 + (10 - t) = 9 - t$ (c) $v_O(t) = t - 1 + e^{-t}$

Problem 10.29 Consider the digital memory element shown in Figure 10.131. The voltage at the storage node with respect to ground is denoted v_M. The figure also shows a parasitic resistance R_P from the storage node to ground. This resistance will cause a leakage of the charge stored in the memory.

The signal A is fed to an inverter and the inverter drives the input d_{IN} of the memory element. All inverters shown in the figure have a load resistor R_L and the on resistance of the pulldown MOSFETs in each of the inverters is R_{ON}. Assume that the on resistance of the switch driven by the *Store* signal is also R_{ON}. The supply voltage is V_S and the threshold voltage for the MOSFETs is V_T. In doing this problem, assume that R_P is much larger than either R_{ON} or R_L.

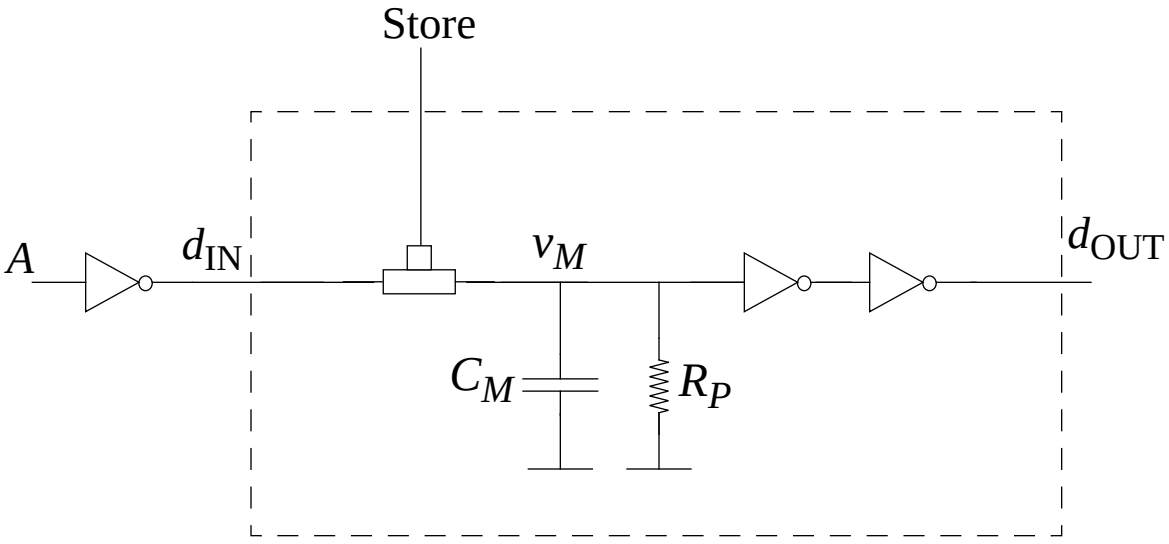


Figure 10.131:

a) Suppose that a 0V to V_S step is applied at the *Store* input of the memory element at $t = 0$. Sketch $v_M(t)$ for $t \geq 0$, assuming that $v_M(t = 0) = 0$, and that A is at 0V throughout. Assuming that $R_{ON} << R_P$, what is the maximum value attained by v_M?

b) Suppose, now, that a rectangular *pulse* of height V_S is applied at the *Store* input of the memory element, and that A is at 0V throughout. The rising transition of the pulse occurs at $t = 0$ and the falling transition at $t = T$. Determine the minimum value of the pulse width T so that v_M can charge up to V_H, where $V_H = V_{IH} = V_{OH}$, the high voltage threshold of the static discipline. Assume the following: $v_M(t = 0) = 0$; $V_H < V_S$; $V_H > V_T$;

c) Let us now consider the case in which A is at V_S throughout, and $v_M(t = 0) = V_S$. Sketch $v_M(t)$ for $t \geq 0$, when a 0V to V_S step is applied at the *Store* input of the memory element at $t = 0$. What is the minimum value attained by v_M?

d) Suppose, now, that a rectangular *pulse* of height V_S is applied at the *Store* input of the memory element. The rising transition of the pulse occurs at $t = 0$ and the falling transition at $t = T$. Determine the minimum value of the pulse width T so that v_M can discharge from V_S to V_L, where $V_L = V_{IL} = V_{OL}$, the low voltage threshold of the static discipline. Assume as in (c) that A is at V_S throughout and that $v_M(t = 0) = V_S$. Assume further that $V_L < V_T$ and that V_L is greater than the minimum value attainable by v_M.

e) Suppose the memory element is storing a 1 (assume $v_M = V_S$) at $t = 0$ and that *Store = 0*. Assuming that no further *Store* signals occur, determine the period of time for which the output (d_{OUT}) of the memory element will be valid. (Hint: the output becomes invalid when d_{OUT} switches from 1 to 0.)

Solution:

a) See Figure 10.132.

V_S

Assuming R_P is much larger than R_L.

b) $T_{min} = -C_M(R_L + R_{ON}) \ln(1 - \frac{V_H}{V_S})$

c) See Figure 10.133.

$\frac{R_{ON}}{R_{ON}+R_L}V_S$

d) $T_{min} = -C_M(R_{ON} + \frac{R_{ON}R_L}{R_{ON}+R_L}) \ln(\frac{V_L - \frac{R_{ON}}{R_{ON}+R_L}V_S}{\frac{R_L}{R_{ON}+R_L}V_S})$

e) $-C_M R_P \ln(\frac{V_T}{V_S})$

ANS:: (a) V_S (b) $T_{min} = -C_M(R_L + R_{ON}) \ln(1 - \frac{V_H}{V_S})$ (c) $\frac{R_{ON}}{R_{ON}+R_L}V_S$ (d) $T_{min} = -C_M(R_{ON} + \frac{R_{ON}R_L}{R_{ON}+R_L}) \ln(\frac{V_L - \frac{R_{ON}}{R_{ON}+R_L}V_S}{\frac{R_L}{R_{ON}+R_L}V_S})$ (e) $-C_M R_P \ln(\frac{V_T}{V_S})$

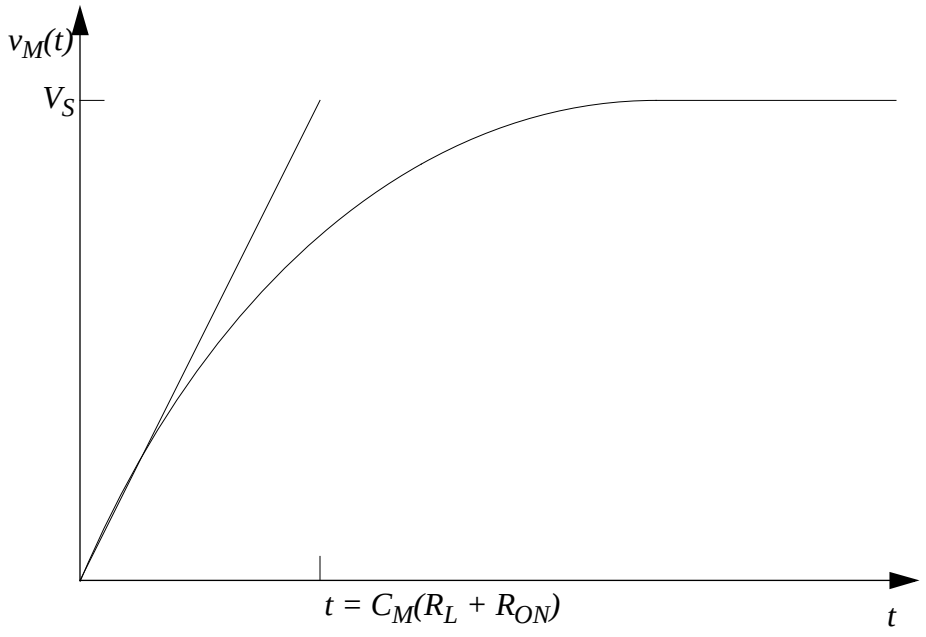


Figure 10.132:

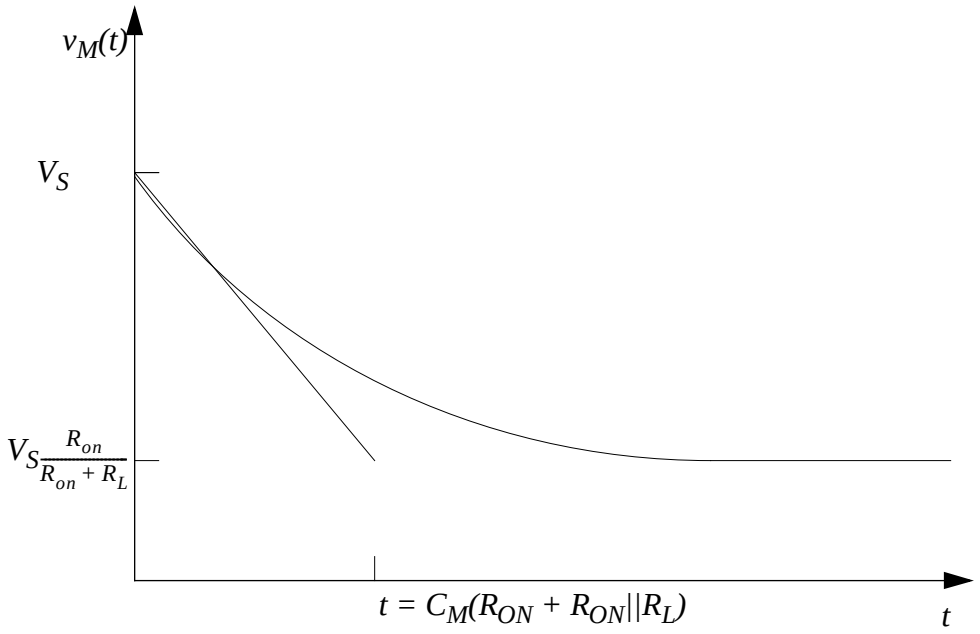


Figure 10.133:

Chapter 11

Energy and Power in Digital Circuits

Exercises

Exercise 11.1 An inverter built using a NMOS transistor and a resistor R_L drives a capacitance C_L. The power supply voltage is V_S and the on resistance of the MOSFET is R_{ON}. The threshold voltage for the MOSFET is V_T. Assume that logical 0's are represented using 0V and logical 1's using V_S volts.

a) Determine the steady-state power consumed by the inverter when a 0 is applied to its input.

b) Determine the steady-state power consumed by the inverter when a 1 is applied to its input.

c) Determine the static power and the dynamic power consumed by the inverter when a sequence of the form $01010101\cdots$ is applied to its input. Assume that signal transitions (0 to 1, or 1 to 0) happen every T seconds. Assume further that T is much greater than the circuit time constant.

d) Assuming the input in part (c), by what factor does the dynamic power decrease if (i) T is increased by a factor of 2, (ii) V_S is decreased by a factor of 2, (iii) C_L is decreased by a factor of 2.

e) Suppose that the inverter must satisfy a static discipline with high and low voltage thresholds $V_{IH} = V_{OH} = V_H$ and $V_{IL} = V_{OL} = V_L$ respectively. You are given a MOSFET with on resistance R_{ON} and threshold V_T. Assume that $V_L < V_T < V_H < V_S$. Choose a value for R_L in terms of the other circuit parameters such that the power consumed by the inverter is minimized.

Solution:

a) The MOSFET is in cutoff and therefore acts as an open circuit - so in the steady state, no current flows through it and therefore no power is consumed.

$P_{steady-state,0} = 0$

b) The power can be calculated using the formula $P = VI$, where V is the supply voltage, and I is the current that flows from supply to ground, which in this case can be calculated using the formula $V = IR$. Therefore, the power is equal to $\frac{V^2}{R}$, where R is the total resistance.

$P_{steady-state,1} = \frac{V_S^2}{R_{ON}+R_L}$

c) The static power remains unchanged since in the steady state a capacitor acts as an open circuit, providing a fundamentally identical system as before. Therefore the static power is one-half the result derived in part B, because the circuit is only on one-half of the time.

To calculate dynamic power, we use the circuit model shown in Figure 11.1.

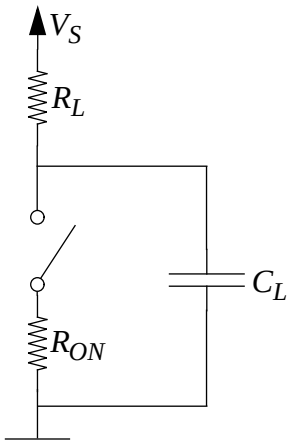


Figure 11.1:

Since power is equal to energy change per unit time, the best way to calculate the average total power (both static and dynamic) is to find the total energy dissipated by each resistor per cycle, and divide by the total cycle length. Energy dissipation is the integral of instantaneous power consumption, so we get the following equation:

$$E_{total} = \int_0^{2T} \frac{(V_S - v_C(t))^2}{R_L} dt + \int_0^{2T} \frac{v_C(t)^2}{R_{on}} dt.$$

The function $v_C(t)$ is shown in Figure 11.2

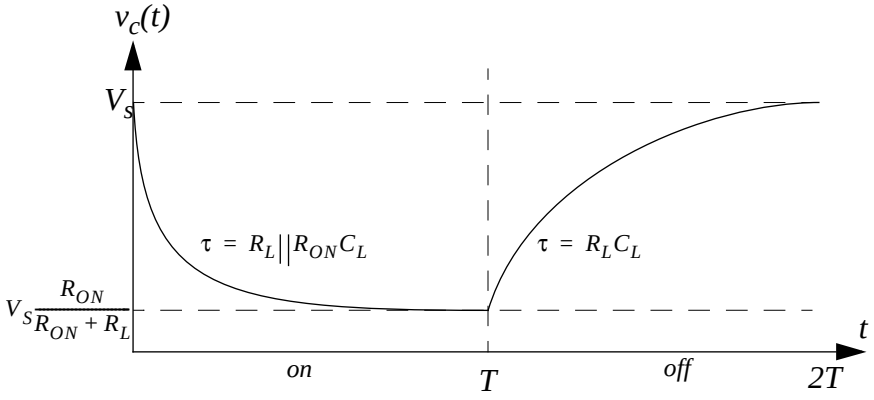


Figure 11.2:

It consists of two exponentials with different time-constants, as shown. The integration is an exercise in elementary calculus, and results in the following:

$$E_{total} = \frac{V_S^2 T}{R_{ON} + R_L} + \frac{V_S^2 R_L^2 C_L}{(R_L + R_{ON})^2}.$$

If we divide through by the total interval $2T$, we get the following.

$$P_{total} = \frac{V_S^2}{2(R_{ON} + R_L} + \frac{V_S R_L^2 C_L}{(R_L + R_{ON})^2 T}.$$

The static power is the first term, so the second term is the dynamic power. This makes sense because if the capacitor were not there, the dynamic power consumption would disappear.

$P_{static} = \frac{V_S^2}{2(R_L+R_{ON})}, P_{dynamic} = \frac{V_S^2 R_L^2 C_L}{(R_L+R_{ON})^2 T}$

d) i) $T \Rightarrow 2T : P_{dyn} \Rightarrow \frac{1}{2}P_{dyn}$

ii) $V_S \Rightarrow \frac{1}{2}V_S : P_{dyn} \Rightarrow \frac{1}{4}P_{dyn}$

iii) $C_L \Rightarrow \frac{1}{2}C_L : P_{dyn} \Rightarrow \frac{1}{2}P_{dyn}$

e) Power actually decreases with increasing R_L, so we can make R_L as large as possible without violating the static discipline. However, the problem arises when we look at the dynamic behavior of the system - as R_L is made very large, the time constant of the capacitor charging and discharging also becomes very large, making the system very slow and therefore useless.

ANS:: (a) $P_{steady-state,0} = 0$, (b) $P_{steady-state,1} = \frac{V_S^2}{R_{ON}+R_L}$, (c) $P_{static} = \frac{V_S^2}{2(R_L+R_{ON})}$, $P_{dynamic} = \frac{V_S^2 R_L^2 C_L}{(R_L+R_{ON})^2 T}$, (d) (i) halved, (ii) quartered, (iii) halved, (e) Maximize R_L while looking out for dynamic constraints.

Exercise 11.2 Determine $\overline{f}$ for the functions given below. Express your answer in a simplified sum of products form. (Hint: use DeMorgan's laws).

a) $f = \overline{A \cdot B}$

b) $f = \overline{A + B}$

c) $f = A + B$

Solution:

a) $\overline{f} = A \cdot B$

b) $\overline{f} = A + B$

c) $\overline{f} = \overline{A + B} = \overline{A} \cdot \overline{B}$

ANS:: (a) $\overline{f} = A \cdot B$ (b) $\overline{f} = A + B$ (c) $\overline{f} = \overline{A} \cdot \overline{B}$

Exercise 11.3 Give a CMOS implementation (using NMOS and PMOS transistors only) of the following logic functions. In doing these exercises, is the value of the on resistance of the MOSFETs needed? Why or why not?

a) $\overline{A \cdot B}$

b) $\overline{A + B}$

c) $A + B$

Solution:

a) See Figure 11.3

b) See Figure 11.4

c)

$$A + B = \overline{\overline{A} \cdot \overline{B}}$$

See Figure 11.5

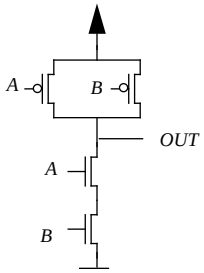


Figure 11.3:

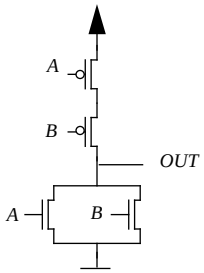


Figure 11.4:

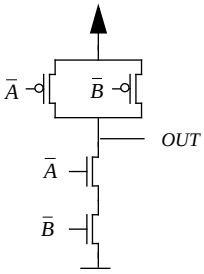


Figure 11.5:

The value of the resistance is not needed, because by design CMOS implementation satisfies the static discipline.

Exercise 11.4 Write a truth table and a boolean expression that describes the operation of each of the digital circuits in Figure 11.6.

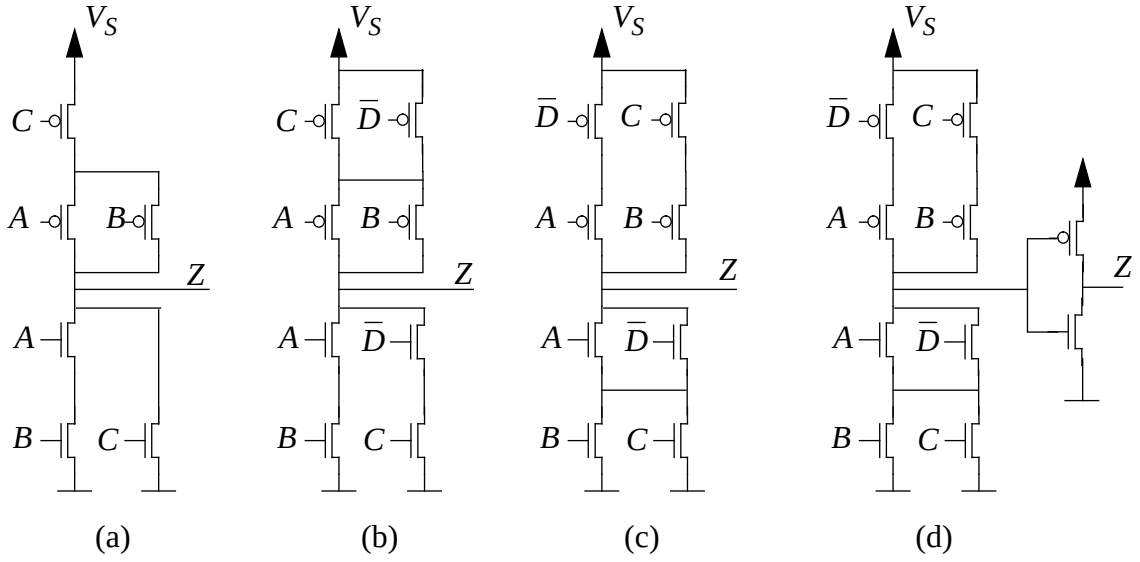


Figure 11.6:

Solution:

a)

$$Z_1 = \overline{AB + C}$$

b)

$$Z_2 = \overline{AB + C\overline{D}}$$

c)

$$Z_3 = \overline{(A + \overline{D}) \cdot (B + C)}$$

d)

$$Z_4 = (A + \overline{D}) \cdot (B + C)$$

a) See Table 11.4

b) See Table 11.1

c) See Table 11.1

A	B	C	Z_1
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Table 11.1:

A	B	C	D	Z_2	Z_3	Z_4
0	0	0	0	1	0	0
0	0	0	1	1	0	0
0	0	1	0	0	1	1
0	0	1	1	1	0	0
0	1	0	0	1	1	1
0	1	0	1	1	0	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	1	1

d) See Table 11.1

Problems

Problem 11.1 This problem examines the power dissipated by a small digital logic circuit. The circuit comprises a series-connected inverter and NOR gate as shown in Figure 11.7. The circuit has two inputs, A and B, and one output, Z. The inputs are assumed to be periodic with period T_4 as shown in the same figure. Assume that $R_{\rm ON}$ for each MOSFET is zero.

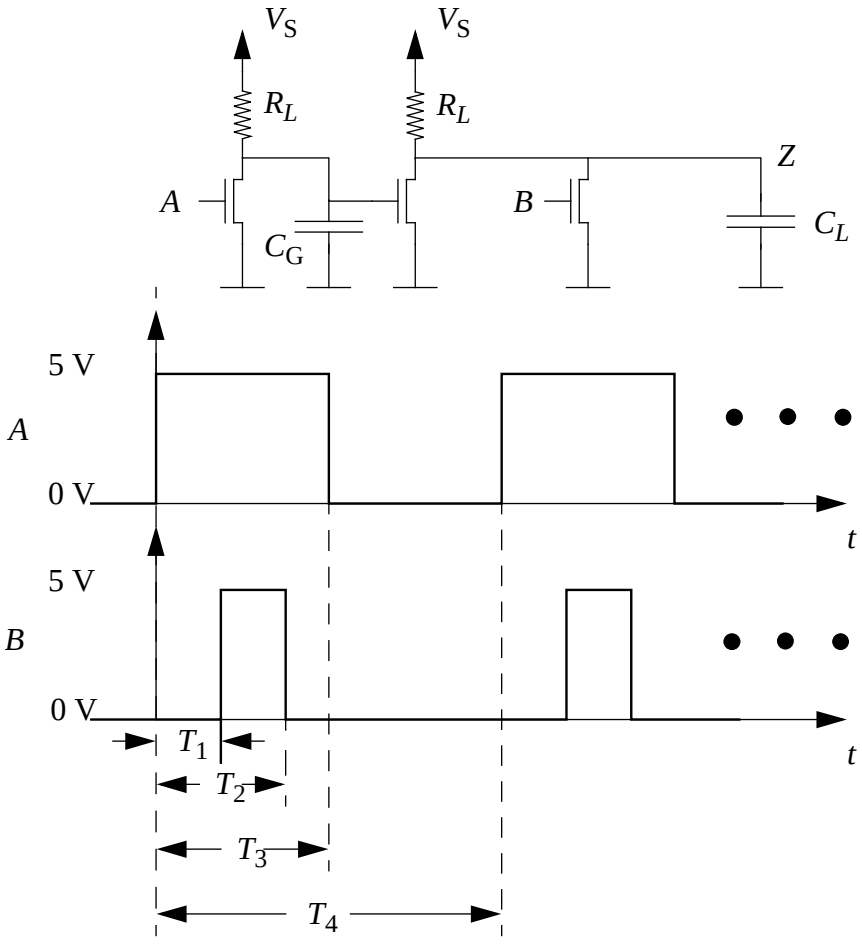


Figure 11.7:

a) Sketch and clearly label the waveform for the output Z for $0 \leq t \leq T_4$. In doing so, assume that $C_{\rm G}$ and $C_{\rm L}$ are both zero.

b) Derive the time-average static power consumed by the circuit in terms of $V_{\rm S}$, $R_{\rm L}$, T_1, T_2, T_3 and T_4. Here, time-average power is defined as the total energy dissipated by the gate during the period $0 \leq t \leq T_4$ divided by T_4.

c) Now assume that $C_{\rm G}$ and $C_{\rm L}$ are nonzero. Derive the time-average dynamic power consumed by the circuit in terms of $V_{\rm S}$, $R_{\rm L}$, $C_{\rm G}$, $C_{\rm L}$, T_1, T_2, T_3 and T_4. In doing so, assume that the circuit time constants are all much smaller than T_1, $T_2 - T_1$, $T_3 - T_2$ and $T_4 - T_3$.

d) Evaluate the time-average static and dynamic powers for $V_{\rm S} = 5$ V, $R_{\rm L} = 10$ kΩ, $C_{\rm G} = 100$ fF, $C_{\rm L} = 1$ pF, $T_1 = 100$ ns, $T_2 = 200$ ns, $T_3 = 300$ ns and $T_4 = 600$ ns.

e) What is the amount of energy consumed by the circuit in 1 minute for the parameters in part (d).

f) By what percentage does the total time-average power consumption drop if the power supply voltage $V_{\rm S}$ drops by 30%?

Solution:

a) The waveform for the output Z for $0 \leq t \leq T_4$ is given below in Figure 11.1.

The truth table: (see Table 11.2)

Table 11.2:

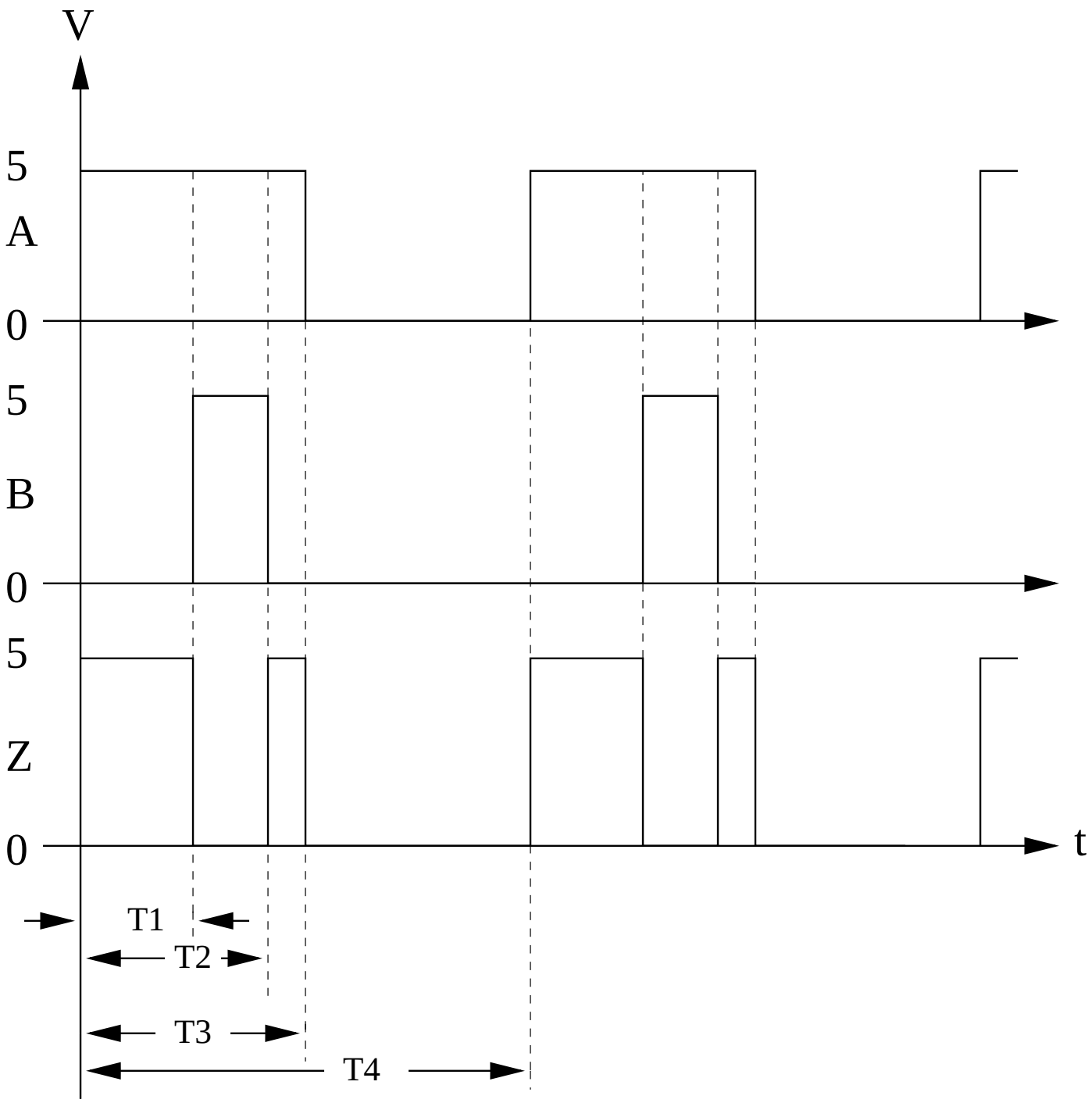
A	B	Z
0	0	0
0	1	0
1	0	1
1	1	1

b) Assuming $R_{ON} = 0$, then: For $0 \leq t \leq T_1$ only the first MOSFET is on, i.e.

$$P_{\rm static} = \frac{V_{\rm S}^2}{R_L}$$

For $T_1 \leq t \leq T_2$ the first and the third MOSFET's are on, i.e.

$$P_{\rm static} = 2\frac{V_{\rm S}^2}{R_L}$$


V
5
A
0
5
B
0
5
Z
0
t
T1
T2
T3
T4

For $T_2 \leq t \leq T_3$ again only the first MOSFET is on, i.e.

$$P_{\text{static}} = \frac{V_S^2}{R_L}$$

For $T_3 \leq t \leq T_4$ only the second MOSFET is on, i.e.

$$P_{\text{static}} = \frac{V_S^2}{R_L}$$

Therefore, the time-average static power consumed by the circuit is given by

$$P_{\text{static,ave}} = \frac{T_1}{T_4}\left(\frac{V_S^2}{R_L + R_{on}}\right) + \frac{T_2 - T_1}{T_4}\left(\frac{2V_S^2}{R_L}\right) + \frac{T_3 - T_2}{T_4}\left(\frac{V_S^2}{R_L}\right)$$
$$+\frac{T_4 - T_3}{T_4}\left(\frac{V_S^2}{R_L}\right)$$
$$= \frac{V_S^2}{R_L}\left(\frac{-T_1 + T_2 + T_4}{T_4}\right)$$

c) For $0 \leq t \leq T_1$ the dynamic dissipation occurs while C_G discharges, and C_L charges, i.e.

$$P_{\text{dynamic}} = \frac{C_G V_S^2 + C_G V_S^2}{2T_1}$$

For $T_1 \leq t \leq T_2$ the dynamic dissipation occurs while C_L discharges, i.e.

$$P_{\text{dynamic}} = \frac{C_L V_S^2}{2(T_2 - T_1)}$$

For $T_2 \leq t \leq T_3$ the dynamic dissipation occurs while C_L charges, i.e.

$$P_{\text{dynamic}} = \frac{C_L V_S^2}{2(T_3 - T_2)}$$

For $T_3 \leq t \leq T_4$ the dynamic dissipation occurs while C_L, C_G charges, and C_L discharges, i.e.

$$P_{\text{dynamic}} = \frac{C_G V_S^2 + C_G V_S^2}{2(T_4 - T_3)}$$

Thus, the time-average dynamic power consumed by the circuit is given by

$$P_{\text{dynamic,ave}} = \frac{T_1}{T_4}\left(\frac{C_G V_S^2 + C_G V_S^2}{2T_1}\right) + \frac{T_2 - T_1}{T_4}\left(\frac{C_L V_S^2}{2(T_2 - T_1)}\right)$$

$$+\frac{T_3 - T_2}{T_4}\left(\frac{C_L V_S^2}{2(T_3 - T_2)}\right) + \frac{T_4 - T_3}{T_4}\left(\frac{C_G V_S^2 + C_G V_S^2}{2(T_4 - T_3)}\right)$$

$$= \frac{V_S^2}{T_4}(C_G + 2C_L)$$

d) Static:

$$P_{\text{static,ave}} = \frac{V_S^2}{R_L + R_{on}}\left(\frac{-T_1 + T_2 + T_4}{T_4}\right)$$
$$= \frac{5^2}{10 \times 10^3 + 0}\left(\frac{-100 + 200 + 600}{600}\right)$$
$$= 2.9\,mW$$

Dynamic:

$$P_{\text{dynamic,ave}} = \frac{1}{T_4}\left(C_G V_S^2 + 2C_L V_S^2\right)$$
$$= \frac{1}{600 \times 10^{-9}}\left(100 \times 10^{-15} \cdot 5^2 + 2 \cdot 1 \times 10^{-12} \cdot 5^2\right)$$
$$= 87.5\,\mu W$$

e)

$$E = Pt$$
$$= (P_{static} + P_{dynamic})(60sec)$$
$$= 0.180J$$

f) Since the power depends linearly on V_S^2, 30% drop in V_S translates to a 51% drop in the total time-average power consumption.

ANS:: (b) $\frac{V_S^2}{R_L}\left(\frac{-T_1+T_2+T_4}{T_4}\right)$ (c) $\frac{V_S^2}{T_4}(C_G + 2C_L)$ (d) $P_{static} = 2.9\,mW$, $P_{dynamic} = 87.5\,\mu W$ (e)$0.18J$ (f)51%

Problem 11.2 Implement the logic function $Z = \overline{A + B + CD}$ using NMOS transistors alone. In other words, use an NMOS transistor in place of the pull-up resistor. Your implementation must satisfy a static discipline with low and high voltage thresholds given by $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$, where $0 < V_L < V_T < V_H < V_S$. V_S is the power supply voltage. As your answer, specify the W/L values for the pullup and the pulldown transistors.

For what combination of inputs does the circuit dissipate the greatest amount of static power? Determine the static power dissipation for this combination of inputs.

Solution:

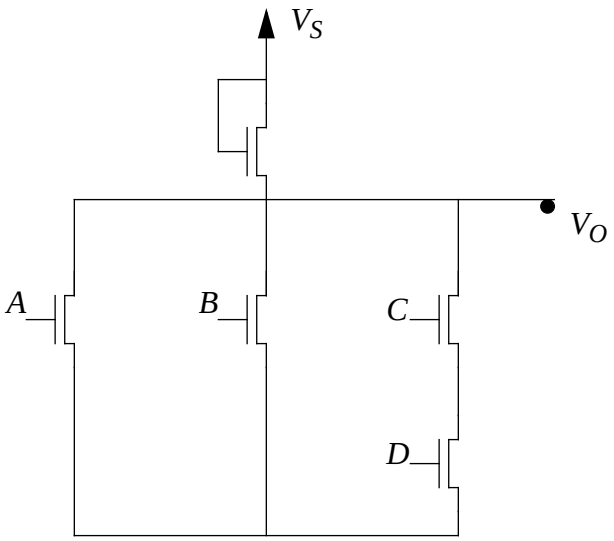


Figure 11.8:

See Figure 11.8 for logic diagram.

Specify the L/W values:

$$V_L > V_S \frac{2(L/W)_{pl}}{(L/W)_{pu} + 2(L/W)_{pd}}$$

$$V_L > V_S \frac{1}{\frac{1}{2}\frac{(L/W)_{pu}}{(L/W)_{pd}} + 1}$$

$$\frac{V_L}{V_S} > \frac{1}{\frac{1}{2}\frac{(L/W)_{pu})}{(L/W)_{pd})} + 1}$$

$$\frac{(L/W)_{pu})}{(L/W)_{pd}) + 1} > 2(\frac{V_S}{V_L} - 1)$$

Greatest power dissipated when total resistance is lowest. This occurs when all MOSFETS are on, i.e., $A = B = C = D = 1$.

Static power dissipation:

$$P_{static} = \frac{V_S^2}{R_{off}} = \frac{V_S^2}{R_{pu} + \frac{2}{5}R_{pd}}$$

ANS:: $P_{static} = \frac{V_S^2}{R_{pu} + \frac{2}{5}R_{pd}}$

Problem 11.3 A circuit consists of N inverters, where $N >> 1$. Each inverter is built using a NMOS transistor and a resistor R_L. The power supply voltage is V_S and the on resistance of the MOSFETs is R_{ON}. The threshold voltage for the MOSFETs is V_T.

a) Suppose we do not know how the inverters are connected to each other or to the inputs and outputs of the circuit. How might you estimate the amount of static power that the circuit is likely to consume?

b) Suppose it is known that the inverters are connected in series as one long chain. Estimate the amount of static power dissipated by the circuit.

Solution:

a) To estimate static power, find all combinations of the circuit layout, and take the average of the power output of the combinations of on-off.

b) On average, $\frac{N}{2}$ inverters will be dissipating power. So:

$$P_{static} = \frac{N}{2} \cdot \frac{V_S^2}{R_L + R_{on}}$$

ANS:: (b) $P_{static} = \frac{N}{2} \cdot \frac{V_S^2}{R_L + R_{on}}$

Problem 11.4 Consider the digital memory element illustrated in Figure 11.9. Assume that the inverters are implemented using a pulldown NMOS transistor with on resistance R_{ON}, and a pullup resistor R_L. The power supply voltage is V_S. What is the instantaneous power dissipated by the memory element when it stores a logical 1? What is the instantaneous power dissipated by the memory element when it stores a logical 0?

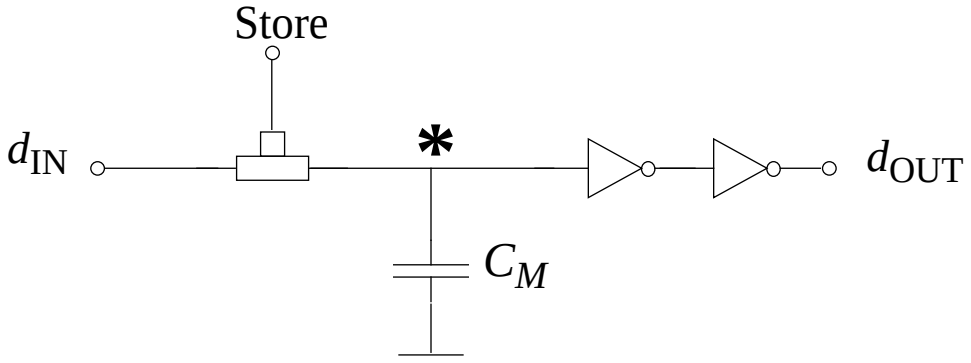


Figure 11.9:

Solution:

Instantaneous power dissipated:

– for logical 1:

$$P = \frac{V_S^2}{R_{on} + R_L}$$

– for logical 0:

$$P = \frac{V_S^2}{R_{on} + R_L}$$

ANS:: $P = \frac{V_S^2}{R_{on}+R_L}$ for both

Problem 11.5 Give a CMOS implementation (using NMOS and PMOS transistors only) of the following logic functions.

1. $(A + B) \cdot (C + D)$
2. $\overline{(A + B) \cdot (C + D)}$
3. $\overline{A} \cdot \overline{B} \cdot C \cdot D$
4. $(\overline{Y \cdot W})(\overline{X \cdot W})(\overline{\overline{X} \cdot Y \cdot \overline{W}})$

Solution:

1. $(A + B) \cdot (C + D)$ See Figure 11.10(a)
2. $\overline{(A + B) \cdot (C + D)}$ See Figure 11.10(b)
3. $\overline{A} \cdot \overline{B} \cdot C \cdot D$ See Figure 11.10(c)
4. $(\overline{Y \cdot W})(\overline{X \cdot W})(\overline{\overline{X} \cdot Y \cdot \overline{W}}) = (\overline{Y}+\overline{W}) \cdot (\overline{X}+\overline{W}) \cdot (X+\overline{Y}+W)$ See Figure 11.10(d)

Problem 11.6

a) Express $\overline{F}$ in a simplified sum-of-products form given that $F = A\overline{B} + C\overline{D}$.

b) Implement the logic function $F = A\overline{B} + C\overline{D}$ with an NMOS digital logic circuit that obeys the static discipline defined by the low-level and high-level logic thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$, respectively. Assume the the supply voltage is V_S, and that the on-state resistance of the NMOS transistors is R_{ON}. Determine the lowest value of the pull-up resistor R_{PU} for which the circuit will obey the static discipline in terms of R_{ON}, V_S, V_L and V_H; not all variables need appear in your answer.

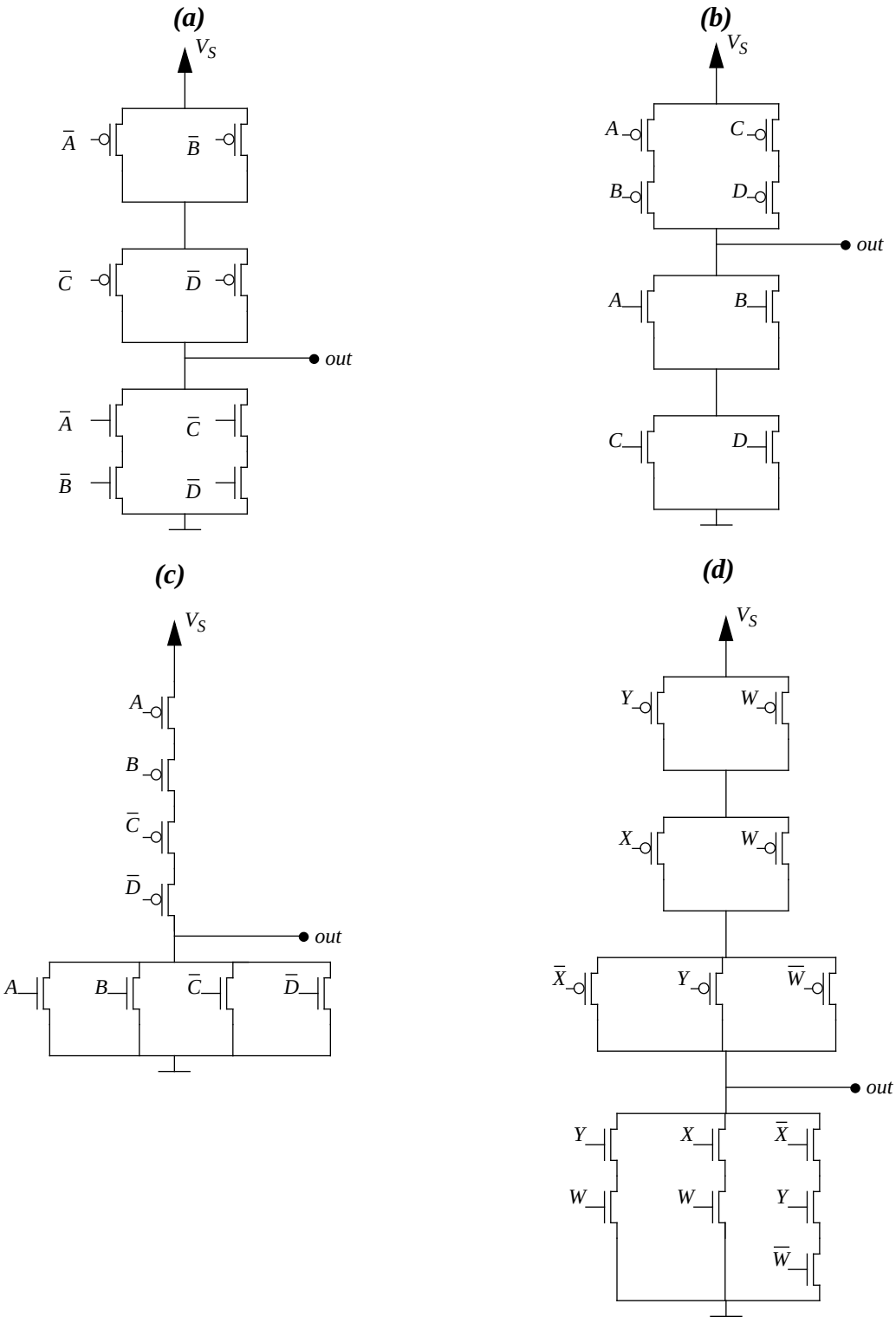

(a)
V_S
$\overline{A}$
$\overline{B}$
$\overline{C}$
$\overline{D}$
out
$\overline{A}$
$\overline{C}$
$\overline{B}$
$\overline{D}$
(b)
V_S
A
C
B
D
out
A
B
C
D
(c)
V_S
A
B
$\overline{C}$
$\overline{D}$
out
A
B
$\overline{C}$
$\overline{D}$
(d)
V_S
Y
W
X
W
$\overline{X}$
Y
$\overline{W}$
out
Y
X
$\overline{X}$
W
W
Y
$\overline{W}$

Figure 11.10:

c) Implement the logic function $F = A\overline{B} + C\overline{D}$ with a CMOS digital logic circuit. Hint: make use of the result from Part (a).

d) Suppose that the NMOS and CMOS circuits above drive a capacitance C_L. Assume that the on-state resistance of both the PMOS and NMOS transistors is R_{ON}. For both the NMOS and CMOS circuits determine the worst-case output rise time. For the purpose of this problem, assume that the worst-case output rise time is the time the output takes to go from 0 V to V_H. Sketch the form of the output for both the NMOS and the CMOS circuit.

e) Suppose that the inputs are arranged such that $B = 1$, $C = 0$ and $D = 1$, and that a 0V-to-5V square wave signal is applied to the input A. Assume the square wave cycle time is T, and that T is large enough so that the output comes close to its steady state value for both falling and rising transitions. Under these conditions, compute the power consumed by the CMOS and NMOS circuits when driving the capacitance C_L load.

Solution:

a)

$$\overline{F} = \overline{A\overline{B} + C\overline{D}} = \overline{A\overline{B}} \cdot \overline{C\overline{D}} = (\overline{A} + B) \cdot (\overline{C} + D)$$

$$\overline{F} = \overline{AC} + \overline{A}D + B\overline{C} + BD$$

b) See Figure 11.11 for logic diagram

$$V_L > V_S \cdot \frac{2R_{on}}{2R_{on} + R_{pu}}$$

$$\frac{V_L}{2V_S R_{on}} > \frac{1}{2R_{on} + R_{pu}}$$

$$\frac{2R_{on}V_S}{V_L} < 2R_{on} + R_{pu}$$

Smallest R_{pu}:

$$R_{on}(\frac{2V_S}{V_L} - 2)$$

c) See Figure 11.12 for logic diagram

d) NMOS output rise time (worst-case):

$$\tau = R_{on}C_L$$

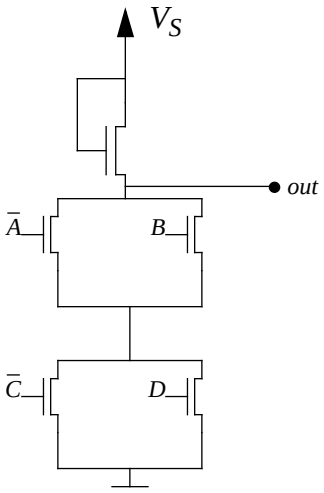


Figure 11.11:

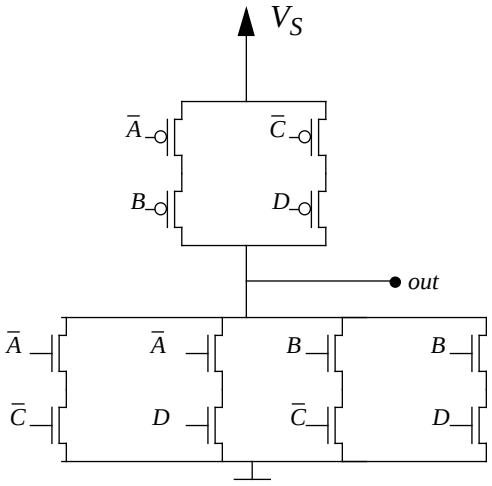


Figure 11.12:

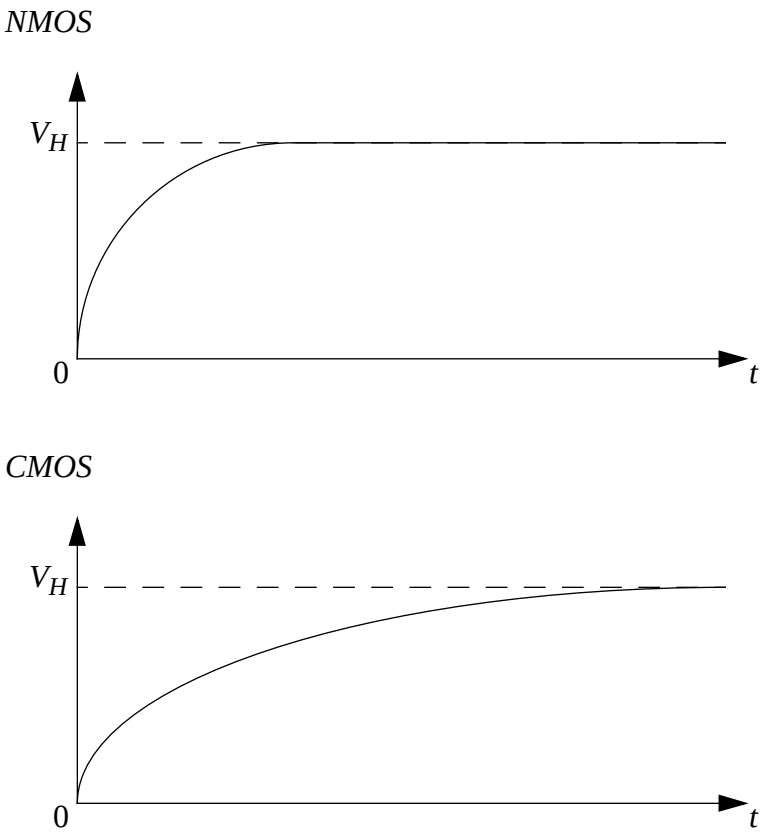


Figure 11.13:

CMOS output rise time (worst-case):

$$\tau = 2R_{on}C_L$$

See Figure 11.13 for sketches

e) NMOS: Power consumed: Alternates between $V_S \cdot \frac{\frac{3}{2}}{1+\frac{3}{2}}$ and $V_S \cdot \frac{1}{1+1}$

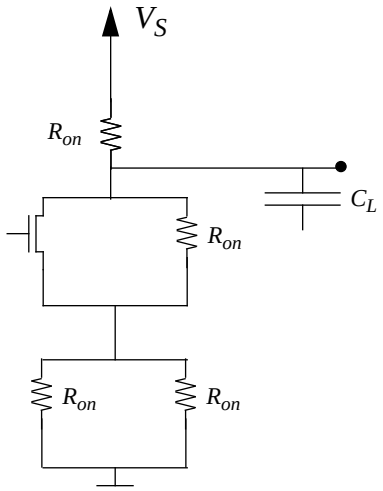


Figure 11.14:

$$P = C_L[(\frac{3}{2}V_S)^2 - (\frac{1}{2}V_S)^2]$$

$$P = C_L V_S^2 \cdot \frac{11}{100}$$

CMOS: no power dissipated

ANS:: (a)$\overline{F} = \overline{AC} + \overline{A}D + B\overline{C} + BD$ (b)$R_{on}(\frac{2V_S}{V_L} - 2)$ (d) $NMOS : \tau = R_{on}C_L$, $CMOS : \tau = 2R_{on}C_L$ (e) $NMOS : P = C_L V_S^2 \cdot \frac{11}{100}$, $CMOS : none$

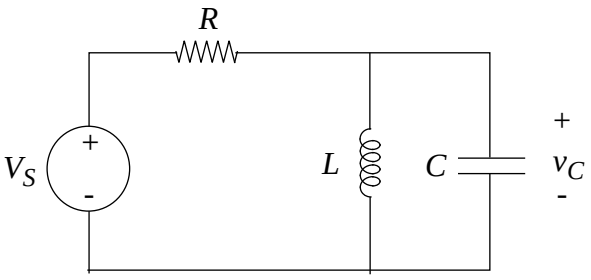
Chapter 12

Transients in Second Order Systems

Exercises

Exercise 12.1

a) Is the zero input response of the circuit shown in Figure 12.1 underdamped, overdamped, or critically damped?



R = 15 Ω L = 1 μH

C = 0.01 μF

Figure 12.1:

b) What is the form of the zero input response (v_C) for the same circuit? Make a rough sketch.

c) Compare the envelope of the zero input response with the rate of delay of the zero input response of the RC circuit in Figure 12.2:

How do they differ?

Solution:

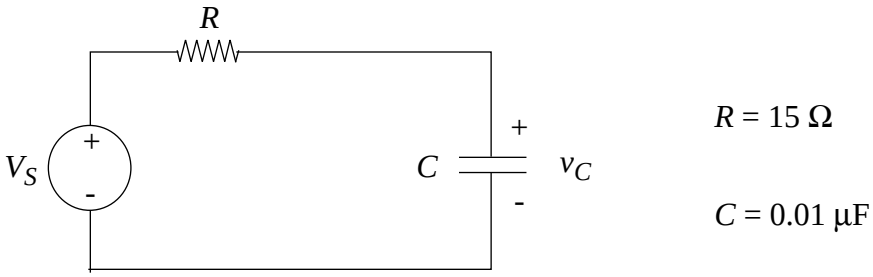


Figure 12.2:

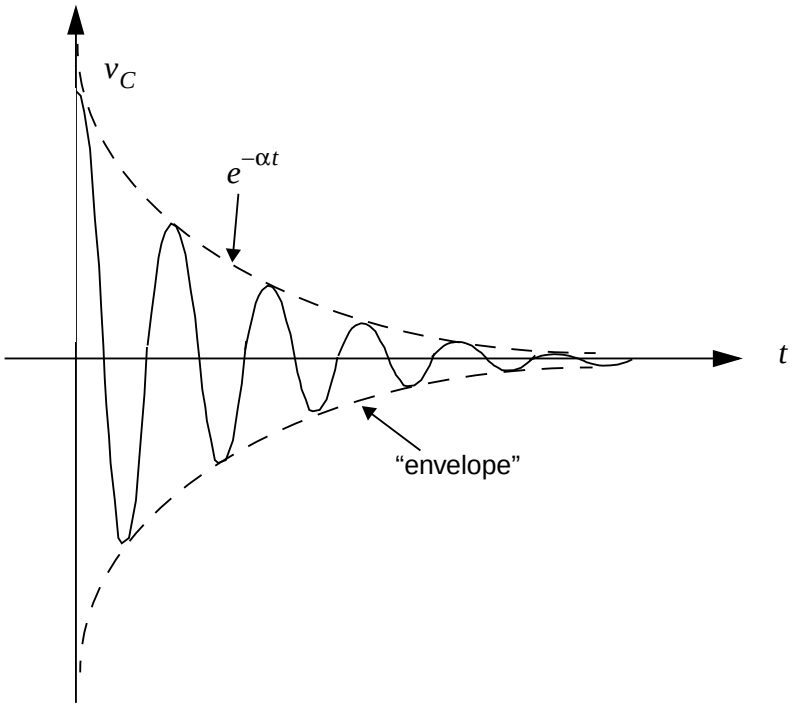


Figure 12.3:

a) $\frac{d^2 v_C}{dt^2} + \frac{1}{RC}\frac{dv_C}{dt} + \frac{1}{LC} = 0$

$2 \cdot \alpha = \frac{1}{RC}$

${\omega_o}^2 = \frac{1}{LC}$

$\alpha < \omega_o \quad \rightarrow$ UNDERDAMPED

b) $v_C = K\ e^{-\alpha t} \cdot \cos(\omega_d \cdot t + \phi)$

$\omega_d = \sqrt{{\omega_o}^2 - \alpha^2}$

$\phi = \tan^{-1}(\frac{\alpha}{\omega_d})$

$\omega_o = 10 \times 10^6$

$\alpha = 3.33 \times 10^6$

c) (1) v_C in RC circuit in zero-input case decays as $e^{-t/\tau} = e^{-t/RC}$.

(2) v_C above in the RLC circuit decays with "envelope" as $e^{-\alpha\tau} = e^{-t/2RC}$.

Therefore, the RC circuit zero-input response decays twice as fast as the RLC response;
i.e. $\tau_{RLC} = 2 \cdot \tau_{RC}$;
RLC takes twice as long to decay.

ANS:: (a) $2\alpha = \frac{1}{RC}$, ${\omega_o}^2 = \frac{1}{LC}$, since $\alpha < \omega_o$, underdamped, (b) $v_C = Ke^{-\alpha t}\cos(\omega_d t + \phi)$, $\omega_d = \sqrt{{\omega_o}^2 - \alpha^2}$, $\phi = \tan^{-1}(\frac{\alpha}{\omega_d})$, $\omega_o = 10 \times 10^6$, $\alpha = 3.33 \times 10^6$, (c) v_C in RC circuit decays as $e^{-t/RC}$, while v_C in RLC circuit decays with "envelope" $e^{-t/2RC}$.

Exercise 12.2 For each of the circuits in Figure 12.4, find and sketch the indicated zero-input response corresponding to the indicated initial conditions.

a) In Figure 12.4, find v_2, assuming $v_1(0) = 1V, v_2(0) = 0$.

b) In Figure 12.5, find v, assuming $i(0) = 0, v(0) = 1V$

c) Repeat (b), but with the resistor changed to 5Ω.

Solution:

a) (1) $\frac{v_1}{8k} + \frac{v_1 - v_2}{6k} + \left(\frac{1}{24}\mu F\right)\frac{dv_1}{dt} = 0$

(2) $v_1 - \left(\frac{1}{18}\mu F\right)\frac{dv_2}{dt}(6000) - v_2 = 0 \quad \rightarrow \quad v_1 = v_2 + \frac{1}{3000}\frac{dv_2}{dt}$

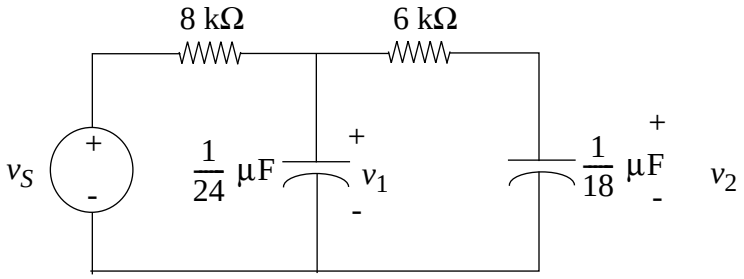


Figure 12.4:

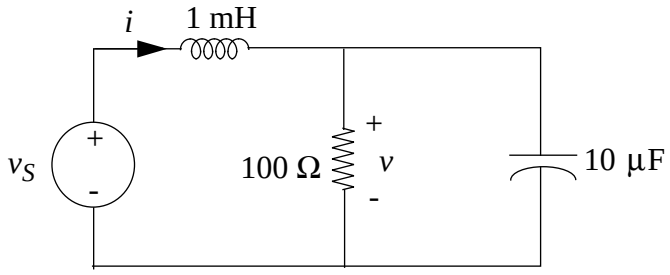


Figure 12.5:

Plug (2) into (1), find

$$v_2 = A\ e^{-1000t} + B\ e^{-9000t}$$

Initial conditions allow us to find constants A and B:

$$A + B = 0 \quad \rightarrow \quad \text{from } v_2(0) = 0$$

$$A + B - \frac{1}{3}A - 3B = 1 \quad \rightarrow \quad \text{from } v_1(0) = 1\text{Volt}$$

$$A = \frac{3}{8}$$

$$B = -\frac{3}{8}$$

$$v_2 = \frac{3}{8}(e^{-1000t} - e^{-9000t})\ ;\ t \text{ in seconds} \quad \text{(a)}$$

b)

$$\frac{v-0}{100} + C\,\frac{dv}{dt} - i = 0$$

$$-v = L\,\frac{di}{dt} \quad \rightarrow \quad \frac{di}{dt} = -\frac{v}{L}$$

$$(s^2 + 1000s + 100 \cdot 10^6)v = 0$$

$$s_{1,2} = \underbrace{-500}_{\alpha} \pm \underbrace{9,990j}_{\omega_d} \quad \rightarrow \quad {\omega_o}^2 = {\omega_d}^2 + \alpha^2 \quad \omega_o = 10,000$$

Thus,

$$v = 1.001\ e^{-500t}\ (0.999\ \cos\omega_d t - 0.05 \sin\omega_d t) \quad \text{(b)}$$

c)

$$(s^2 + 20,000s + 100 \times 10^6)v$$

$$s_{1,2} = -10,000$$

$$v = A\ e^{-10,000t} + Bte^{-10,000t}$$

Initial condition: $v(0) = 1V \quad \rightarrow \quad A = 1$

$$i = -1000 \cdot \int v = -1000 \left[\frac{-A}{10^4}\ e^{-10^4 t} + B \underbrace{\int te^{-10^4 t} dt}_{\text{integrate by parts}} \right]$$

$$i(t=0) = 0 = 10^4 \cdot A + B \quad \rightarrow \quad B = -10^4 \ \text{ since } A = 1$$

$$v = (1 - 10^4)e^{-10^4 t} \quad \text{(c)}$$

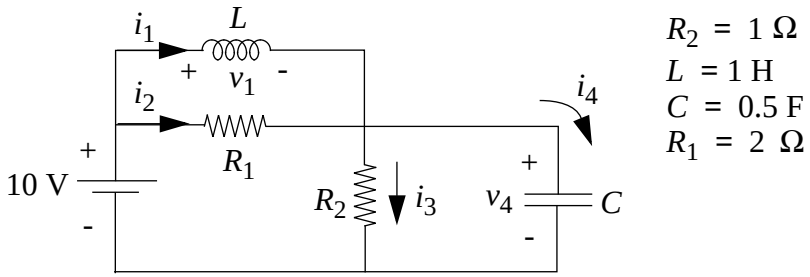


Figure 12.6:

ANS:: (a) $v_2 = \frac{3}{8}(e^{-1000t} - e^{-9000t})$, (b) $v = 1.001e^{-500t}(0.999\cos\omega_d t - 0.05\sin\omega_d t)$, (c) $v = (1 - 10^4)e^{-10^4 t}$

Exercise 12.3 In the circuit in Figure 12.6, a constant voltage source of 10 volts is applied at $t = 0$. Find all branch voltages and all branch currents at $t = 0^+$ and at $t = \infty$ given $i_1(0^-) = 2$ amps and $v_4(0^-) = 4$ volts.

Solution:

At $t = 0^+$,

$i_1 + i_2 = \frac{10}{2} = 5A$

Therefore, $i_3 + i_4 = 5A$

$i_1 = 2Amps$	$v_1 = 6Volts$
$i_2 = 3Amps$	$v_2 = 6Volts$
$i_3 = 4Amps$	$v_3 = 4Volts$
$i_4 = 1Amp$	$v_4 = 4Volts$

At $t = \infty$,

$i_1 = 10Amps$	$v_1 = 0$ (L behaves like a wire)
$i_2 = 0$	$v_2 = 0$ (no current flows through R_1)
$i_3 = 10Amps$	$v_3 = 10Volts$
$i_4 = 0$	$v_4 = 10Volts$

ANS:: $t = 0^+ : i_1 = 2A, v_1 = 6V, i_2 = 3A, v_2 = 6V, i_3 = 4A, v_3 = 4V, i_4 = 1A, v_4 = 4V$. At $t = \infty$: $i_1 = 10A, v_1 = 0, i_2 = 0, v_2 = 0, i_3 = 10A, v_3 = 10V, i_4 = 0, v_4 = 10V$

Exercise 12.4 Is the zero-input response of the circuit in Figure 12.7 underdamped, overdamped, or critically damped? (Provide some kind of justification of your answer, either a calculation or a sentence of explanation.)

$L = 1\mu H \quad C = 0.01\mu F \quad$ and $R_1 = R_2 = 15\Omega$

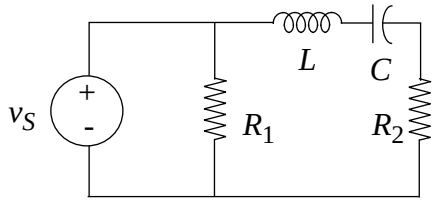


Figure 12.7:

Solution:

For the zero-input case, we may treat the circuit as if R_1 were not there.

$$iR_2 + v_C + v_L = 0$$

$$R_2\frac{di}{dt} + \underbrace{\frac{dv_C}{dt}}_{\frac{i}{C}} + \underbrace{\frac{dv_L}{dt}}_{L\cdot\frac{d^2i}{dt^2}} = 0 \quad \rightarrow \quad (s^2 + \frac{R_2}{L}s + \frac{1}{LC})i = 0$$

$$2\alpha = \frac{R_2}{L} \quad \rightarrow \quad \alpha = 7.5 \times 10^6$$

$$\omega_o = \sqrt{1/LC} = 10 \times 10^6$$

$\alpha < \omega_o$, therefore the response is underdamped.

ANS:: $\alpha = 7.5 \times 10^6, \omega_o = 10 \times 10^6$, so underdamped

Exercise 12.5 In the circuit in Figure 12.8, the inductor current and capacitor voltage have been constrained by some external magic to be $i_L = 5$ Amps, $v_C = -6$ volts. At $t = 0$, the external restraints are removed, and the natural response of the circuit is allowed to evolve. Find the initial slopes of the state variables.

Solution:

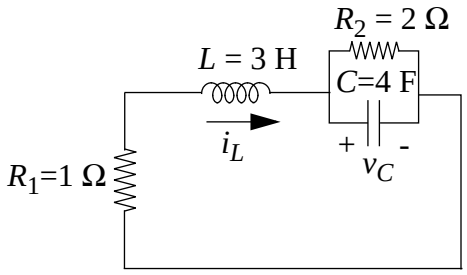


Figure 12.8:

$$C\,\frac{dv_C}{dt} - i_L + \frac{v_C}{R_2} \;\rightarrow\; \frac{dv_C}{dt}\,|_{t=0^+} = \frac{i_L}{C} - \frac{v_C}{CR_2} = \frac{1}{4}(5 - (-\frac{6}{2})) = 2\text{Volts/s}$$

$$-i_L R_1 - L\frac{di_L}{dt} - v_C = 0$$

$$\frac{di_L}{dt} = (-i_L R_1 - v_C)\frac{1}{L} = \frac{1}{3}\text{Amp/s}$$

ANS:: $\frac{dv_C}{dt}\,|_{t=0^+} = 2$Volts/s, $\frac{di_L}{dt} = \frac{1}{3}$Amp/s

Exercise 12.6

a) Write the differential equations for the circuit in Figure 12.9 in state variable form.

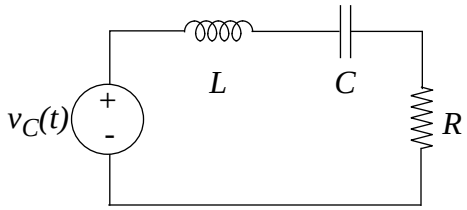


Figure 12.9:

b) Assuming $v_C(0) = 0$, sketch $v_C(t)$ for a very short pulse of height v_i. Don't work it out: just show the form.

Solution:

a) $\frac{dv_C}{dt} = \frac{i_L}{C}$

$\frac{di_L}{dt} = [v_i(t) - i_L R - v_C] \cdot \frac{1}{L}$

b) See Figure 12.10.

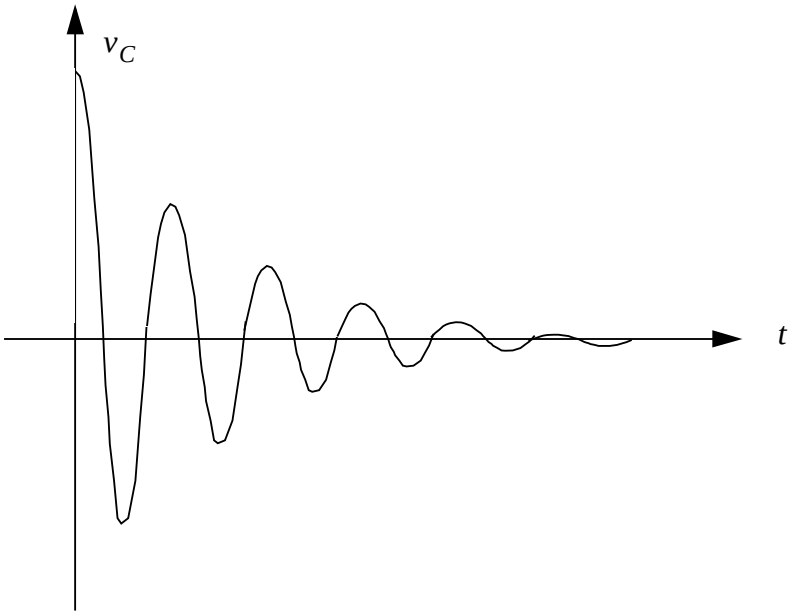


Figure 12.10:

ANS:: $\frac{dv_C}{dt} = \frac{i_L}{C}$, $\frac{di_L}{dt} = [v_i(t) - i_L R - v_C] \cdot \frac{1}{L}$

Exercise 12.7 Solve the following sets of coupled first-order state equations for $t > 0$ with the indicated inputs and initial values. Plot the positions of the natural frequencies in the complex plane. Sketch the state trajectories.

a)

$$\frac{dx_1}{dt} = -3x_1 + x_2$$
$$\frac{dx_2}{dt} = x_1 - 3x_2$$
$$x_1(0) = 2$$
$$x_2(0) = 0$$

b)

$$\frac{dx_1}{dt} = -4x_2$$
$$\frac{dx_2}{dt} = 4x_1$$
$$x_1(0) = 2$$
$$x_2(0) = 0$$

Solution:

a) $x_1 = \overset{o}{x}_2 + 3x_2$

Note $\overset{o}{x}_2 = \frac{dx_2}{dt}$

$$(s^2 + 6s + B)x_2 = 0 \quad \rightarrow \quad x_2 = A\, e^{-4t} + B\, e^{-2t}$$

$$x_1(t=0) = 2 = -4A - 2B + 3A + 3B$$

$$x_2(t=0) = 0 = A + B$$

So, $A = -1, \quad B = 1, \quad$ which implies

$$x_2 = e^{-2t} - e^{-4t}$$

$$x_1 = e^{-2t} + e^{-4t}$$

b)

$$x_2 = -\frac{\overset{o}{x}_1}{4} \quad \rightarrow \quad (s^2 + 16)x_1 = 0 \quad \rightarrow \quad s_{1,2} = \pm 4j$$

$$x_1 = Ae^{4jt} + Be^{-4jt}$$

$$x_2(0) = 0 = -\frac{1}{4}(4jA - 4jB) \quad \rightarrow \quad A = B$$

$$x_1(0) = 2 = A + B \quad \rightarrow \quad A = B = 1$$

$$x_1 = e^{4jt} + Be^{-4jt} \quad \rightarrow \quad x_1 = 2\cos 4t \;\; \text{since} \;\; \cos 4t = \frac{(e^{4jt} + e^{-4jt})}{2}$$

$$x_2 = -\frac{1}{4}(-(4)2\sin 4t) \quad \rightarrow \quad x_2 = 2\sin 4t$$

ANS:: (a) $x_1 = e^{-2t} + e^{-4t}$, $x_2 = e^{-2t} - e^{-4t}$, (b) $x_1 = 2\cos 4t$, $x_2 = 2\sin 4t$

Exercise 12.8 Find the roots of the characteristic polynomial (often called the network natural frequencies) in each of the networks in Figure 12.11:

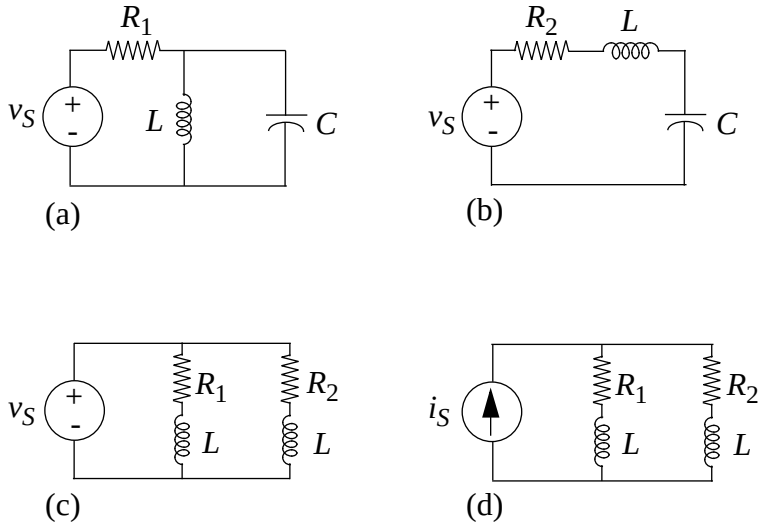


Figure 12.11:

Numerical values: $R_1 = 10\Omega, L = 10\mu H, C = 10\mu F, R_2 = 2\Omega$

Solution:

a)

$$\frac{v_S - v_L}{R_1} - i_L - i_C = 0$$

Setting $v_S = 0$, and noting that $v_L = v_C, \;\; L\frac{di_L}{dt} = v_L, \;\; i_C = C\frac{dv_C}{dt}$, we find

$$\left(s^2 + \frac{s}{R_1 C} + \frac{1}{LC}\right) v_C = 0$$

$$s_{1,2} = -5000 \pm 99,874j$$

b)

$$v_S - iR_2 - v_L - v_C = 0$$

$$(s^2 + \frac{R_2}{L}s + \frac{1}{LC})i = 0 \quad \rightarrow \quad s_{1,2} = -100,000 \text{ (double root)}$$

c)

$$i_1 R_1 + L\frac{di_1}{dt} = 0 \quad \rightarrow \quad R_1 + Ls_1 = 0 \quad \rightarrow \quad s_1 = -\frac{R_1}{L}$$

$$i_2 R_2 + L\frac{di_2}{dt} = 0 \quad \rightarrow \quad s_2 = -\frac{R_2}{L}$$

$$s_{1,2} = -1,000,000; \; -200,000$$

d)

$$i_1 = -i_2 \quad \rightarrow \quad L\frac{di_1}{dt} + i_1 R_1 - i_2 R_2 - L\frac{di_2}{dt} = 0 \text{ (first-order circuit)}$$

$$s = -\frac{R_1 + R_2}{2L}$$

$$s = -600,000$$

ANS:: (a) $-\alpha \pm j\omega_d; a = 5 \times 10^3$rad/sec, $\omega_d = 10^5$rad/sec, (b) $-\alpha$(double root); $\alpha = 10^5$rad/sec, (c) $-\alpha_1, -\alpha_2; \alpha_1 = 10^6$rad/sec, $\alpha_2 = 2 \times 10^5$rad/sec, (d) one natural frequency at $-\alpha; \alpha = 6 \times 10^5$rad/sec

Problems

Problem 12.1 Electrical networks are used to model physical systems governed by linear differential equations. The most important problems which arise in such modeling concern the interplay of accuracy and simplicity. It is usually very important to know when certain effects can safely be ignored in order to simplify the model and subsequent

analysis. Such knowledge can be obtained by understanding the consequences of making the simplifying assumptions.

Two networks which could be used to model an acoustic system are shown in Figure 12.12. It is known that the inductance L is small (specifically $L << (R^2C)/4)$ but it is not known whether a circuit model with no inductances will be adequate. You are to help answer this problem by determining the difference in the responses of the capacitor voltage v_C for the two circuits. Specifically assume:

$$\begin{aligned} i_S(t) &= I u_{-1}(t) \qquad \text{(a step of amplitude I)} \\ v_C(0^-) &= 0 \\ i_L(0^-) &= 0 \end{aligned}$$

Determine $v_C(t)$ for $t > 0$ for both circuits. You should identify the effects of the inductance on such characteristics of the response as the natural frequencies, approximate behavior for small t, and asymptotic behavior.

You can greatly simplify the form of your results by making use of some assumptions derived from Taylor's theorem. For $x << 1$,

$$\sqrt{1-x} \simeq 1 - 1/2x \tag{12.1}$$

and

$$e^{-x} \simeq 1 - x \tag{12.2}$$

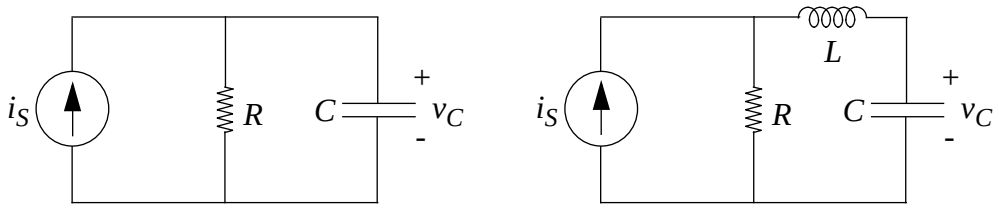


Figure 12.12:

Solution:

A time-domain solution using differential equations is presented first:

We can write the following KCL equation:

$$I_s = \frac{v_L + v_C}{R} + C v_C'.$$

We also know that:

$$v_L = Li_C' = LCv_C''.$$

Substituting, we get:

$$\frac{R}{LC}I_s = v_c'' + \frac{R}{L}v_c' + \frac{1}{LC}v_C.$$

The roots of the characteristic equation are:

$$s = \frac{-R}{2L} \pm \frac{R}{2L}\sqrt{1 - \frac{4L}{R^2C}}.$$

Since we know that $\frac{4L}{R^2C} << 1$, we can simplify to get the following roots:

$$s = \frac{-R}{L}, \frac{-1}{LC}.$$

We now have the following solution to the differential equation:

$$v_C = Ae^{\frac{-t}{RC}} + Be^{\frac{-R}{L}t} + IR.$$

By inspection, since the inductor acts as an open circuit at $t = 0$, we know that $v_C(0) = 0$ and $i_C(0) = v_C'(0) = 0$, so we substitute in those values, getting the following conditions:

$$A + B + IR = 0,$$

$$\frac{-A}{RC} - \frac{-RB}{L} = 0.$$

Solving for A and B, we get:

$$v_C = IR + \frac{-ICR^3}{R^2C - L}e^{\frac{-t}{RC}} + \frac{LIR}{R^2C - L}e^{\frac{R}{L}t}.$$

If we set the inductor to zero, we get the following:

$$v_C = IR - IRe^{\frac{-t}{RC}}.$$

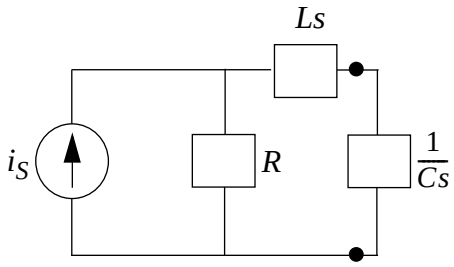


Figure 12.13:

An alternate, more elegant solution involves working in the frequency domain.

First, draw the impedance model as shown in Figure 12.13. From here, determine the Thevenin equivalent of the left side.

The Thevenin impedance Z_{TH} is equal to $R+Ls$, while the Thevenin voltage is equal to $i_S R$. A voltage-divider relationship ensues:

$$v_C = v_{TH}\frac{\frac{1}{Cs}}{Z_{TH}+\frac{1}{Cs}}.$$

This can be simplified to form an admittance transfer function:

$$\frac{v_C}{i_S} = \frac{\frac{R}{LC}}{s^2+\frac{R}{L}s+\frac{1}{LC}}.$$

We must find the roots of the denominator:

$$s = \frac{-RC \pm \sqrt{R^2C^2-4LC}}{2LC} = \frac{-R}{2L} \pm \frac{R}{2L}\sqrt{1-\frac{4L}{R^2C}}.$$

If we use the Taylor series approximation, we can simplify to get the following two roots:

$$s_1 = \frac{-R}{L}, s_2 = \frac{-1}{RC}.$$

Our new approximate admittance function is therefore:

$$\frac{v_C}{i_S} = \frac{\frac{R}{LC}}{s^2+[\frac{R}{L}+\frac{1}{RC}]s+\frac{1}{LC}}.$$

We substitute in that $i_S(t) = Iu(t)$, which corresponds to $i_S(s) = \frac{I}{s}$ when the Laplace transform is taken. Our output function is therefore:

$$v_C(s) = \frac{\frac{IR}{LC}}{s(s+\frac{R}{L})(s+\frac{1}{RC})}.$$

This can be simplified using partial fractions to get the following:

$$v_C(s) = I\left(\frac{R}{s} + \frac{\frac{-LR}{L-R^2C}}{s+\frac{R}{L}} + \frac{\frac{R^3C}{L-R^2C}}{s+\frac{1}{RC}}\right).$$

We convert this back into a time-domain expression by taking the inverse Laplace transform:

$$v_C(t) = IR - \frac{ILR}{L-R^2C}e^{\frac{-Rt}{L}} + \frac{IR^3C}{L-R^2C}e^{\frac{-t}{RC}}.$$

Substituting in that I = 1, we get the following:

$$v_C(t) = IR - \frac{LIR}{L-R^2C}e^{\frac{-Rt}{L}} + \frac{IR^3C}{L-R^2C}e^{\frac{-t}{RC}}.$$

From here, we can make the following approximation if we leave out the inductor:

$$v_C(t) = IR(1-e^{\frac{-t}{RC}}).$$

Not coincidentally, these are the same results that we got using differential equations in the time domain.

See Figures 12.14 and 12.15 for the transfer functions. Note that without the inductor, the initial slope is nonzero, while with the inductor, the slope is zero. The natural frequencies are changed by the presence of the inductor since without the inductor there is but one natural frequency, and with the inductor there are two. For a very small inductor, the second natural frequency is very low and therefore almost negligible in comparison to the natural frequency caused by the capacitor. The asymptotic behavior is identical for both since the inductor has no long-term steady state effect. No matter the size of the inductor, the voltage across the capacitor approaches IR asymptotically.

ANS:: with small inductor: $v_C(t) = IR - \frac{LIR}{L-R^2C}e^{\frac{-Rt}{L}} + \frac{IR^3C}{L-R^2C}e^{\frac{-t}{RC}}$, without inductor: $v_C(t) = IR(1-e^{\frac{-t}{RC}})$.

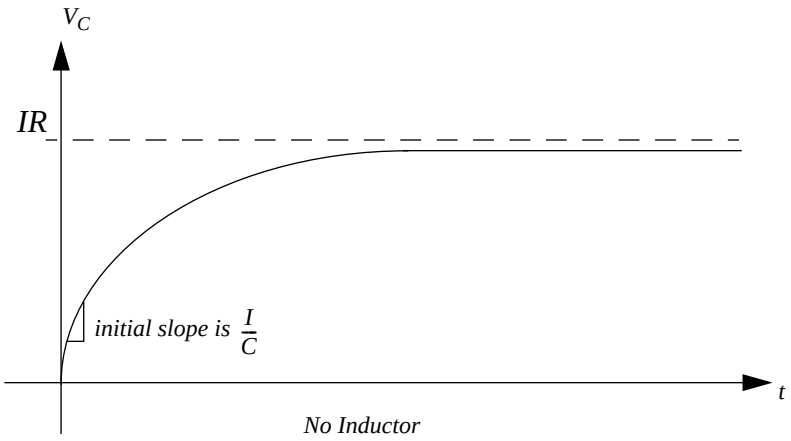


Figure 12.14:

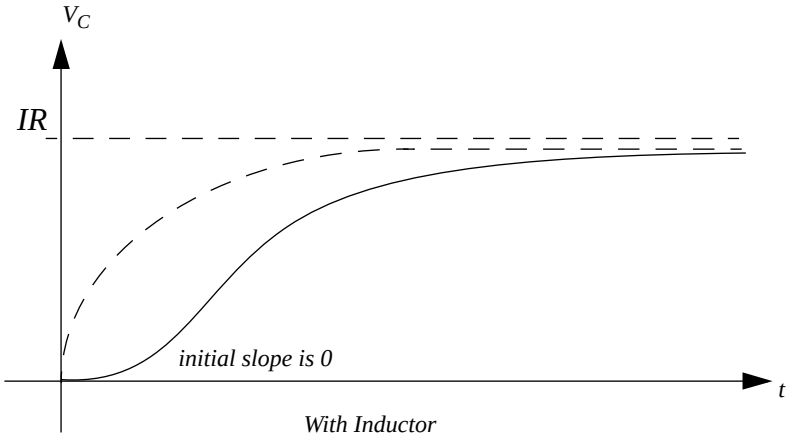


Figure 12.15:

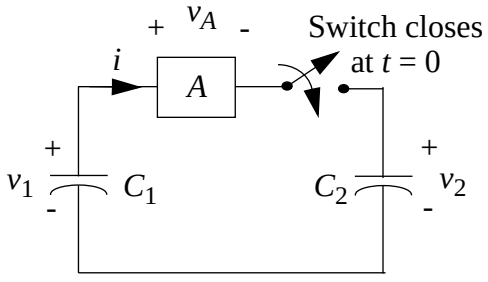


Figure 12.16:

Problem 12.2 Capacitor C_1 has an initial voltage $v_1(0) = V$. Capacitor C_2 is initially uncharged, $v_2(0) = 0$. The voltage across element A tends to zero as time tends to infinity. At time $t = 0$, the switch is closed.

See Figure 12.16.

a) Compute the initial charge of the system.

b) Find the voltage across both capacitors a long time after the switch has been closed. Remember that the total charge of the system must be conserved.

c) Find the energy stored in the system after a long time.

d) Find the ratio of final stored energy to initial energy. Where did the rest of the energy go?

e) Assume element A is a resistor R. Find its voltage or current, and from that, find out the energy lost in it.

f) Find the ratio of lost energy to initial energy. Is it what you expected? Does it depend on R?

g) What would happen if an inductor was placed in series with R? Sketch the behavior of the current. (No calculations are needed.)

Solution:

a) Again, only C_1 has any voltage. Thus, the total charge of the system is $Q_i = C_1 V$.

b) We are told that the voltage across A tends to zero. Therefore, $v_1 = v_2$ after a long time. Let's call this voltage v_f. The final charge of the system is

$$Q_f = C_1 v_f + C_2 v_f = (C_1 + C_2) v_f$$

Charge must be conserved since there is no place for charge to go. Thus, $Q_f = Q_i = C_1 V$. Substituting $C_1 V$ for Q_f, we have

$$C_1 V = (C_1 + C_2) v_f \Rightarrow v_f = \frac{C_1}{C_1 + C_2} V$$

c) Since both capacitors have the same voltage, the energy as $t \to \infty$ is

$$E_f = \frac{1}{2} C_1 v_f^2 + \frac{1}{2} C_2 v_f^2 = \frac{1}{2} (C_1 + C_2) v_f^2$$

Substituting the expression we found for v_f, we get

$$E_f = \frac{1}{2} (C_1 + C_2) \frac{C_1^2}{(C_1 + C_2)^2} V^2 = \frac{1}{2} \frac{C_1^2}{C_1 + C_2} V^2$$

d)

$$\frac{E_f}{E_i} = \frac{\frac{1}{2}\frac{C_1^2}{C_1+C_2}V^2}{\frac{1}{2}C_1V^2} = \frac{C_1}{C_1+C_2}$$

The rest of the energy, namely $\frac{C_2}{C_1+C_2}$, must be dissipated in element A.

e) If A is a resistor R, then the system is first order with $\tau = R\frac{C_1C_2}{C_1+C_2}$, since C_1 and C_2 are in series as seen from the resistor. We also know that the initial and final voltage across R is the difference in voltage of the two capacitors:

$$v_R(0) = V, \quad v_R(t \to \infty) = 0$$

From this information, we can obtain the voltage across R:

$$v_R(t) = Ve^{-t/\tau}, \quad \tau = R\frac{C_1C_2}{C_1+C_2}$$

The power lost across R is

$$P_R = \frac{v_R^2}{R} = \frac{V^2}{R}e^{-t/\tau}, \quad \tau = R\frac{C_1C_2}{C_1+C_2}$$

The energy lost in R is

$$E_R = \int_0^\infty \frac{V^2}{R}e^{-t/\tau}dt, \quad \tau = R\frac{C_1C_2}{C_1+C_2}$$

This integral yields

$$E_R = \frac{V^2}{2}\frac{C_1C_2}{C_1+C_2}$$

f)

$$\frac{E_R}{E_i} = \frac{\frac{V^2}{2}\frac{C_1C_2}{C_1+C_2}}{\frac{1}{2}C_1V^2} = \frac{C_2}{C_1+C_2}$$

The ratio can be checked by noting that $E_R/E_i + E_f/E_i = 1$, thus accounting for all the energy in the system. surprisingly, the energy lost in the resistor is independent from the value of its resistance.

g) If an inductor was placed in series with R, the charge would oscillate between the two capacitors until it reached equilibrium. At that point the current through the inductor and the resistor would be zero. The energy lost in the resistor would be the same as before, since our assumption about element A (in this case, a series combination of an inductor and a resistor) still holds.

ANS:: (a) $Q_i = C_1 V$, (b) $C_1 V = (C_1 + C_2) v_f \Rightarrow v_f = \frac{C_1}{C_1+C_2} V$, (c) $E_f = \frac{1}{2}(C_1 + C_2)\frac{C_1^2}{(C_1+C_2)^2} V^2 = \frac{1}{2}\frac{C_1^2}{C_1+C_2} V^2$, (d) $fracE_f E_i = \frac{C_1}{C_1+C_2}$, (e) $E_R = \frac{V^2}{2}\frac{C_1 C_2}{C_1+C_2}$, (f) $fracE_R E_i = \frac{C_2}{C_1+C_2}$

Problem 12.3 Shown in Figure 12.17 is one possible circuit model for a transformer, for use where there can be a common ground between primary and secondary. Assume: $L_1 = 2.5H$, $L_2 = 0.025H$, $M = k\sqrt{L_1 L_2}$, where $k < 1$, $R_1 = 1k\Omega$, $R_2 = 10\Omega$.

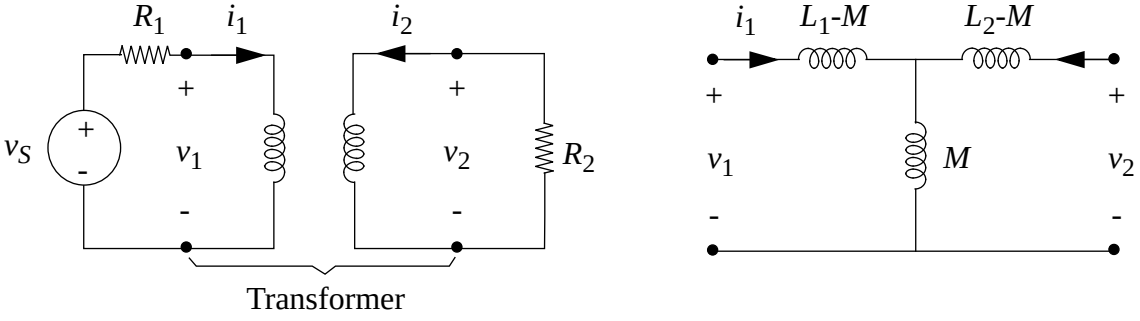


Figure 12.17:

a) Write the state equations for this network using i_1 and i_2 as state variables, and using the given circuit model to represent the transformer.

b) Determine the behavior of the natural frequencies of the network as a function of the coupling constant k. In particular, what are the natural frequencies in the limit of small k, and in the so-called tight-coupling limit, where k approaches unity?

c) Assume that v_S is a 1-volt square pulse of length 5 msec. Find $v_2(t)$ for the case $k = .98$. Is the output a good replica of a square pulse, or are there obvious departures from the square pulse shape?

Solution:

a) We write the following KVL equations:

$$v_S = R_1 i_1 + (L_1 - M) i_1' + M(i_1' + i_2') = R_1 i_1 + L_1 i_1' + M i_2',$$

$$0 = R_2 i_2 + (L_2 - M) i_2' + M(i_1' + i_2') = R_2 i_2 + L_2 i_2' + M i_1'.$$

These can be simplified to get the following state equations:

$$i_1' = \frac{L_2}{M^2 - L_1 L_2} R_1 i_1 - \left(\frac{R_2}{M} + \frac{R_2 L_1 L_2}{M(M^2 - L_1 L_2)} \right) i_2 - \frac{L_2}{M^2 - L_1 L_2} v_S,$$

$$i_2' = \frac{-M}{M^2 - L_1 L_2} R_1 i_1 + \frac{R_2 L_1}{M^2 - L_1 L_2} i_2 + \frac{M}{M^2 - L_1 L_2} v_S.$$

b) Since we are looking for the internal characteristics of the system, we do not need to give it a driving condition, so we set $v_S = 0$.

The two state equations can be simplified to give the following result:

$$i_1' = \frac{L_2 R_1}{M^2 - L_1 L_2} i_1 - \frac{R_2 M}{M^2 - L_1 L_2} i_2,$$

$$i_2' = \frac{L_1 R_2}{M^2 - L_1 L_2} i_2 - \frac{R_1 M}{M^2 - L_1 L_2} i_1.$$

From here, we can eliminate i_2 and i_2' using standard differential equation techniques and get the following equation:

$$i_1'' + \frac{-L_2 R_1 - L_1 R_2}{M^2 - L_1 L_2} i_1' + \frac{-R_1 R_2}{M^2 - L_1 L_2} i_1 = 0.$$

This corresponds to a transfer function whose denominator is:

$$s^2 + \frac{L_1 R_2 + L_2 R_1}{L_1 L_2 - M^2} s + \frac{R_1 R_2}{L_1 L_2 - M^2}.$$

This can be written in terms of K:

$$(1 - K^2)(L_1 L_2) s^2 + (L_1 R_2 + L_2 R_1) s + (R_1 R_2).$$

The transfer function can also be easily found in the frequency domain, using Laplace transforms. This solution is demonstrated below.

First, we must draw the impedance model for this circuit, which is shown in Figure 12.18. Z_1, Z_2, and Z_3 are the impedances of the three inductors, and i_1, i_2, and i_3 are the currents that go through them, as shown in the diagram.

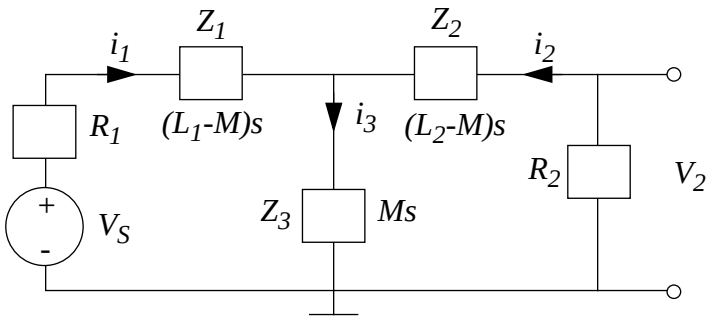


Figure 12.18:

First of all, v_2 is most easily calculated as a Thevenin equivalent voltage by a series of Norton-to-Thevenin-to-Norton simplifications, as shown in Figure 12.19. The last diagram in the figure is a voltage divider, and after simplification, the following result ensues:

$$v_2 = \frac{v_S R_2 Z_3}{R_1 R_2 + R_1 Z_2 + R_1 Z_3 + R_2 Z_1 + R_2 Z_3 + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}.$$

From here, it is very easy to find i_2, since it is the current going through resistor R_2, so it has current $-\frac{v_2}{R_2}$. i_3 can be found by finding the voltage across Z_3, which is the sum of the voltages across R_2 and Z_2.

$$i_3 = -i_2 \frac{Z_2 + R_2}{Z_3}.$$

In order to find the natural frequencies, we find the roots of the denominator of the system function, which is:

$$(1 - K^2)(L_1 L_2)s^2 + (R_1 L_2 + R_2 L_1)s + R_1 R_2.$$

This was derived in the time-domain previously.

If k is close to zero, then the denominator can be factored, and the two roots are:

$$s = -\frac{R_1}{L_1}, -\frac{R_2}{L_2}.$$

As k gets close to 1, one of the natural frequencies increases without bound, and the other gets closer and closer to the following value:

$$s = \frac{-R_1 R_2}{R_1 L_2 + R_2 L_1}.$$

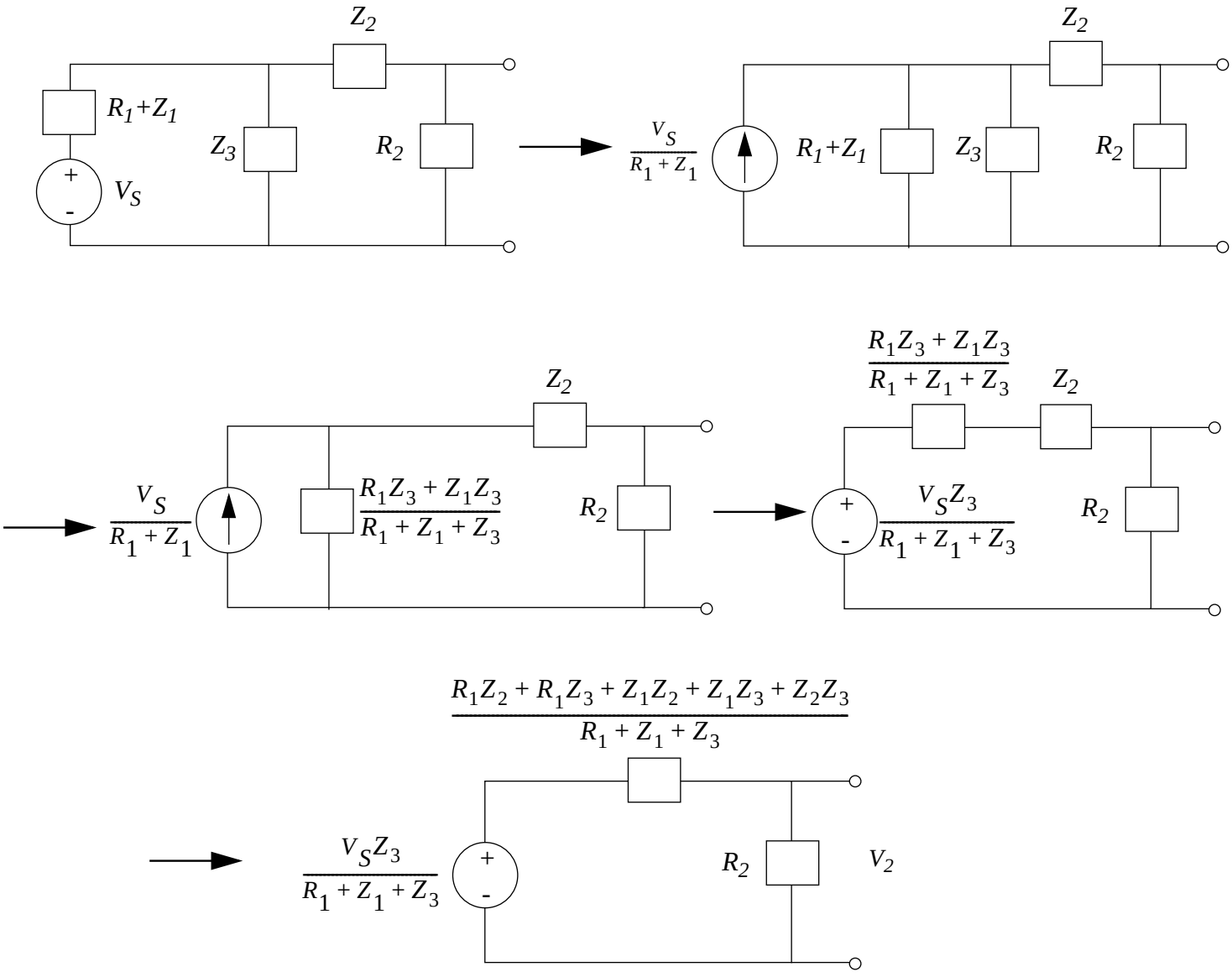

Z_2
R_1+Z_1
Z_3
R_2
V_S
$\frac{V_S}{R_1+Z_1}$
$\frac{R_1Z_3+Z_1Z_3}{R_1+Z_1+Z_3}$
$\frac{V_SZ_3}{R_1+Z_1+Z_3}$
$\frac{R_1Z_2+R_1Z_3+Z_1Z_2+Z_1Z_3+Z_2Z_3}{R_1+Z_1+Z_3}$
V_2

Figure 12.19:

c) We can find the transfer function in the time domain by realizing that the response to a square pulse is the response to a unit step, added to a response to another step that is shifted in time.

We can find the two natural frequencies by substituting in to the characteristic equation previously derived. The two roots are $s = -202.02$ and $s = -20000$ so the response to a unit step will be of the following form:

$$v_2(t) = Ae^{-202.02t} + Be^{-20000t}.$$

This for time $t > 0$, of course. The initial value is zero, since the output voltage is dependent on the current through a resistor, which is the same as the current through an inductor, and the current through an inductor cannot change instantaneously.

We must find the final values of each of the exponentials. Since the output dies away as t becomes very large, A and B must be equal in magnitude and opposite in sign.

Therefore, we have:

$$v_2(t) = V(e^{-202.02t} - e^{-20000t}).$$

The derivative of our output is:

$$v_2'(t) = 19797.98V_f(e^{-202.02t} - e^{-20000t}).$$

The derivative at time $t = 0$ is equal to $19797.98V_f$, and if we can find the initial derivative another way without finding V_f, then we can use that result to find V_f.

That method is as follows:

Very shortly after time $t = 0$, the inductors are so close to open circuits, that their resistance is very high, and the two ordinary resistors may be neglected. The inductors obey the rule $V = L\frac{dI}{dt}$, so the derivative of the current through any inductor may be found using simple current-divider laws. In other words, we treat the voltage-source as a voltage-source, and the inductors as *resistors*, and then remember that the "current" found through "resistor" L_2 is really the derivative of a current.

This is an exercise in simple circuit analysis, and the easiest way to it is a Thevenin-Norton conversion, and then one current divider. This is shown in Figure 12.20.

The result is:

$$\frac{di_{L2}}{dt} = \frac{v_S M}{L_1 L_2 - M^2}.$$

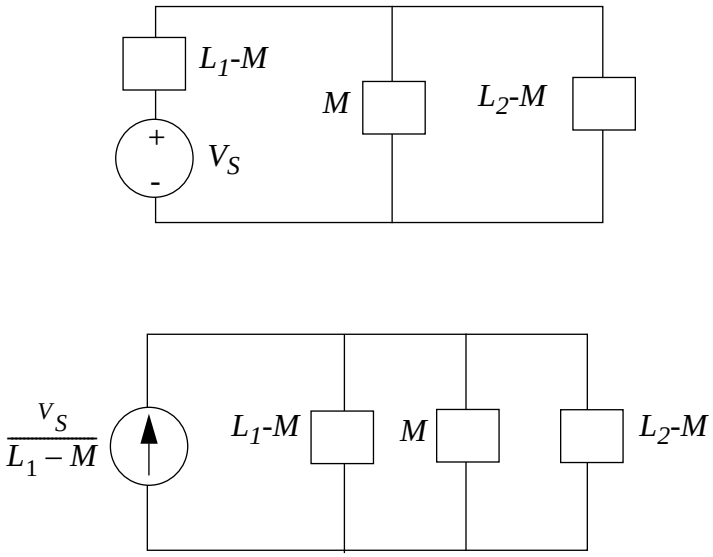


Figure 12.20:

Then, we know that the resistor R_2 obeys the law $V = IR$, so we know that $V' = I'R$, so knowing I', we can find V', which is equal to:

$$v_2'(0) = \frac{v_S R_2 M}{L_1 L_2 - M^2}.$$

Substituting in the numbers, we get the following:

$$v_2'(0) = 989.89.$$

From here, we can divide through by 19797.98 and get that $V_f = .05$

The final solution is therefore:

$$v_{2-up}(t) = (.05e^{-202.02t} - .05e^{-20000t}).$$

However, this is only the solution to the up-step. The solution to the down step must be added. ($u(t)$ is the unit step function.)

$$v_2(t) = v_{2-up}(t)u(t) - v_{2-up}(t - .005)u(t - .005).$$

This solution can be done out with less sleight-of-mind in the frequency domain.

We have already found the transfer function $\frac{v_2}{v_S}$:

$$\frac{v_2}{v_S} = \frac{R_2 K\sqrt{L_1 L_2}s}{(1-K^2)(L_1L_2)s^2 + (R_1L_2 + R_2L_1)s + R_1R_2}.$$

The input function, $v_S(s)$ can be expressed as the difference of two unit step functions, one shifted in time. We could deal directly with such a function, but it is much easier to deal with one unit step function, and, because superposition allows us to do so in a linear time-invariant system, we shift the response in time correspondingly. So we must find the response of the system to a unit step function. This is done by multiplying the system function by the Laplace transform of the unit step:

$$v_2 = \frac{R_2 K\sqrt{L_1 L_2}s}{(1-K^2)(L_1L_2)s^2 + (R_1L_2 + R_2L_1)s + R_1R_2}\frac{1}{s}.$$

Substituting in numbers, we get:

$$v_2(s) = \frac{2.45}{.002475s^2 + 50s + 10000}.$$

Finding the roots of the denominator and then doing partial fraction decomposition gives us:

$$v_2(s) = \frac{.05}{s + 202.02} - \frac{.05}{s + 20000}.$$

Then, an inverse Laplace transform results in:

$$v_{2-up}(t) = (.05e^{-202.02t} - .05e^{-20000t})u(t).$$

This is the response to only half of our input. We must add an inverted and shifted unit step to this, to get our final value:

$$v_2(t) = v_{2-up}(t)u(t) - v_{2-up}(t - .005)u(t - .005).$$

The graph of the output is shown in Figure 12.21. This does not resemble a square wave due to the fact that while the coupling constant is high enough to allow one natural frequency to be extremely high, the second natural frequency, which is a function of the sizes of the resistors and inductors, is too high and allows for a very quick decay. The second natural frequency must be decreased enough to allow the square wave to not dissipate quite as fast.

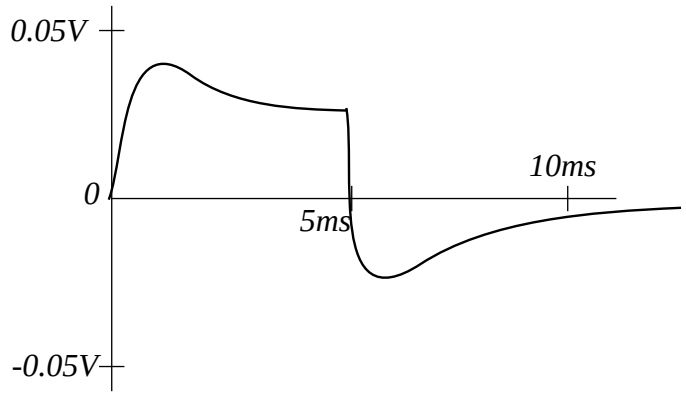


Figure 12.21:

ANS:: (a) $i_1' = \frac{L_2}{M^2-L_1L_2}R_1 i_1 - \left(\frac{R_2}{M} + \frac{R_2L_1L_2}{M(M^2-L_1L_2)}\right) i_2 - \frac{L_2}{M^2-L_1L_2}v_S, i_2' = \frac{-M}{M^2-L_1L_2}R_1 i_1 + \frac{R_2L_1}{M^2-L_1L_2}i_2 + \frac{M}{M^2-L_1L_2}v_S$, (c) $v_2(t) = (.05e^{-202.02t} - .05e^{-20000t})u(t) - (.05e^{-202.02(t-.005)} - .05e^{-20000(t-.005)})u(t-.005)$.

Problem 12.4 Assuming $y(t) = Be^{st}$, for each differential equation, find the particular solution and the general form of the homogeneous solution. Plot the natural frequencies in the complex plane.

Assume τ, α, ω_0 are constants. Do not worry about the dimensions of the right-hand side. Assume B always has the appropriate dimension.

1) $\frac{dx}{dt} + \frac{x}{\tau} = y$

2) $\frac{dx}{dt} + \frac{x}{\tau} = \frac{dy}{dt}$

3) $\frac{x}{\tau} = \frac{y}{\tau} + \frac{dy}{dt}$

4) $\frac{d^2x}{dt^2} + \omega_0^2 x = y$

For 5) and 6), assume α and ω_0 are both positive numbers.

5) $\frac{d^2x}{dt^2} + 2\alpha\frac{dx}{dt} + \omega_0^2 x = y$ Assume $\alpha > \omega_0$.

6) $\frac{d^2x}{dt^2} + 2\alpha\frac{dx}{dt} + \omega_0^2 x = \frac{dy}{dt}$ Assume $\alpha < \omega_0$.

Solution:

The easiest way to do these would clearly be via a lookup table to get the form of the homogeneous and particular solutions, but such a “solution” is not particularly insightful.

One realizes that if the driving function y is of the form e^{St} then the particular solution is of that form too. The homogeneous solution is determined also by inspection by substituting in $x = e^{At}$ and using elementary differential equation solving techniques. But again, that solution is very mechanical and probably reveals no new insight.

The alternate approach involves Laplace transforms.

Due to the unfortunate choice of s as one of the parameter variables in this problem, we will be doing the Laplace transforms in terms of s as always, but converting the form of y into Be^{St} - note the distinction between capital and lowercase. Another convention is as follows: if f is a time domain function, then F is its frequency-domain equivalent. In any answer identifying the form of the homogeneous and particular solutions, C and C_n are arbitrary constants whose value are not held between problem parts. Finally, $x(0)$ and $x'(0)$ represent initial values of a function and its derivative at zero, and are constants.

1)

$$\frac{dx}{dt} + \frac{x}{\tau} = Be^{St}.$$

Take the Laplace transform of this...

$$sX + \frac{X}{\tau} = \frac{B}{s - S} + x(0).$$

Simplify algebra to get:

$$X = \frac{B}{(s + \frac{1}{\tau})(s - S)} + \frac{x(0)}{s + \frac{1}{\tau}}.$$

A partial-fraction decomposition results in:

$$X = \left(\frac{-B}{\frac{1}{\tau} + S} + x(0)\right)\frac{1}{s + \frac{1}{\tau}} + \frac{B}{\frac{1}{\tau} + S}\frac{1}{s - S}.$$

This results in a time-domain solution of:

$$x = \left(\frac{-B}{\frac{1}{\tau} + S} + x(0)\right)e^{\frac{-t}{\tau}} + \frac{B}{\frac{1}{\tau} + S}e^{St}.$$

The homogeneous solution is of the form $Ce^{\frac{-t}{\tau}}$ and the particular solution is of the form Ce^{St}.

The natural frequencies of the function are S and $-\frac{1}{\tau}$, and are shown in Figure 12.22.

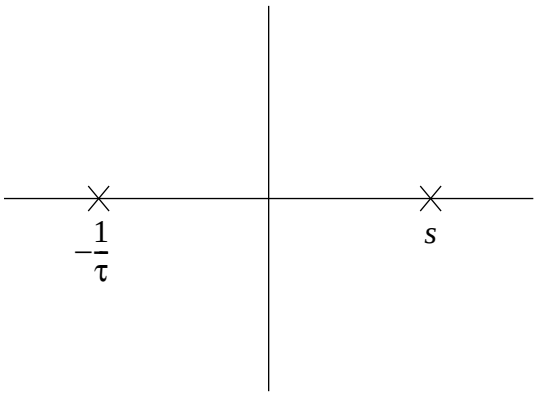


Figure 12.22:

2) If $y(t)$ is of the form Be^{St} then $y'(t)$ is of the form BSe^{St}, and a solution can be derived from the solution to part 1 by substituting BS for every instance of B.

$$x = \left(\frac{-BS}{\frac{1}{\tau}+S} + x(0)\right) e^{\frac{-t}{\tau}} + \frac{BS}{\frac{1}{\tau}+S} e^{St}.$$

The final solutions are the same as for part 1.

The homogeneous solution is of the form $Ce^{\frac{-t}{\tau}}$ and the particular solution is of the form Ce^{St}.

The natural frequencies of the function are S and $-\frac{1}{\tau}$, and are shown in Figure 12.23.

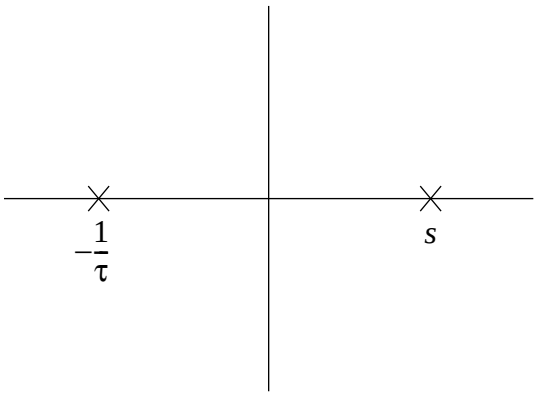


Figure 12.23:

3) This equation can be expressed as:

$$x = B(1 + S\tau)e^{St}.$$

There is no homogeneous solution, and the particular solution is of the form Ce^{St}. The natural frequency of the function is S as shown in Figure 12.24.

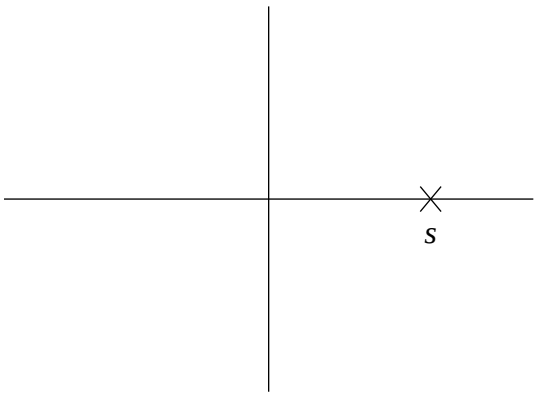


Figure 12.24:

4)

$$\frac{d^2x}{dt^2} + \omega_o^2 x = Be^{St}.$$

Taking the Laplace transform of this, one gets:

$$s^2X - sx(0) - x'(0) + \omega_o^2 X = \frac{B}{s - S}.$$

This can be rewritten as:

$$X = \frac{B}{(s - S)(s^2 + \omega_o^2)} + \frac{sx(0) + x'(0)}{s^2 + \omega_o^2}.$$

A partial-fraction decomposition results in the following:

$$X = X_0\frac{1}{s - S} + X_1\frac{s}{s^2 + \omega_o^2} + X_2\frac{\omega_o}{s^2 + \omega_o^2},$$

$$X_0 = \frac{B}{\omega_o^2 + S^2},$$

$$X_1 = \frac{-B}{\omega_o^2 + S^2} + x(0),$$

$$X_2 = \frac{-BS\frac{1}{\omega_o}}{\omega_o^2 + S^2} + \frac{x'(0)}{\omega_o}.$$

This can be converted into a time-domain equation of the form:

$$X = \frac{B}{\omega_o^2 + S^2}e^{St} + \left(\frac{-B}{\omega_o^2 + S^2} + x(0)\right) cos(\omega_o t) + \left(\frac{-BS\frac{1}{\omega_o}}{\omega_o^2 + S^2} + \frac{x'(0)}{\omega_o}\right) sin(\omega_o t)$$

The homogeneous solution is of the form $C_1 cos(\omega_o t) + C_2 sin(\omega_o t)$ and the particular solution is of the form Ce^{St}.

The natural frequencies of the function are S and $\pm j\omega_o$, and are shown in Figure 12.25.

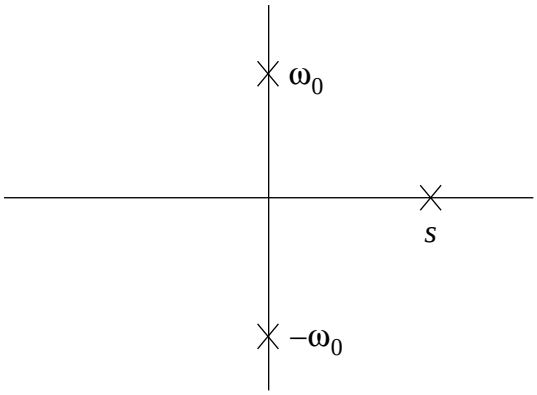


Figure 12.25:

5)

$$\frac{d^2x}{dt^2} + 2\alpha\frac{dx}{dt} + \omega_o^2 x = Be^{St}.$$

Converting this to the frequency domain, one gets:

$$s^2X - sx(0) - x'(0) + 2\alpha[sX - x(0)] + \omega_o^2 x = \frac{B}{s - S}.$$

This can be rewritten as:

$$X = \frac{B}{(s-S)(s^2+2\alpha s+\omega_o^2)} + \frac{(s+2\alpha)x(0)+x'(0)}{s^2+2\alpha s+\omega_o^2}$$

A partial-fraction decomposition results in:

$$X = X_0\frac{1}{s-S} + X_1\frac{1}{s^2+2\alpha s+\omega_o^2},$$

$$X_0 = \frac{B}{\omega_o^2+2\alpha S+S^2},$$

$$X_1 = \frac{-Bs-2B\alpha-BS}{\omega_o^2+2\alpha S+S^2} + (s+2\alpha)x(0)+x'(0).$$

In order to properly take an inverse Laplace transform, the second term must be written in the following form:

$$\frac{K(s+\alpha)}{s^2+2\alpha s+\omega_o^2} + \frac{L\sqrt{\omega_o^2-\alpha^2}}{s^2+2\alpha s+\omega_o^2}.$$

When this is done, the following result is gotten:

$$K = \frac{-B}{\omega_o^2+2\alpha S+S^2} + x(0),$$

$$L = \frac{1}{\sqrt{\omega_o^2-\alpha^2}}\left(\frac{-B\alpha-BS}{\omega_o^2+2\alpha S+S^2} + \alpha x(0)+x'(0)\right).$$

From this, an inverse Laplace transform can be taken. This intermediate step will come in useful for part 6.

$$x = Ke^{St} + Le^{-\alpha t}cos(\sqrt{\omega_o^2-\alpha^2}t) + \frac{M}{\sqrt{\omega_o^2-\alpha^2}}e^{-\alpha t}sin(\sqrt{\omega_o^2-\alpha^2}t),$$

$$K = \frac{B}{\omega_o^2+2\alpha S+S^2},$$

$$L = \frac{-B}{\omega_o^2 + 2\alpha S + S^2} + x(0),$$

$$M = \frac{-B\alpha - BS}{\omega_o^2 + 2\alpha S + S^2} + \alpha x(0) + x'(0).$$

However, since $|\alpha| > |\omega_o|$, $\sqrt{\omega_o^2 - \alpha^2}$ is imaginary, so we can write the previous statement as:

$$x = Ke^{St} + \frac{L}{2}e^{-\alpha t}(e^{j\sqrt{\omega_o^2-\alpha^2}} + e^{-j\sqrt{\omega_o^2-\alpha^2}}) + \frac{M}{2j}e^{-\alpha t}(e^{j\sqrt{\omega_o^2-\alpha^2}} - e^{-j\sqrt{\omega_o^2-\alpha^2}}).$$

This can be simplified to:

$$x = Ke^{st} + \frac{L + \frac{M}{\sqrt{\alpha^2-\omega_o^2}}}{2}e^{-\alpha-\sqrt{\alpha^2-\omega_o^2}} + \frac{L - \frac{M}{\sqrt{\alpha^2-\omega_o^2}}}{2}e^{-\alpha+\sqrt{\alpha^2-\omega_o^2}}.$$

The homogeneous solution is of the form $C_1e^{-\alpha-\sqrt{\alpha^2-\omega_o^2}} + C_2e^{-\alpha+\sqrt{\alpha^2-\omega_o^2}}$ and the particular solution is of the form Ce^{St}.

The natural frequencies of the function are S and $-\alpha \pm \sqrt{\alpha^2 - \omega_o^2}$, and are shown in Figure 12.26.

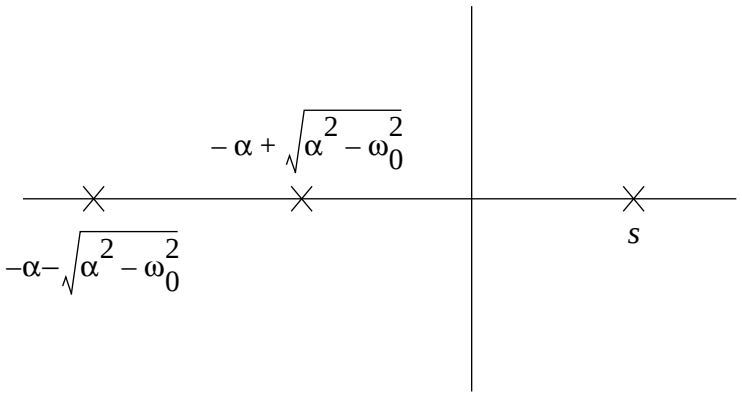


Figure 12.26:

6) We start with this intermediate result derived in part 5:

$$x = Ke^{St} + Le^{-\alpha t}cos(\sqrt{\omega_o^2 - \alpha^2}t) + \frac{M}{\sqrt{\omega_o^2 - \alpha^2}}e^{-\alpha t}sin(\sqrt{\omega_o^2 - \alpha^2}t),$$

$$K = \frac{B}{\omega_o^2 + 2\alpha S + S^2},$$

$$L = \frac{-B}{\omega_o^2 + 2\alpha S + S^2} + x(0),$$

$$M = \frac{-B\alpha - BS}{\omega_o^2 + 2\alpha S + S^2} + \alpha x(0) + x'(0).$$

We must replace all instances of B with BS, which results in the following.

$$K = \frac{BS}{\omega_o^2 + 2\alpha S + S^2},$$

$$L = \frac{-BS}{\omega_o^2 + 2\alpha S + S^2} + x(0),$$

$$M = \frac{-BS\alpha - BS^2}{\omega_o^2 + 2\alpha S + S^2} + \alpha x(0) + x'(0).$$

The homogeneous solution is of the form $C_1e^{-\alpha}cos(\sqrt{\omega_o^2 - \alpha^2}t) + C_2e^{-\alpha}sin(\sqrt{\omega_o^2 - \alpha^2}t)$ and the particular solution is of the form Ce^{St}.

The natural frequencies of the function are S and $-\alpha \pm j\sqrt{\omega_o^2 - \alpha^2}$, and are shown in Figure 12.27.

ANS:: (1) homogeneous: $Ce^{\frac{-t}{\tau}}$, particular: Ce^{St} (2) homogeneous: $Ce^{\frac{-t}{\tau}}$, particular: Ce^{St} (3) homogeneous: none, particular: Ce^{St} (4) homogeneous: $C_1cos(\omega_o t) + C_2sin(\omega_o t)$, particular: Ce^{St}, (5) homogeneous: $C_1e^{-\alpha-\sqrt{\alpha^2-\omega_o^2}} + C_2e^{-\alpha+\sqrt{\alpha^2-\omega_o^2}}$, particular: Ce^{St}, (6) homogeneous: $C_1e^{-\alpha}cos(\sqrt{\omega_o^2 - \alpha^2}t) + C_2e^{-\alpha}sin(\sqrt{\omega_o^2 - \alpha^2}t)$, particular: Ce^{St}.

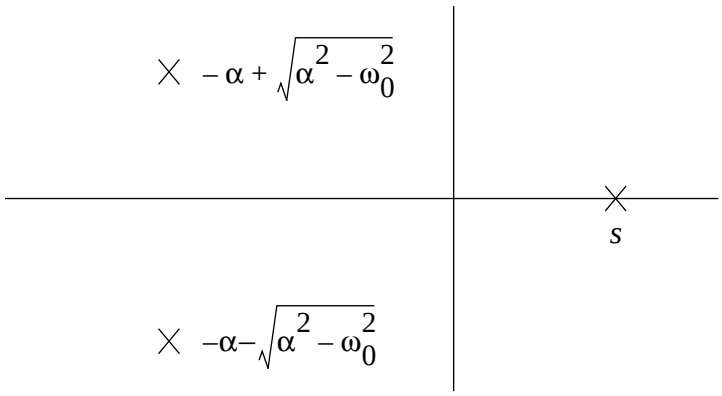


Figure 12.27:

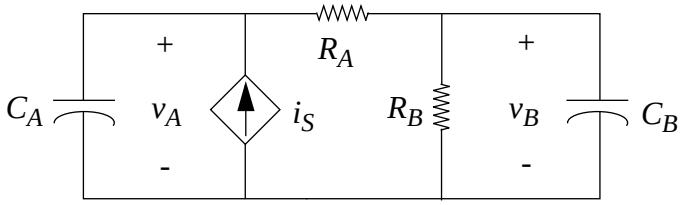


Figure 12.28:

Problem 12.5 The circuit in in Figure 12.28 is the electrical analogue of a temperature control system.

Assuming $C_A = 1F, C_B = 4F, R_A = 1\Omega, R_B = 4\Omega$.

$i_S = K(V_0 - v_B)^2$ where $K = 25A/V^2, V_0 = 1.1V$

a) Write dynamical equations for this network in state form. Use v_A and v_B as state variables.

(As a check on your state equations, the stable steady-state value of v_B is $1V$. That is, you should have $dv_A/dt = dv_B/dt = 0$ for $v_B = 1V$.)

b) Now assume $v_A = V_A + v_0$ and $v_B = V_B + v_b$, where V_A and V_B are the steady-state values and v_a and v_b are small variations. Determine a small-signal *linear* circuit model in which v_a and b_b are the state variables.

c) Is the zero-input response of the small-signal circuit underdamped, overdamped, or critically damped?

Solution:

a) Two node equations:

$$C_A\frac{dv_A}{dt}+\frac{v_A-v_B}{R_A}=K(V_0-v_B)^2, C_B\frac{dv_B}{dt}+\frac{v_B}{R_B}=\frac{v_A-v_B}{R_A}.$$

b) Since $i_S=K(V_0-v_B)^2$, then the following small-signal approximation is valid:

$$\frac{i_s}{v_b}=\frac{di_S}{dv_B}=-2K(V_0-V_B).$$

$$i_s=-2K(V_0-V_B)v_b$$

See Figure 12.29 for a small-signal model.

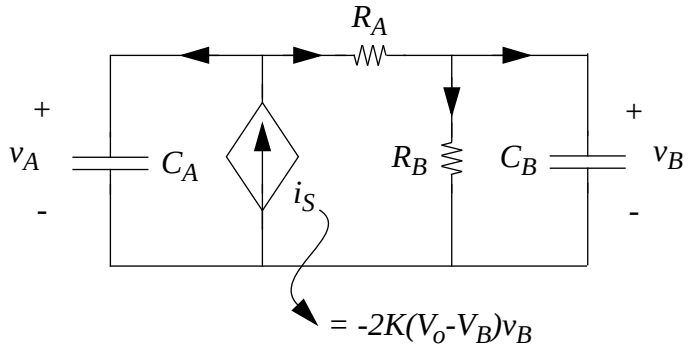


Figure 12.29:

c) First, write two new state equations using the small-signal model:

$$C_A\frac{dv_a}{dt}+\frac{v_a-v_b}{R_A}=-2K(V_0-V_B)v_b,$$

$$C_B\frac{dv_b}{dt}+\frac{v_b}{R_B}=\frac{v_a-v_b}{R_A}.$$

We substitute in the numerical values given, and get the following:

$$\frac{dv_a}{dt}+v_a-v_b=-5v_b,$$

$$4\frac{dv_b}{dt}+.25v_b=v_a-v_b.$$

We can eliminate v_a, getting the following:

$$16\frac{d^2v_b}{dt^2} + 21\frac{dv_b}{dt} + 21 = 0.$$

This has the following characteristic equation:

$$16s^2 + 21s + 21 = 0.$$

Since $21^2 - 4(16)(21) < 0$, the system is overdamped.

ANS:: (a) $C_A\frac{dv_A}{dt} + \frac{v_A - v_B}{R_A} = K(V_0 - v_B)^2, C_B\frac{dv_B}{dt} + \frac{v_B}{R_B} = \frac{v_A - v_B}{R_A}$, (b) $i_s = -2K(V_0 - V_B)v_b$, (c) Overdamped.

Problem 12.6 In the circuit in Figure 12.30, the switch has been in position 1 for all $t < 0$. At $t = 0$, the switch is moved to position 2 (and remains there for $t > 0$). Find and sketch $v_C(t)$ and $i_L(t)$ for $t > 0$.

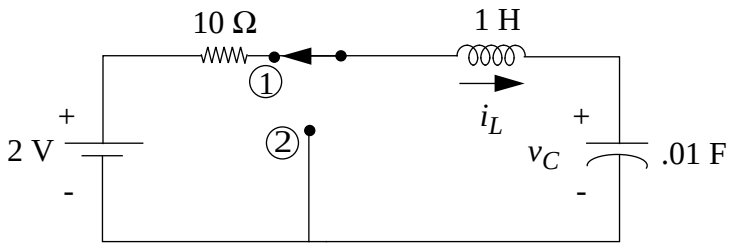


Figure 12.30:

Solution:

At time $t > 0$, the circuit becomes an LC oscillator.

The natural frequency ω_o is equal to $\sqrt{\frac{1}{LC}}$. Since the capacitor starts out charged, initially, the voltage across the capacitor is a cosine function with maximum amplitude of $2V$. The current through the inductor is the same as the current through the capacitor, and it is characterized by the capacitor I-V relation: $i_C = C\frac{dv_C}{dt}$. Taking the derivative, we get a negative sinusoidal relation.

ANS:: $v_C = 2cos(\sqrt{\frac{1}{LC}}t), i_L = -2\sqrt{\frac{C}{L}}sin(\sqrt{\frac{1}{LC}}t)$.

See Figures 12.31 and 12.32 for the plots of these two functions.

Problem 12.7 Figure 10.75 (Problem 10.8 in the chapter on first order transients) illustrated a parasitic inductance associated with VLSI package pins. Figure 12.33 is a modification of Figure 10.75 and shows a lumped parasitic capacitor C_P associated with the

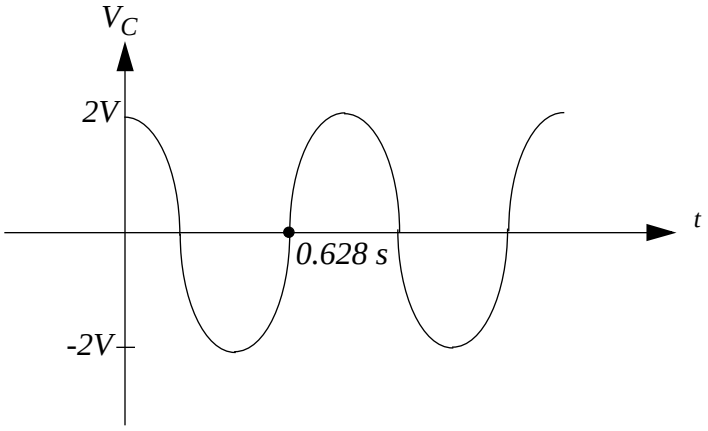


Figure 12.31:

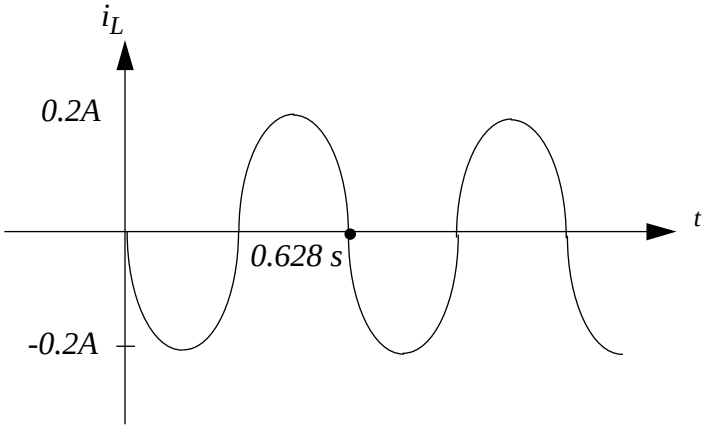


Figure 12.32:

power node within the VLSI chip. In this problem, we will study the combined effect of the parasitic inductance L_P and capacitance C_P.

Assume that the input B is 0V at all times. Assume further that the input A has 0V applied to it initially. At time $t = t_0$, a 5V step is applied at the input A. Plot the form of v_P as a function of time for the underdamped and overdamped cases, assuming that $v_P = V_S$ for $t < t_0$. Clearly show the value of v_P just prior to t_0 and just after t_0. Assume that the on resistance of a MOSFET is given by the relation $\frac{L}{W}R_n$ and that the MOSFET's threshold voltage is $V_T < V_S$. Also assume that $V_T < 5V$. Compare this result with that for the inductor acting alone as computed in Problem 10.8 (Figure 10.75) in the chapter on first order transients.

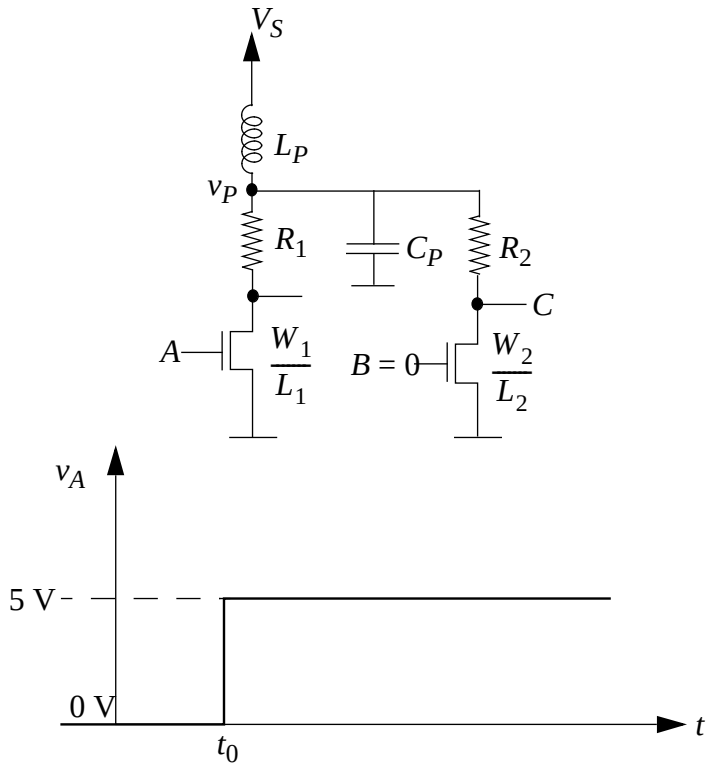


Figure 12.33:

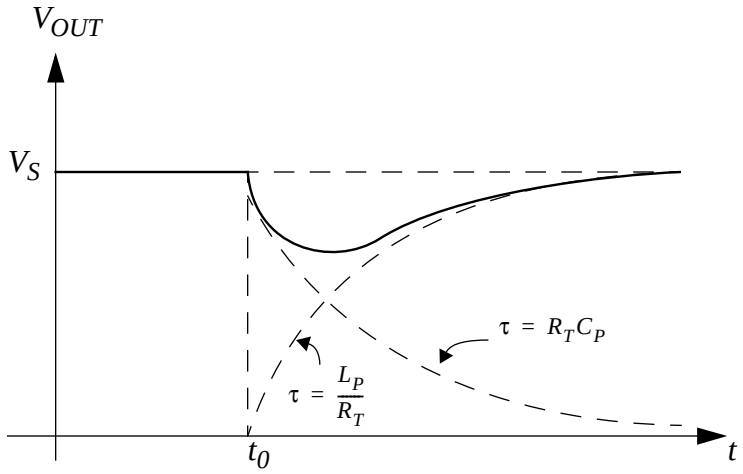
Solution:

Before the switch occurs, the resistors R_1 and R_2 are floating. We are also given that the voltage across the capacitor for $t < 0$ is V_S.

Next, the MOSFET is closed, and the voltage across the capacitor starts dropping, since the inductor current cannot build up suddenly and so the capacitor supplies the current. Note that resistor R_2 is still floating.

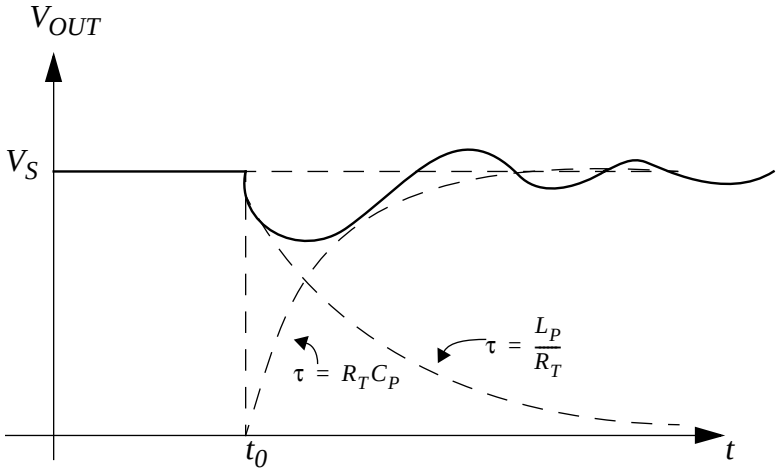
This occurs with a time constant of $\tau = C_P(R_1 + R_{ON})$. Soon the inductor current

builds up and the voltage will rise again towards V_S. The lower envelope of this rise will have a time constant $\tau = \frac{L}{R}$. If the system is overrdamped, then the solution is as shown in Figure 12.34 while the underdamped case is shown in Figure 12.35.



Overdamped Case

Figure 12.34:



Underdamped Case

Figure 12.35:

Chapter 13

SSS: Impedance and Frequency Response

Exercises

Exercise 13.1 Find the magnitude and phase of each of the following expressions

a) $(8+j7)(5e^{j30^\circ})(e^{-j39^\circ})(0.3-j0.1)$

b) $\frac{(8.5+j34)(20e^{-j25^\circ})(60)(\cos 10^\circ + j\sin 10^\circ)}{(25e^{j20^\circ})(37e^{j23^\circ})}$

c) $(25e^{j30^\circ})(10e^{j27^\circ})(14-j13)/(1-j2)$

d) $(13e^{j(15^\circ+j1.5)})(6e^{(1-j30^\circ)})$

Solution:

a) $(8+j7) = 10.63\ e^{41.18^\circ \cdot j}$
$(0.3-j0.1) = 0.316e^{-18.43Z^\circ \cdot j}$
$MAG = 16.8$
$PHASE = 13.75\,\text{deg}$

b) $MAG = \frac{35 \cdot 20 \cdot 60 \cdot 1}{25 \cdot 37} = 45.47$
$PHASE = 76^\circ - 25^\circ + 10^\circ - 20^\circ - 23^\circ = 18^\circ$

c) $MAG = \frac{25 \cdot 10 \cdot 19 \cdot 1}{2.236} = 2136$

$PHASE = 30^\circ + 27^\circ - 42^\circ + 63^\circ = 78^\circ$

d) $13e^{j(15+1.5j)} \cdot 6e^{(1-30j)} = \frac{13 \cdot e^{j15} e^{-1.5} \cdot 6 \cdot e^1}{e^{j30}}$

$MAG = 47.3$

$PHASE = -15^\circ$

ANS:: (a) $MAG = 16.8$, $PHASE = 13.75\,\text{deg}$, (b) $MAG = 45.47$, $PHASE = 18^\circ$, (c) $MAG = 2136$, $PHASE = 78^\circ$, (d) $MAG = 47.3$, $PHASE = -15^\circ$

Exercise 13.2 Find the real and imaginary parts of the following expressions

a) $(3 + j5)(4e^{j50^\circ})(7e^{-j20^\circ})$

b) $(10e^{j50^\circ})(e^{j20^\circ})$

c) $(10e^{j50^\circ})(e^{j\omega t})$

d) $Ee^{j\omega t}$where $E = |E|e^{j\Theta}$

Solution:

a) $5.83e^{j59^\circ} \cdot 4e^{j50^\circ} \cdot 7e^{-j20^\circ} = 163.26e^{89j} \quad \rightarrow \quad 2.84 + j163$

b) $10e^{j70^\circ} \quad \rightarrow \quad 3.42 + j9.4$

c) $10e^{j(\omega t+50)} \quad \rightarrow \quad 10(\cos(\omega t + 50^\circ) + j\sin(\omega t + 50^\circ))$

d) $|E|\ e^{j(\omega t+\theta)} \quad \rightarrow \quad |E|(\cos(\omega t + \theta) + j\sin(\omega t + \theta))$

ANS:: (a) $2.84 + j163$, (b) $3.42 + j9.4$, (c) $10(\cos(\omega t + 50^\circ) + j\sin(\omega t + 50^\circ))$, (d) $|E|(\cos(\omega t + \theta) + j\sin(\omega t + \theta))$

Exercise 13.3 Find the system function V_L/I for the network shown in Figure 13.1. Then find the response $v_L(t)$ for $i(t) = I\cos\omega t$ under steady state conditions.

Solution:

$$V_L = \frac{RILs}{Ls + R} \quad \rightarrow \quad \frac{V_L}{I} = \frac{RLs}{Ls + R}$$

l

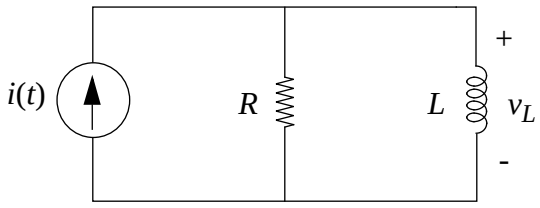


Figure 13.1:

$$|\frac{V_L}{I}| = \frac{RL\omega}{\sqrt{(L\omega)^2 + R^2}} \text{ , angle of } \frac{V_L}{I} = \tan^{-1}\left(\frac{R}{\omega L}\right) = \phi$$

$$v_L(t) = \frac{RLI\omega}{\sqrt{(L\omega)^2 + R^2}} \cdot \cos(\omega t + \phi)$$

ANS:: $\frac{V_L}{I} = \frac{RLs}{Ls+R}$, $v_L(t) = \frac{RLI\omega}{\sqrt{(L\omega)^2+R^2}} \cdot \cos(\omega t + \phi)$, $\phi = \tan^{-1}\left(\frac{R}{\omega L}\right)$

Exercise 13.4 Referring to Figure 13.2, given $i(t) = I_0 \cos \omega t$, where $I_0 = 3mA$ and $\omega = 10^6$ rad/sec, determine $v(t)$ in the sinusoidal steady state. Assume $R = 1k\Omega$ and $L = 1mH$.

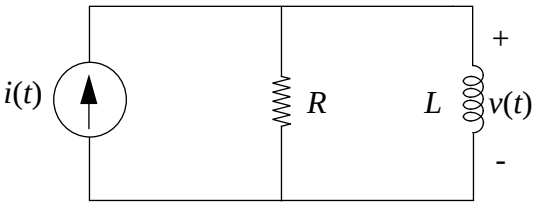


Figure 13.2:

Solution:

$$V = \frac{I_0 LsR}{Ls + R} = +\frac{3}{2} + \frac{3}{2}j = \frac{3}{\sqrt{2}}\, e^{j45^\circ}$$

Therefore,

$$v(t) = \frac{3}{\sqrt{2}} \cos(10^6 \cdot t + 45^\circ)$$

ANS:: $v(t) = \frac{3}{\sqrt{2}} \cos(10^6 \cdot t + 45^\circ)$

Exercise 13.5 The two-terminal linear network in Figure 13.3 is known to contain exactly two elements. The magnitude of the impedance function is as shown, (log-log coordinates).

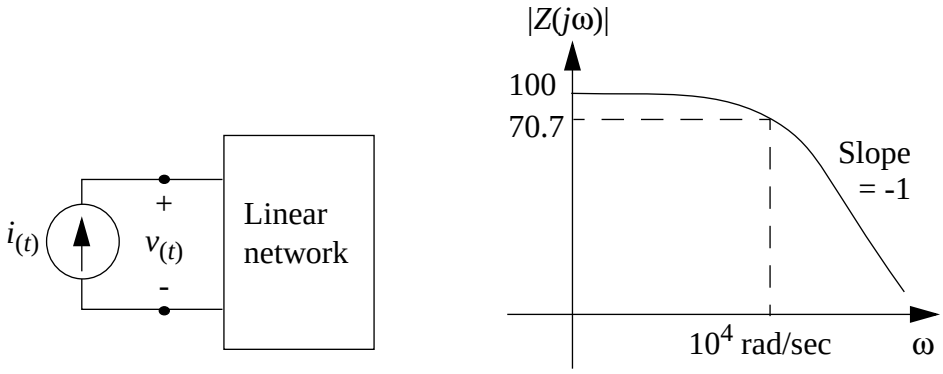


Figure 13.3:

Draw a two-element circuit that has the impedance magnitude function indicated in the sketch. Specify the numerical value of each element.

Solution:

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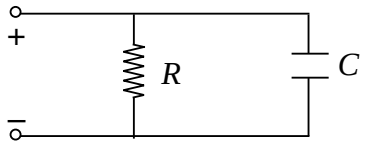


Figure 13.4:

$Z = \frac{R}{j\omega RC+1}$

$\frac{1}{RC} = 10^4 rad/s$

$R = 100\Omega$

$C = 1\mu F$

ANS:: $Z = \frac{R}{j\omega RC+1}$, $\frac{1}{RC} = 10^4 rad/s$, $R = 100\Omega$, $C = 1\mu F$

Exercise 13.6 For each of the circuits shown in Figure 13.5, select the magnitude of the frequency response for the system function (i.e., impedance, admittance or transfer function) from those given. It is not necessary to relate the critical frequencies to the circuit parameters, and you may choose a magnitude response more than once.

Please note that the magnitude responses, except (7), are sketched on a log-log scale, with slopes labeled.

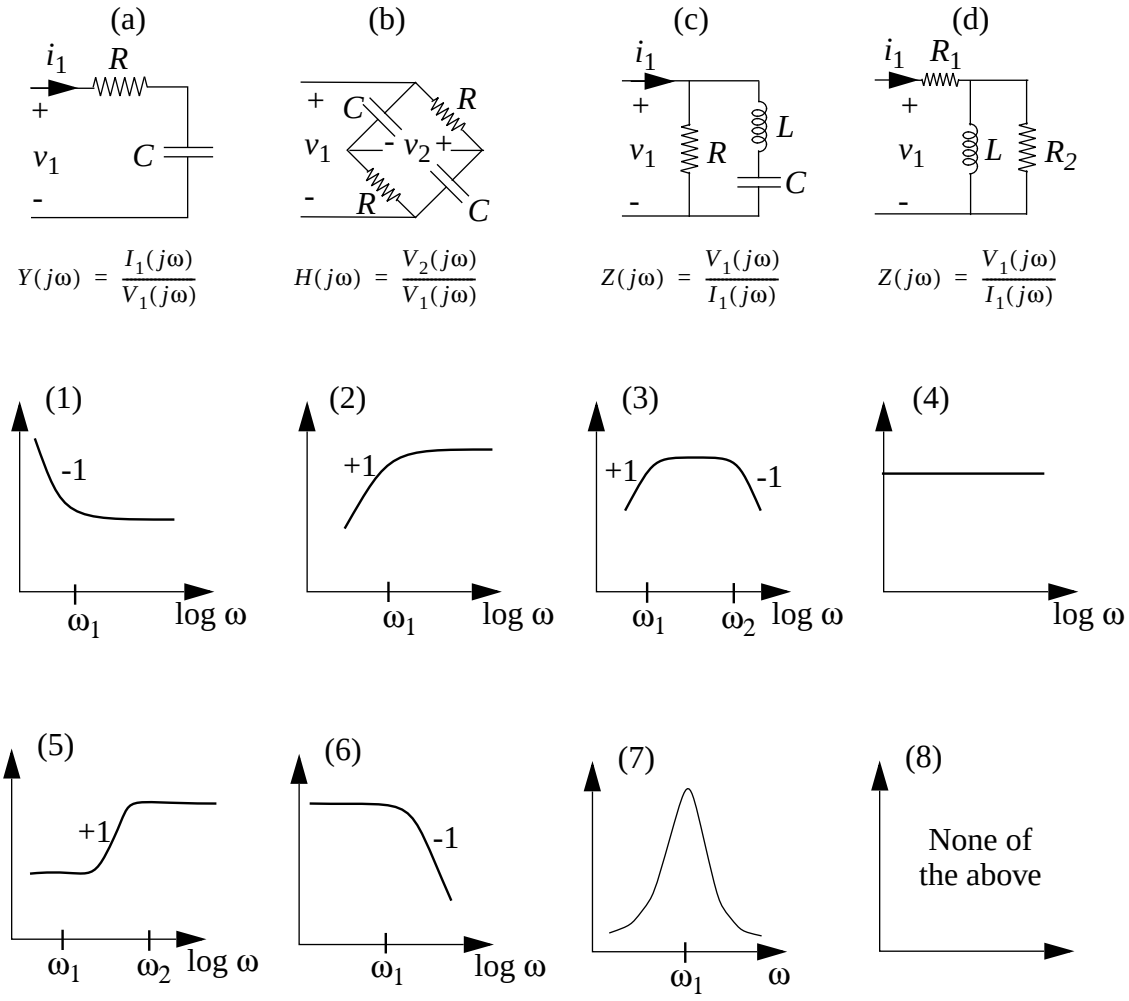


Figure 13.5:

Solution:

a	b	c	d
2	4	8	5

ANS:: (a) 2 (b) 4 (c) 8 (d) 5

Exercise 13.7 A linear network is excited with a sinusoidal voltage $v_I(t) = \cos(t - \frac{5\pi}{8})$ for all time, as shown in Figure 13.6.

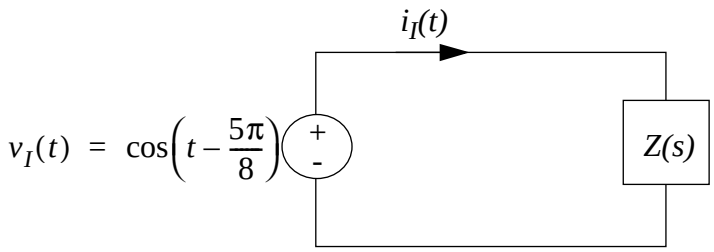


Figure 13.6:

The current observed under the sinusoidal steady-state conditions is $i_I(t) = \sqrt{2}\sin(t + \frac{\pi}{8})$.

What is $Z(s = j1)$, the impedance of the network at an excitation frequency of one radian per second?

Solution:

$$Z = \frac{V}{I} = \frac{e^{j(t-5\pi/8)}}{\sqrt{2}\, e^{j(t+\pi/8-\pi/2)}}$$

$$\text{since} \quad \sin\left(t + \frac{\pi}{8}\right) = \cos\left(\frac{\pi}{2} - t - \frac{\pi}{8}\right) = \cos\left(t - \frac{3\pi}{8}\right)$$

$$Z_{s=j} = \frac{1}{\sqrt{2}}\, e^{-(\pi/4)j}$$

ANS:: $Z_{s=j} = \frac{1}{\sqrt{2}}\, e^{-(\pi/4)j}$

Exercise 13.8 Find $v_2(t)$ in the sinusoidal steady state in Figure 13.7. Assume $L = 10H$, $R_1 = 120\Omega$, and $R_2 = 60\Omega$.

Solution:

$$\frac{v_2}{v_i} = \frac{Ls \mid\mid R_2}{R_1 + Ls \mid\mid R_2} = |H(j\omega)|\, e^{j\phi}$$

where

$$|H(j\omega)| = \frac{\omega R_2 L}{\sqrt{\omega^2 L^2 (R_1 + R_2)^2 + {R_1}^2 {R_2}^2}}$$

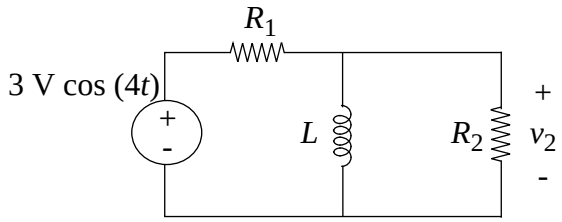


Figure 13.7:

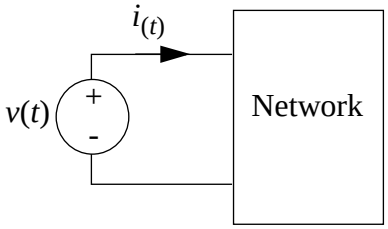


Figure 13.8:

and

$$\phi = \pi/2 - \tan^{-1}\left[\frac{\omega L(R_1 + R_2)}{R_1 R_2}\right]$$

For $\omega = 4, \quad \phi = \pi/4$, and $|H(j\omega)| = \frac{1}{3\sqrt{2}}$,

$$v_2(t) = \frac{1}{\sqrt{2}}\ \cos\left(4t + \frac{\pi}{4}\right)$$

ANS:: $v_2(t) = \frac{1}{\sqrt{2}}\ \cos\left(4t + \frac{\pi}{4}\right)$

Exercise 13.9 A sinusoidal test signal is applied to a linear network that is constructed from exactly two circuit elements as shown in Figure 13.8.

The magnitude portion of the Bode plot for the impedance $Z(j\omega) = \frac{V(j\omega)}{I(j\omega)}$ is shown in Figure 13.9.

Draw the network and find the element values.

Solution:

$$\frac{R}{L} = 2 \times 10^6 rad/s$$

$$\frac{V(j\omega)}{I(j\omega)} = R + L\omega j$$

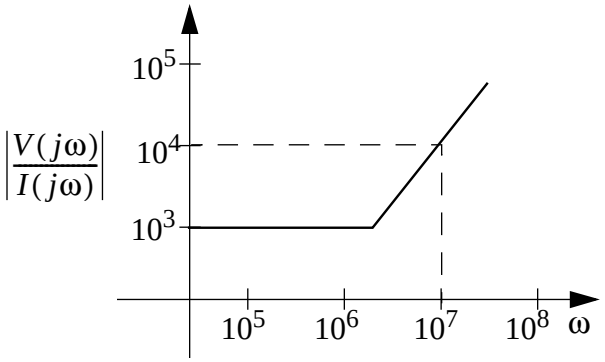


Figure 13.9:

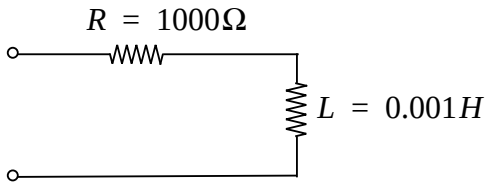


Figure 13.10:

ANS:: $\frac{R}{L} = 2 \times 10^6 rad/s$, $\frac{V(j\omega)}{I(j\omega)} = R + L\omega j$

Exercise 13.10 The circuit shown in Figure 13.11 is a highly simplified model of a power transmission system.

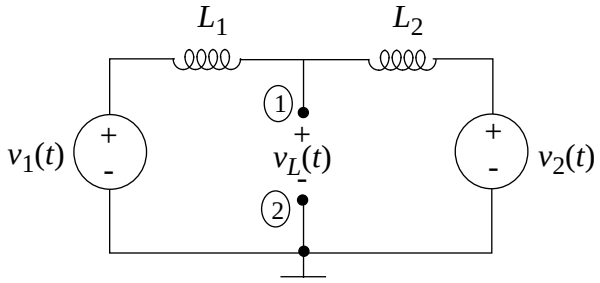


Figure 13.11:

$v_1(t)$ and $v_2(t)$ are the voltages of two power generators:

$v_1 = V\cos\omega t \quad v_2 = V\cos(\omega t + \Phi)$

Find the Thévenin equivalent of this circuit at the terminals 1-2 in terms of a complex amplitude V_{oc} and a complex Thévenin impedance Z_{th}.

Solution:

$$R_{TH} = Z_{TH} = \frac{L_1 s - L_2 L s}{L_1 s + L_2 s} = \frac{L_1 L_2 s}{L_1 + L_2} = Z_{TH}$$

By superposition,

$$V_{oc} = \frac{V_1 L_2 s}{L_1 s + L_2 s} + \frac{V_2 L_1 s}{L_1 s + L_2 s} = \frac{L_2 + L_1 e^{j\phi}}{L_1 + L_2} \cdot V$$

ANS:: $R_{TH} = Z_{TH} = \frac{L_1 L_2 s}{L_1 + L_2}, V_{oc} = \frac{L_2 + L_1 e^{j\phi}}{L_1 + L_2} \cdot V$

Exercise 13.11 Write expressions for $H(j\omega) = V_o/V_i$, its magnitude $|H(j\omega)|$ and its phase angle $\angle H(j\omega)$, as a function of ω in the four cases shown in Figure 13.12.

Solution:

(a)

$$\frac{V_o}{V_i} = \frac{\frac{1}{Cs}}{\frac{1}{Cs} + R} = \frac{1}{RCs + 1} = \frac{1}{\sqrt{(\omega RC)^2 + 1}}\, e^{j\phi}$$

$$\phi = \tan^{-1}(-RC\omega)$$

(b)

$$\frac{V_o}{V_i} = \frac{Ls}{Ls + R} = \frac{\omega L}{\sqrt{(\omega L)^2 + R^2}}\, e^{j\phi}$$

$$\phi = \tan^{-1}\left(\frac{R}{\omega L}\right)$$

(c)

$$\frac{V_o}{V_i} = \frac{R}{R + \frac{1}{Cs}} = \frac{RCs}{RCs + 1} = \frac{RC\omega}{\sqrt{(RC\omega)^2 + 1}}\, e^{j\phi}$$

$$\phi = \tan^{-1}\left(\frac{1}{RC\omega}\right)$$

For $C = 1\mu F$ and $R = 1M\Omega$,

$$|H(j\omega)| = \frac{\omega}{\sqrt{\omega^2 + 1}} \text{ and } \phi = \tan^{-1}\left(\frac{1}{\omega}\right)$$

(d)

$$\frac{V_o}{V_i} = \frac{R}{R + Ls} = \frac{R}{\sqrt{(\omega L)^2 + R^2}}\, e^{j\phi}$$

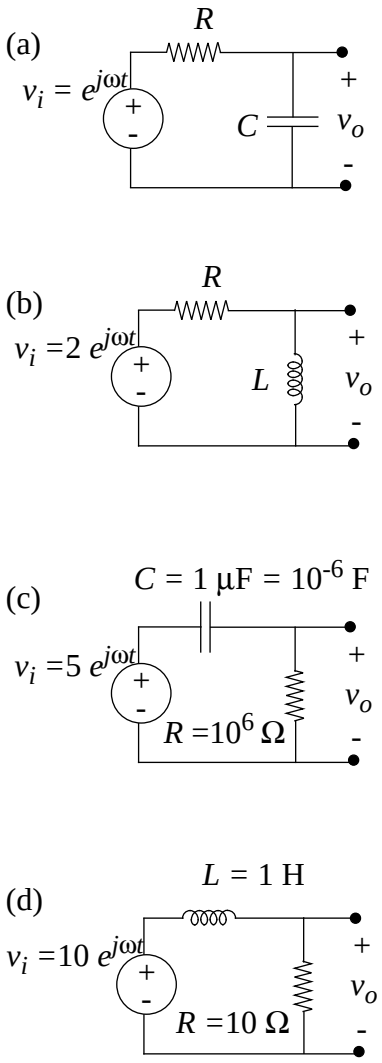

(a)
R
$v_i = e^{j\omega t}$
+
-
C
+
v_o
-
(b)
R
$v_i = 2\ e^{j\omega t}$
+
-
L
+
v_o
-
(c)
$C = 1\ \mu F = 10^{-6}$ F
$v_i = 5\ e^{j\omega t}$
+
-
$R = 10^6\ \Omega$
+
v_o
-
(d)
L = 1 H
$v_i = 10\ e^{j\omega t}$
+
-
$R = 10\ \Omega$
+
v_o
-

Figure 13.12:

$$\phi = \tan^{-1}\left(-\frac{\omega L}{R}\right)$$

For $R = 10\Omega$ and $L = 1$Henry,

$$\frac{V_o}{V_i} = \frac{10}{\sqrt{\omega^2 + 100}}\, e^{j\phi}$$

$$\phi = \tan^{-1}(-\frac{\omega}{10})$$

ANS:: (a) $\frac{V_o}{V_i} = \frac{1}{\sqrt{(\omega RC)^2+1}} e^{j\phi}, \phi = \tan^{-1}(-RC\omega)$, (b) $\frac{V_o}{V_i} = \frac{\omega L}{\sqrt{(\omega L)^2+R^2}} e^{j\phi}, \phi = \tan^{-1}\left(\frac{R}{\omega L}\right)$, (c) $\frac{V_o}{V_i} = \frac{RC\omega}{\sqrt{(RC\omega)^2+1}} e^{j\phi}, \phi = \tan^{-1}\left(\frac{1}{RC\omega}\right)$, (d) $\frac{V_o}{V_i} = \frac{R}{\sqrt{(\omega L)^2+R^2}}\ e^{j\phi}, \phi = \tan^{-1}\left(-\frac{\omega L}{R}\right)$

Exercise 13.12 Plot the log magnitude and the phase angle, both as functions of frequency (on a logarithmic scale), of the complex quantity.

$$H(j\omega) = \frac{1 - j\omega}{1 + j\omega}$$

Label all significant asymptotes, slopes and break points.

Solution:

*MAGNITUDE:

$$|H(j\omega)| = \frac{\sqrt{1^2 + \omega^2}}{\sqrt{1^2 + \omega^2}} = 1$$

Or in decibels,

$$|H(j\omega)| = 20 \cdot \log 1$$

$$|H(j\omega)| = 0\ dB$$

*PHASE ANGLE:

$$\angle H(j\omega) = \angle numerator - \angle denominator = tan^{-1}\frac{-\omega}{1} - tan^{-1}\frac{\omega}{1}$$

$$\angle H(j\omega) = -2 \cdot tan^{-1}\omega$$

As $\omega \rightarrow \infty$, $\angle H(j\omega) \rightarrow -2(90^\circ) \rightarrow -180^\circ$

As $\omega \rightarrow 0$, $\angle H(j\omega) \rightarrow -2(0^\circ) \rightarrow 0^\circ$

As $\omega = 1$, the cutoff frequency, $\angle H(j\omega) = -2(45^\circ) = -90^\circ$

ANS:: $H(j\omega) = \frac{1-j\omega}{1+j\omega}$, magnitude: $|H(j\omega)| = 1$, or in decibels, $|H(j\omega)| = 0\ dB$, phase angle: $\angle H(j\omega) = -2 \cdot tan^{-1}\omega$

Exercise 13.13 In the network shown in Figure 13.13,

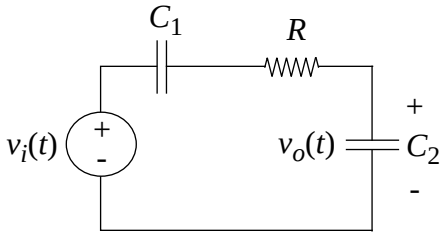


Figure 13.13:

$R = 1kilohm \quad C_1 = 20\mu F \quad C_2 = 20\mu F$

a) Determine the magnitude and phase of $H(j\omega)$, the transfer function relating V_0/V_i.

b) Given $v_i(t) = \cos 100t + \cos 10000t$, determine the sinusoidal steady state output voltage, $v_o(t)$.

Solution:

$$\frac{V_o}{V_i} = \frac{\frac{1}{C_2 s}}{\frac{1}{C_2 s} + R + \frac{1}{C_1 s}} = \frac{1}{1 + \frac{C_2}{C_1} + RC_2 s} = \frac{1}{2 + \frac{j\omega}{50}}$$

a)

$$\frac{V_o}{V_i} = \frac{1}{\sqrt{1 + \frac{\omega^2}{100^2}}} \left(\frac{1}{2}\right) e^{j\phi}$$

$$\phi = \tan^{-1}(-\frac{\omega}{100})$$

b) $\omega = 100$,

$$\frac{V_o}{V_i} = \frac{1}{2\sqrt{2}}\, e^{-j45^\circ} \quad \rightarrow \quad v_o(t) = \frac{1}{2\sqrt{2}} \cos(100t - 45^\circ)$$

$\omega = 10,000$,

$$\frac{V_o}{V_i} = \frac{1}{200.01}\, e^{-j89.4^\circ} \quad \rightarrow \quad v_o(t) = \frac{1}{200.01}\cos(10,000t - 89.4^\circ)$$

$$v_o(t) = \frac{1}{2\sqrt{2}}\cos(100t - 45^\circ) + \frac{1}{200.01}\cos(10,000t - 89.4^\circ)$$

ANS:: (a) $\frac{V_o}{V_i} = \frac{1}{\sqrt{1+\frac{\omega^2}{100^2}}}$ $\left(\frac{1}{2}\right)$ $e^{j\phi}, \phi = \tan^{-1}(-\frac{\omega}{100})$, (b) $v_o(t) = \frac{1}{2\sqrt{2}}\cos(100t - 45^\circ) + \frac{1}{200.01}\cos(10,000t - 89.4^\circ)$

Exercise 13.14 Find $v_2(t)$ in the sinusoidal steady state for the circuit in Figure 13.14.

$L = 10H \quad R_1 = 120\Omega \quad R_2 = 60\Omega$

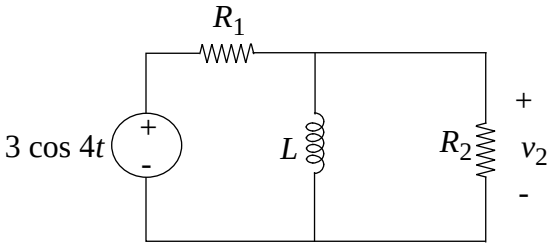


Figure 13.14:

Solution:

$$\frac{v_2}{v_i} = \frac{Ls \mid\mid R_2}{R_1 + Ls \mid\mid R_2} = |H(j\omega)|\, e^{j\phi}$$

where

$$|H(j\omega)| = \frac{\omega R_2 L}{\sqrt{\omega^2 L^2 (R_1 + R_2)^2 + {R_1}^2 {R_2}^2}}$$

and

$$\phi = \pi/2 - \tan^{-1}\left[\frac{\omega L(R_1 + R_2)}{R_1 R_2}\right]$$

For $\omega = 4, \quad \phi = \pi/4$, and $|H(j\omega)| = \frac{1}{3\sqrt{2}}$,

$$v_2(t) = \frac{1}{\sqrt{2}} \cos\left(4t + \frac{\pi}{4}\right)$$

ANS:: $v_2(t) = \frac{1}{\sqrt{2}} \cos\left(4t + \frac{\pi}{4}\right)$

Exercise 13.15

a) Write the transfer function $V_o(s)/V_i(s)$ for the circuit in Figure 13.15.

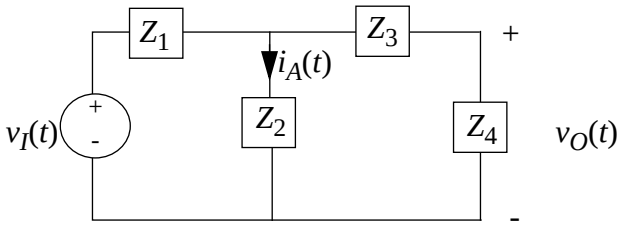


Figure 13.15:

b) Write the transfer function $I_a(s)/V_i(s)$.

Solution:

a)

$$\frac{V_o}{V_i} = \frac{\frac{(Z_3+Z_4)Z_2}{Z_2+Z_3+Z_4}\left(\frac{Z_4}{Z_3+Z_4}\right)}{\frac{(Z_3+Z_4)Z_2}{Z_2+Z_3+Z_4} + Z_1} = \frac{Z_2 \cdot Z_4}{(Z_2+Z_3+Z_4)\cdot Z_1 + (Z_3+Z_4)\cdot Z_2}$$

b)

$$\frac{I_a(s)}{V_i(s)} = \frac{\frac{(Z_3+Z_4)Z_2}{Z_2+Z_3+Z_4}}{\frac{(Z_3+Z_4)Z_2}{Z_2+Z_3+Z_4} + Z_1}\frac{1}{Z_2}$$

$$\frac{I_a(s)}{V_i(s)} = \frac{Z_3+Z_4}{(Z_3+Z_4)Z_2 + Z_1(Z_2+Z_3+Z_4)}$$

ANS:: (a) $\frac{V_o}{V_i} = \frac{Z_2 \cdot Z_4}{(Z_2+Z_3+Z_4)\cdot Z_1 + (Z_3+Z_4)\cdot Z_2}$, (b) $\frac{I_a(s)}{V_i(s)} = \frac{Z_3+Z_4}{(Z_3+Z_4)Z_2 + Z_1(Z_2+Z_3+Z_4)}$

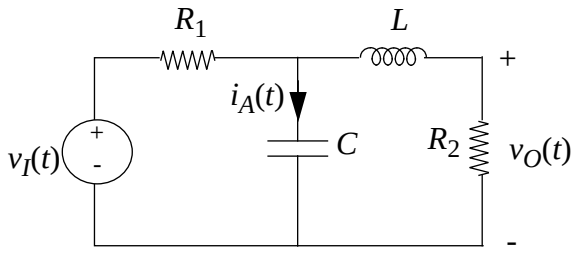


Figure 13.16:

Exercise 13.16 Write the transfer functions $V_o(s)/V_i(s), I_a(s)/V_i(s)$ in the circuit in Figure 13.16.

Solution:

$$e_1 = \frac{Ls + R_2}{LCs^2 + R_2Cs + 1}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{e_1}{R_1 + e_1}\left(\frac{R_2}{R_2 + Ls}\right)$$

$$\frac{I_a(s)}{V_i(s)} = \frac{e_1}{R_1 + e_1} \cdot Cs$$

ANS:: $\frac{V_o(s)}{V_i(s)} = \frac{e_1}{R_1+e_1}\left(\frac{R_2}{R_2+Ls}\right), \frac{I_a(s)}{V_i(s)} = \frac{e_1}{R_1+e_1} \cdot Cs$

Exercise 13.17 Write the transfer function $I_a(s)/I_s(s)$ for the circuit in Figure 13.17.

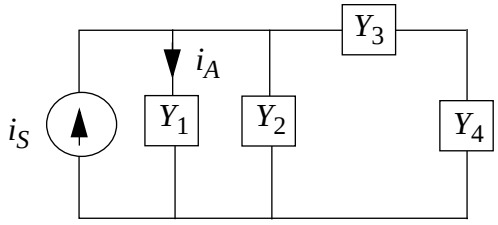


Figure 13.17:

Solution:

$$\frac{(Y_3 + Y_4) \cdot Y_2}{Y_2 + Y_3 + Y_4} = Y_{||}$$

$$\frac{I_a(s)}{I_s(s)} = \frac{Y_{||}}{Y_{||} + Y_1}$$

ANS:: $\frac{I_a(s)}{I_s(s)} = \frac{Y_{||}}{Y_{||}+Y_1}$

Exercise 13.18 Find I_a/I_s in the circuit in Figure 13.18.

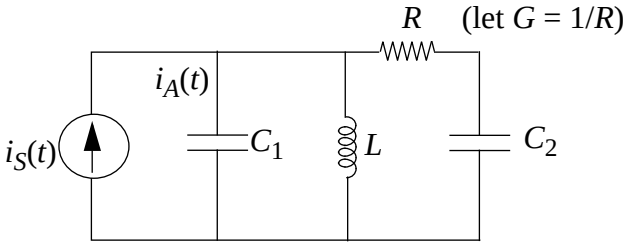


Figure 13.18:

Solution:

$$Z_{||} = \frac{(RC_2 s + 1) \cdot Ls}{LC_2 s^2 + RC_2 s + 1}$$

$$\frac{I_a}{I_s} = \frac{Z_{||}}{Z_{||} + \frac{1}{C_1 s}} = \frac{C_1 s Z_{||}}{C_1 s Z_{||} + 1}$$

ANS:: $\frac{I_a}{I_s} = \frac{C_1 s Z_{||}}{C_1 s Z_{||}+1}$

Problems

Problem 13.1 For each of the networks shown in Figure 13.19:

a) Determine an expression for the indicated complex impedance or transfer function.

b) Sketch the magnitude and angle of the indicated quantity as a function of frequency. You may use either linear or log-log coordinates, but it is recommended that you learn to use both kinds of axes.

Solution:

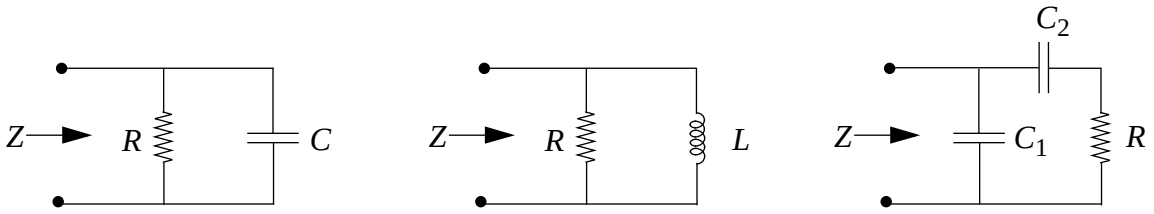


Figure 13.19:

a) i) $Z = \frac{R}{1+j\omega RC}$

ii) $Z = \frac{j\omega RL}{R+j\omega L}$

iii) $Z = \frac{j\omega RC_2+1}{j\omega C_1-\omega^2 C_1 C_2 R+j\omega C_2}$

b) i) See Figure 13.20

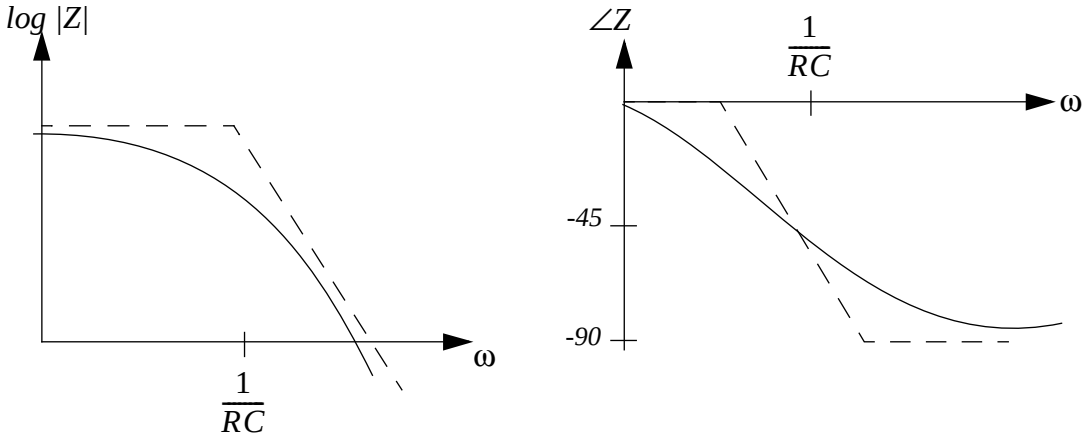


Figure 13.20:

ii) See Figure 13.21

iii) See Figure 13.22

ANS:: (a) (i) $Z = \frac{R}{1+j\omega RC}$ (ii) $Z = \frac{j\omega RL}{R+j\omega L}$ (iii) $Z = \frac{j\omega RC_2+1}{j\omega C_1-\omega^2 C_1 C_2 R+j\omega C_2}$

Problem 13.2 Shown in Figure 13.23 is one possible circuit model for a transformer, for use where there can be a common ground between primary and secondary.

Assume:

$L_1 = 2.5H, L_2 = 0.025H, M = k\sqrt{L_1 L_2}$ where $k < 1, R_1 = 1k\Omega, R_2 = 10\Omega$.

a) Determine an expression for the sinusoidal steady-state transfer function V_2/V_s.

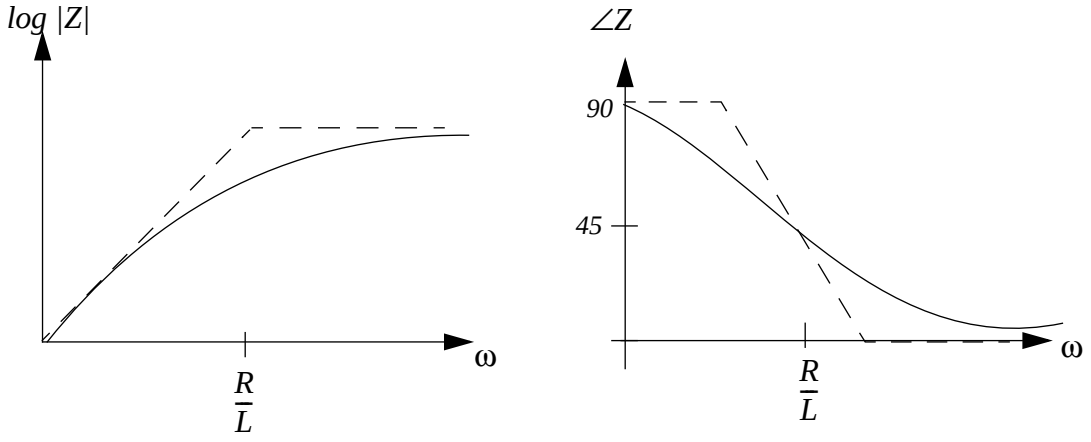


Figure 13.21:

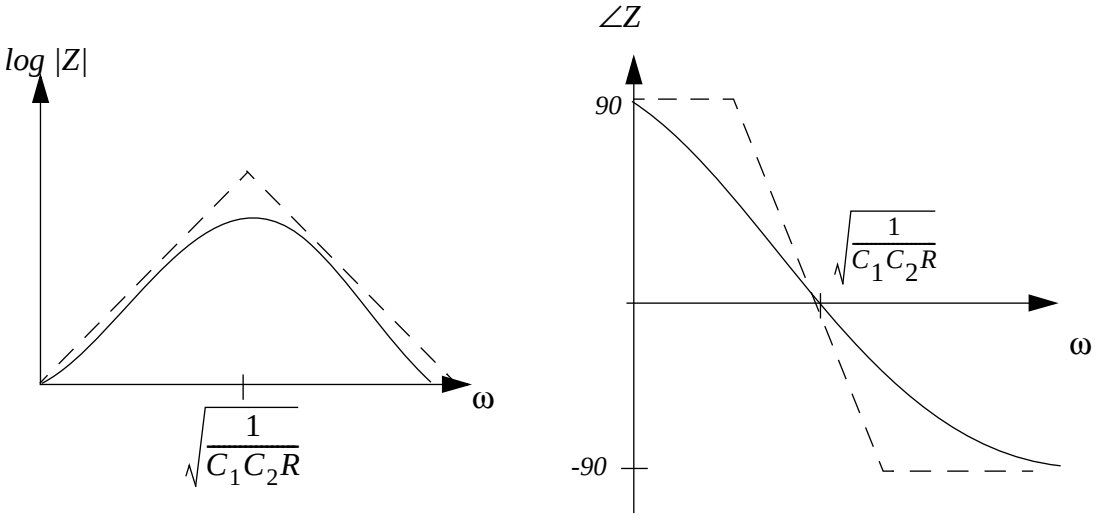


Figure 13.22:

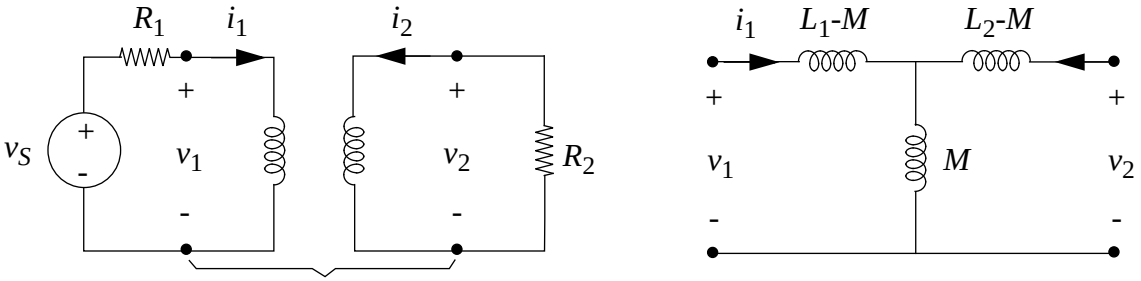


Figure 13.23:

b) In the tight-coupling limit, $k \to 1$, the two natural frequencies are far apart. (See Problem 12.3 in the previous chapter.) For this specific case, sketch the magnitude and angle of the transfer function on log-log scales.

Solution:

a) $\frac{V_2}{V_s} = \frac{j\omega M}{R_1 R_2 + \omega^2(M^2 - L_1 L_2) + j\omega(R_1 L_2 + R_2 L_1)}$

b) See figures on the following pages.

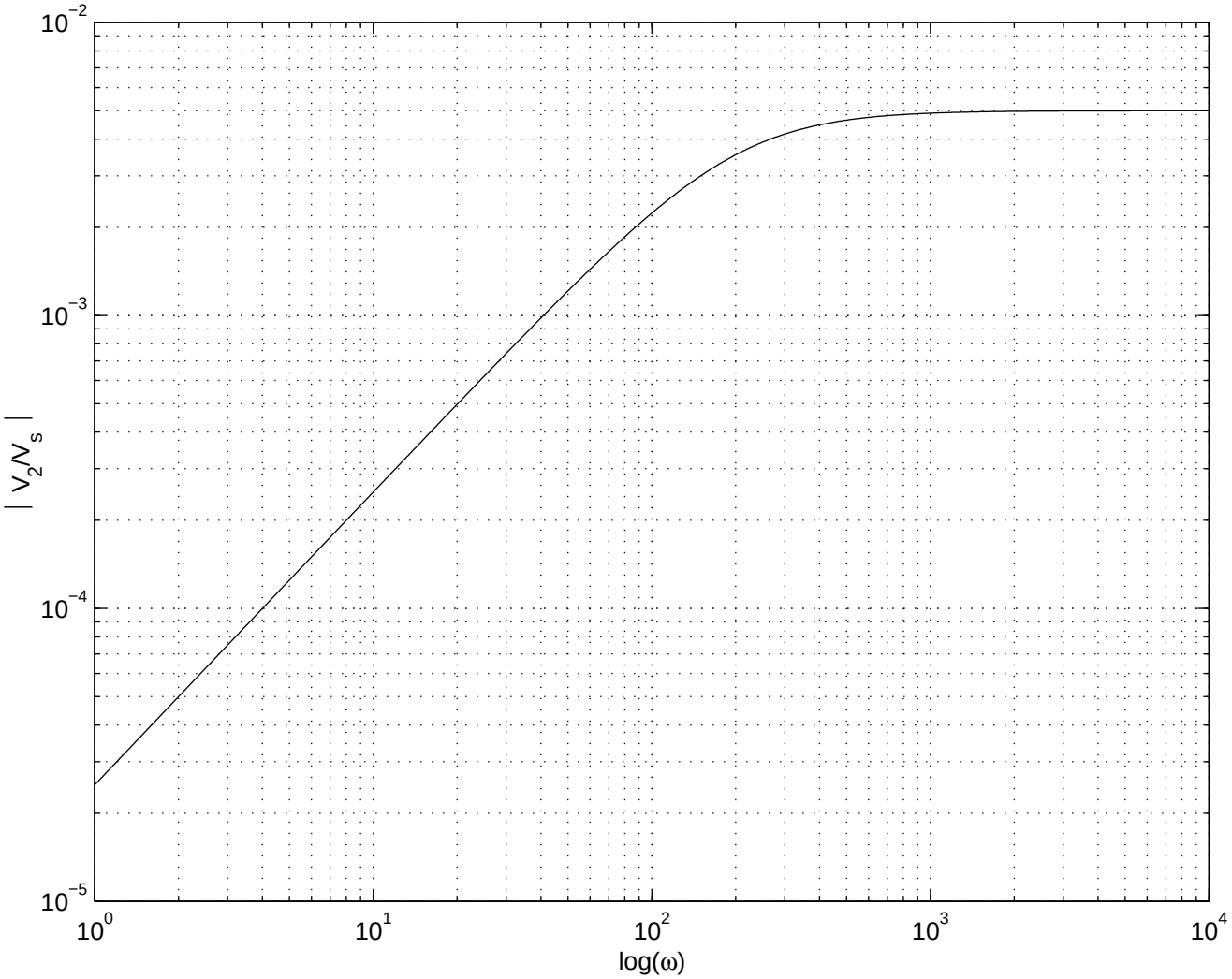


Figure 13.24:

ANS:: (a) $\frac{V_2}{V_s} = \frac{j\omega M}{R_1 R_2 + \omega^2(M^2 - L_1 L_2) + j\omega(R_1 L_2 + R_2 L_1)}$

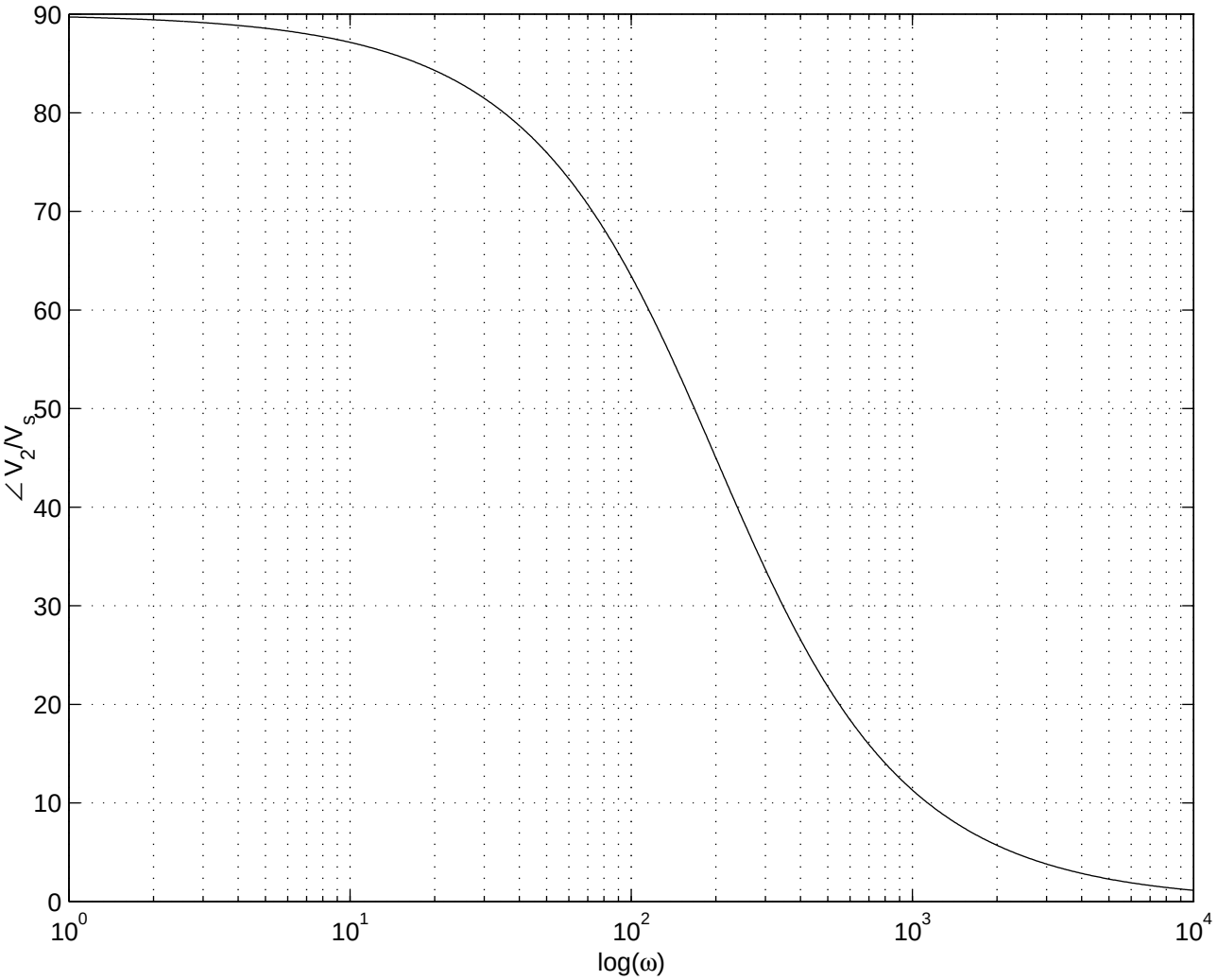


Figure 13.25:

Problem 13.3 An electrical system has the transfer function

$$H(j\omega) = \frac{Y(j\omega)}{X(j\omega)} = \frac{10^5(10 + j\omega)(1000 + j\omega)}{(1 + j\omega)(100 + j\omega)(10000 + j\omega)} \tag{13.1}$$

a) Plot the magnitude of $H(j\omega)$ in decibels versus the logarithm of frequency, labeling all $3dB$ points.

b) Sketch the phase of $H(j\omega)$ versus the logarithm of frequency.

c) For what values of ω does the magnitude of $H(j\omega)$ equal Odb? What is the relationship between the magnitudes of $X(j\omega)$ and $Y(j\omega)$ at these frequencies?

d) List the frequencies at which the phase of $H(j\omega)$ equals 45 degrees.

Solution:

a) See Figure 13.26.

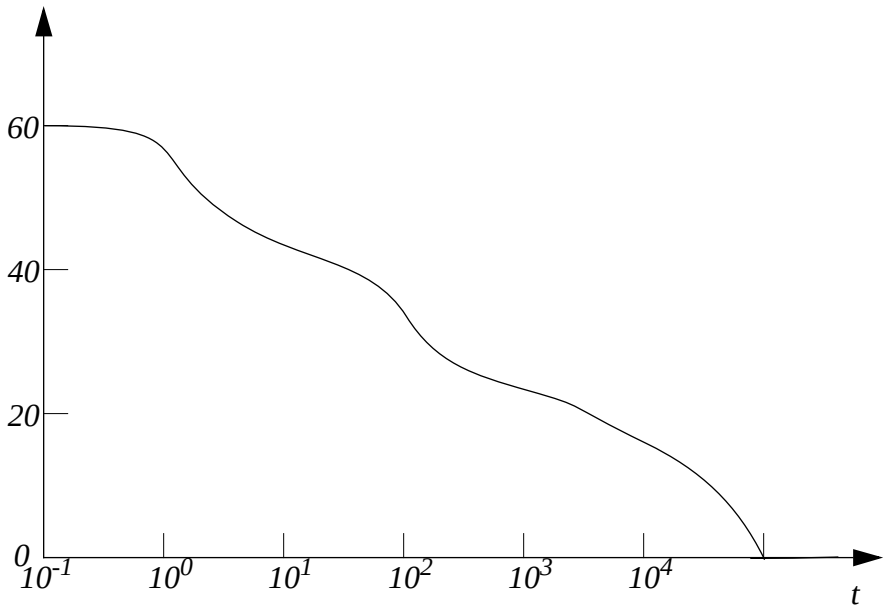


Figure 13.26:

b) See Figure 13.27.

c) The magnitude of $H(j\omega)$ equals $0db$ at $\omega = 10^5$. Here, $\frac{X(j\omega)}{Y(j\omega)} = \frac{1}{2}$.

d) 1; 10; 100; 1,000; 10,000

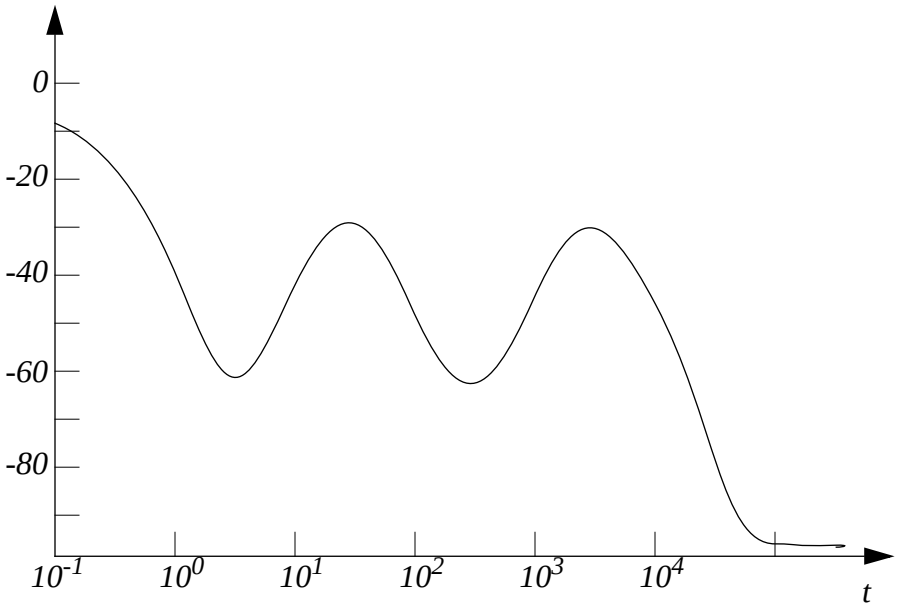


Figure 13.27:

ANS:: (c) $H(j\omega) = 0db$ at $\omega = 10^5$ (d) $1; 10; 100; 1,000; 10,000$

Problem 13.4 Refer to Figure 13.28 for this problem. Assume $R_1 = 1k\Omega$ and $L_1 = 10mH$.

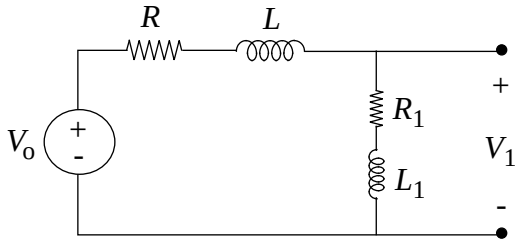


Figure 13.28:

a) Find the transfer function $H(j\omega) = V_1/V_o$.

b) Find R so that the DC gain is $1/10$.

c) Find a value of L so that the response at high frequencies is equal to response at DC.

d) Plot $H(j\omega)$ (magnitude and phase) vs. log ω for the values of R and L found above.

Solution:

a) $H(j\omega) = \frac{R_1 + j\omega L_s}{(R_1+R)+j\omega(L_1+L)}$

b) $R = 9k\Omega$

c) $L = 90mH$

d) See figure.

ANS:: (a) $H(j\omega) = \frac{R_1 + j\omega L_s}{(R_1+R)+j\omega(L_1+L)}$ (b) $R = 9k\Omega$ (c) $L = 90mH$

Problem 13.5 This problem examines the simple door-bell circuit commonly used in homes (Figure 13.29).

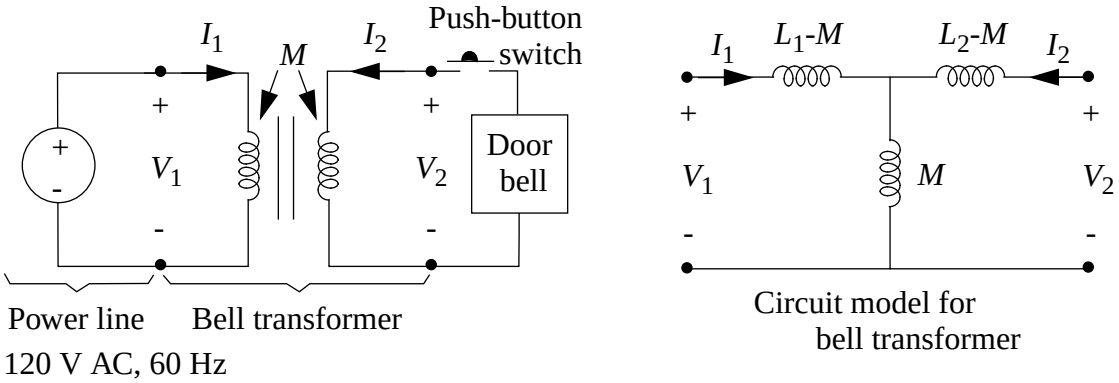


Figure 13.29:

Data for the transformer in Figure 13.29 is given below:
$L_1 = 2.5H, L_2 = .025H, M = k\sqrt{L_1 L_2}$, where $k < 1$.

a) In the limit $k \simeq 1$, what is the voltage V_2 with the push-button switch not pressed (open)? You should use root-mean-square amplitudes for all quantities. The voltage source is given as $120V$ root-mean-square.

b) The door bell operates by repetitive making and breaking of a contact and can normally be modeled as a 10Ω resistance at $60Hz$. Determine the magnitude of the root-mean-square primary current I_1 under normal door bell operation (push button closed, door bell = 10Ω) in the limit of $k \simeq 1$.

c) An important safety issue in such circuits is the prevention of fire in the event that the door bell should accidently stick with its contact closed, thus becoming equal to a short circuit. This can be accomplished by adjusting the value of k. Find the value of k that will limit the root-mean-square primary current to $500mA$ for the case where the push button is pressed and the door bell acts like a short circuit.

Solution:

a) M is approximately 0.25.

$$V_1 = V_{L_1-M} + V_M = (L_1 - M)\frac{di}{dt} + M\frac{di}{dt}$$

$$\frac{di}{dt} = \frac{V_1}{L_1}$$

$$V_2 = M\frac{di}{dt} = \frac{MV_1}{L_1} = \frac{30}{2.5} = 12$$

b) See Figure 13.30.

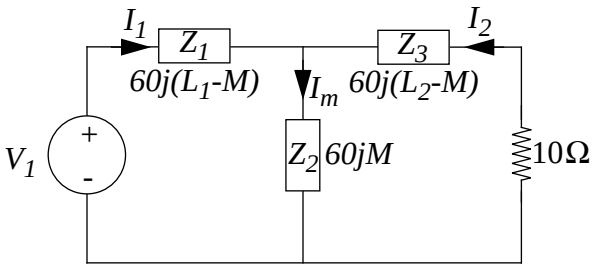


Figure 13.30:

$$Z = \frac{(60jL_2 - 60jM + 10)60jM}{60jL_2 + 10} + 60j(L_1 - M)$$

$$= \frac{3600M^2 - 3600L_1L_2 + 600jL_1}{60jL_2 + 10} = \frac{600jL_1}{60jL_2 + 10}$$

$$I = \frac{60jL_2 + 10)V_1}{600jL_1} = \frac{\sqrt{100 + 3600 * (0.025^2)}|V_1|}{600 * L_1} = \frac{\sqrt{409}}{25}$$

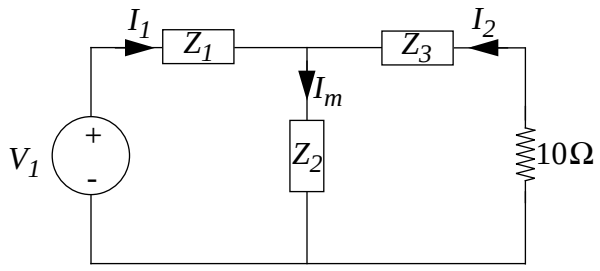


Figure 13.31:

c) See Figure 13.31.

$$Z = \frac{(60jL_2 - 60jM)60jM}{600jL_2} + 60jL_1 - 60jM$$

$$= \frac{60k^2L_1 - 60L_1}{j} = -60L_1j(k^2 - 1)$$

Therefore we have $\frac{V_1}{60L_1(k^2-1)} = 0.5$, and $\frac{120}{75} = k^2 - 1$. Finally, $k = \sqrt{\frac{13}{5}}$.

ANS:: (a) 12 (b) $I = \frac{\sqrt{409}}{25}$ (c) $k = \sqrt{\frac{13}{5}}$

Problem 13.6 In the circuit in Figure 13.32, the switch has been in Position (1) for a long time. At $t = 0$, the switch is moved instantly to Position (2). For the particular parameter values of this circuit, the complete output waveform for *all* time greater than zero is

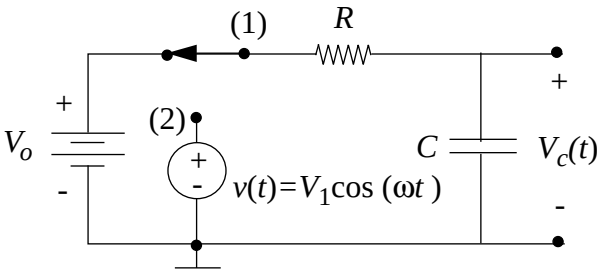


Figure 13.32:

$$v_c(t) = |V_c| \cos(\omega t + \Phi) \tag{13.2}$$

a) Find $|V_c|$ and Φ in terms of $V_1, \omega, R,$ and C.

b) Find V_o in terms of $|V_c|, \omega, R$ and C required to produce the $v_c(t)$ waveform.

Solution:

a) $|V_c| = \frac{V_1}{\sqrt{1+(\omega RC)^2}}$

$\Phi = -\arctan(\omega RC)$

b) $V_o = \frac{V_1}{1+(\omega RC)^2}$

ANS:: (a) $|V_c| = \frac{V_1}{\sqrt{1+(\omega RC)^2}}$, $\Phi = -\arctan(\omega RC)$ (b) $V_o = \frac{V_1}{1+(\omega RC)^2}$

Chapter 14

SSS: Resonance

Exercises

Exercise 14.1

a) For the circuit in Figure 14.1, assume a sinusoidal steady state at a fixed frequency ω_0. Determine an equivalent circuit for the $R-L$ parallel combination (Z_1) in terms of a resistor R' in series with a suitable inductance L'.

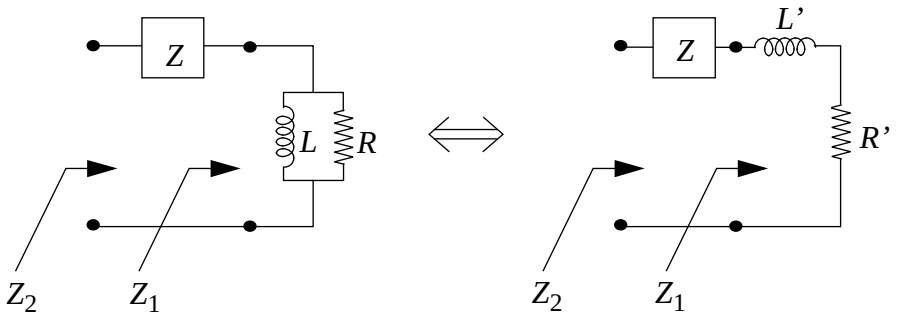


Figure 14.1:

b) Determine the impedance Z that must be added in series with Z_1 such that the total impedance Z_2 is equivalent to a pure resistance at frequency ω_0. What is this value of this resistance?

Solution:

a)

$$Z + \frac{LsR}{Ls + R} = Z + L' + R'$$

$\omega = \omega_o$:

$$\frac{LR\omega_o j}{L\omega_o j + R} = L' j\omega_o + R' = \frac{L^2 R{\omega_o}^2 + R^2 L\omega_o j}{(L\omega_o)^2 + R^2}$$

Equating real and imaginary parts above,

$$L' = \frac{R^2 L}{(L\omega_o)^2 + R^2}$$

$$R' = \frac{{\omega_o}^2 L^2 R}{(L\omega_o)^2 + R^2}$$

b) Add the capacitor in series with

$$C = \frac{R^2 + (\omega_o L)^2}{R^2 {\omega_o}^2 L}$$

ANS:: (a) $L' = \frac{R^2 L}{(L\omega_o)^2+R^2}$, $R' = \frac{{\omega_o}^2 L^2 R}{(L\omega_o)^2+R^2}$, (b) $C = \frac{R^2+(\omega_o L)^2}{R^2 {\omega_o}^2 L}$

Exercise 14.2 For a parallel RLC network with $R = 1k\Omega, L = 1/12H, C = 1/3\mu F$, find $\omega_0, f_0, \alpha, Q_0, \omega_d, \omega_1, \omega_2$ and $\beta = \omega_2 - \omega_1$. ($\omega_1$ and ω_2 are the half-power frequencies.)

Solution:

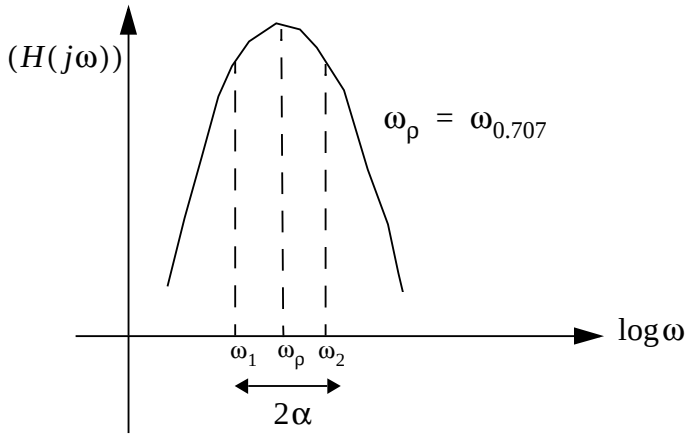


Figure 14.2:

$$\omega_o = \sqrt{\frac{1}{LC}} = 6000 rad/s = 2\pi f_o$$

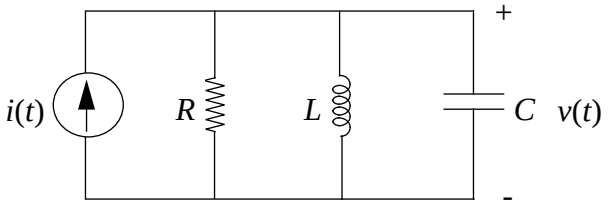


Figure 14.3:

$$f_o = 954.9Hz$$

$$2\alpha = \frac{1}{RC} \quad \rightarrow \quad \alpha = 1500rad/s$$

$$Q_o = \frac{\omega_o}{2\alpha} = \omega_o RC = 2$$

$${\omega_d}^2 = {\omega_o}^2 - \alpha^2$$

$$\omega_d = 5,809rad/s$$

$$\omega_1 = -\omega_P - \alpha = 4684rad/s$$

$$\omega_2 = \omega_P + \alpha = 7684rad/s$$

$$\beta = 3000rad/s$$

$$\omega_P = \omega_o \cdot \sqrt{1 + \frac{1}{4Q^2}} = 6,184rad/s$$

ANS:: $f_o = 0.95kHz, \omega_d = 5.8k$rad/sec, $\omega_2 = 7.89k$rad/sec, $\alpha = 1.5$rad/sec, $\omega_1 = 4.68k$rad/sec, $\beta = 3k$rad/sec, $Q_o = 2$

Exercise 14.3 A parallel resonant RLC circuit (Figure 14.3) driven by a current source, 0.2 cos ωt, (units of amperes) shows a maximum voltage response amplitude of $80V$ at $\omega = 2500$ rad/sec. and $40V$ at 2200 rad/sec. Find R, L, and C.

Solution:

For this circuit,

$$V = I \cdot H(j\omega)$$

$I_o = 0.2Amps$

Peak response occurs at

$$\omega_o = \left(\frac{1}{LC}\right)^{1/2}$$

and at this ω,

$$|V| = I_o \cdot R = 80V$$

$|H(j\omega_o)| \quad \rightarrow \quad R$

Therefore, $R = 400\Omega$

$$|V|_{\omega=2200} = 40V = \left|\frac{I_o \frac{s}{C}}{s^2 + \frac{s}{RC} + \frac{1}{LC}}\right| = \left|\frac{440j/C}{{\omega_o}^2 - \omega^2 + \frac{2200j}{400C}}\right| = \frac{440j/C}{1.41 \times 10^6 + \frac{5.5j}{C}}$$

$$C = 6.756\mu F$$

$${\omega_o}^2 = \frac{1}{LC} = (2500)^2$$

$$L = 23.7mh$$

ANS:: $R = 400\Omega, L = 23.7mH, C = 6.76\mu F$

Exercise 14.4 Find an expression for the value of L that will balance the bridge (Figure 14.4) to make $v_1 - v_2 = 0$, for an input voltage $V\cos\,\omega t$.

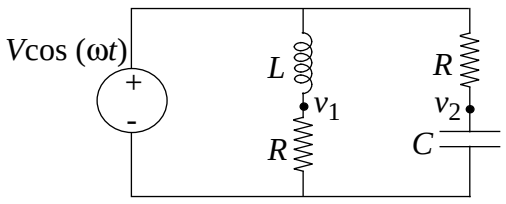


Figure 14.4:

Solution:

We need to meet the following condition:

$$\frac{Ls}{R} = \frac{R}{\frac{1}{Cs}}$$

$$L = R^2 \cdot C$$

ANS:: $L = R^2C$

Exercise 14.5 One or two of the following statements made about the second-order RLC network in Figure 14.5 is/are inconsistent with the rest. Circle the inconsistent statement(s).

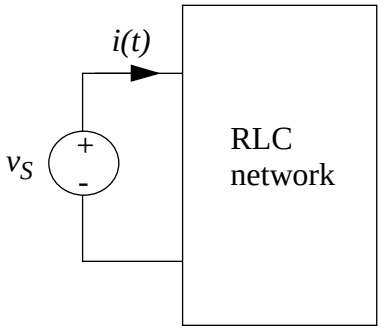


Figure 14.5:

a) The natural frequencies s_1 and s_2 of this circuit are as shown in the complex plane (see Figure 14.6).

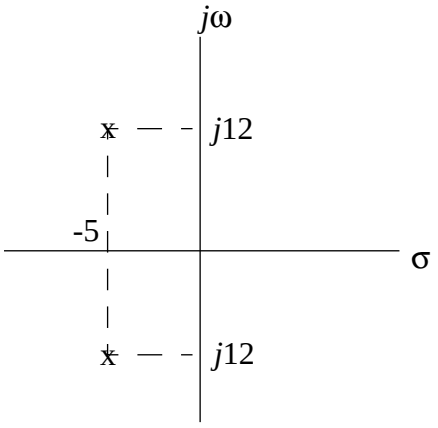


Figure 14.6:

b) $Q = 1.2$

c) The admittance function $Y(j\omega) = I(j\omega)/V_s(j\omega) = j2\omega/[(169 - \omega^2) + j10\omega]$

d) The step response for $t > 0$ is of the form:

$$i(t) = Ae^{-5t}\cos(12t + \phi) \tag{14.1}$$

e) The steady state response to $v_s(t) = B\cos\ 25t$ is of the form:

$$i(t) = C\ \cos\ (25t + \Phi) \tag{14.2}$$

Solution:

(b) is inconsistent with the other statements.

$Q = 1.3$ actually.

$$\omega_o{}^2 = \alpha^2 + \omega_d{}^2 \quad \rightarrow \quad s_{1,2} = -\alpha \pm \omega_d j$$

$$Q = \frac{\omega_o}{2\alpha} = \frac{13}{2(5)} = 1.3$$

ANS:: (b) is inconsistent with the other statements, $Q = 1.3$ actually

Exercise 14.6 Consider the network shown in Figure 14.7.

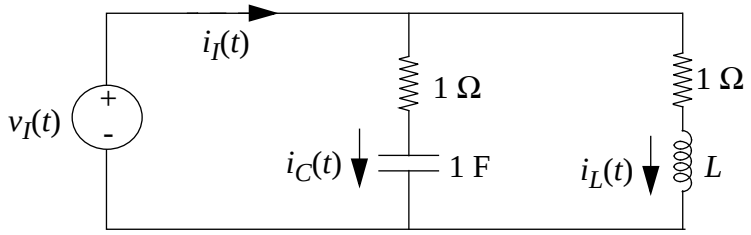


Figure 14.7:

a) Show that by proper choice of the value of L, the impedance $\frac{V_i(s)}{I_i(s)} = Z_i(s)$ can be made independent of s. What value of L satisfies this condition?

b) With L as determined in part a), what is the value of Z_i?

c) Assume that the capacitor voltage and the inductor current are both zero for $t < 0$. Determine $i_C(t)$ for $t > 0$ when $v_I(t)$ is a unit step.

Solution:

a)

$$Z_i = \frac{(R+\frac{1}{Cs})(R+Ls)}{R+\frac{1}{Cs}+R+Ls} = \frac{(RCs+1)(R+Ls)\cdot Cs}{Cs(2RCs+1+LCs^2)}$$

$$Z_i(s) = \frac{R\left(LCs^2+\left(\frac{R^2C+L}{R}\right)s+1\right)}{LCs^2+2RCs+1}$$

We need $\frac{R^2C+L}{R} = 2RC$ for $Z_i(s)$ to be independent of s.

Choose $L = R^2C$ to accomplish this.

$L = 1$ if $R = C = 1$.

b) $Z_i = R$

c) $i_C(t) = \frac{1}{R}\, e^{-t/RC}$

ANS:: (a) $L = 1$ if $R = C = 1$, (b) $Z_i = R$, (c) $i_C(t) = \frac{1}{R}\, e^{-t/RC}$

Exercise 14.7 Each of the following parts makes a statement about a second-order system. Indicate whether the statement is true or false.

a) The network shown in Figure 14.8 (with both R's and C's positive) can exhibit natural responses of the form $e^{-\alpha t}\sin\,\omega t$.

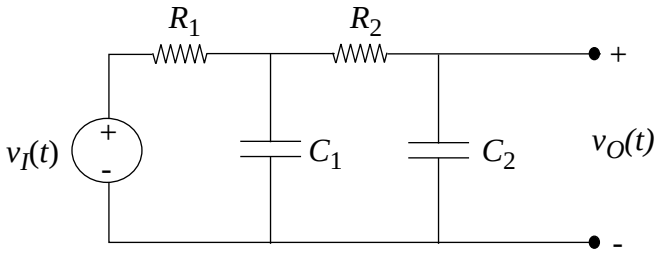


Figure 14.8:

b) The natural response of a RLC network is given by: $v_O(t) = 25e^{-5t}cos(12t+\pi/7)$.

The Q of the network is 1.2.

c) For the circuit shown in Figure 14.9, the output voltage under sinusoidal steady state conditions is zero.

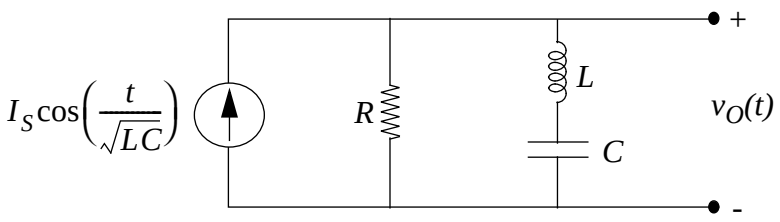


Figure 14.9:

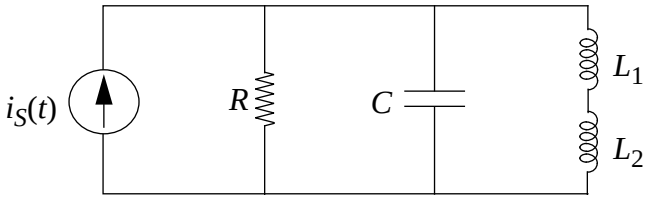


Figure 14.10:

d) The circuit shown in Figure 14.10 contains 3 energy storage elements and thus has 3 natural frequencies.

Solution:

a) False. The roots are purely real and negative from the characteristic equation.

b) False.

$\omega_d = 12$ and $\alpha = 5$

So, $\omega_o = \sqrt{{\omega_d}^2 + \alpha^2} = 13$

$Q = \frac{\omega_o}{2\alpha} = 1.3 \neq 1.2$

c) True.

$$H(s) = \frac{V_s}{I_s} = \frac{R(LCs^2 + 1)}{LCs^2 + RCs + 1}$$

So at

$$s = \frac{j}{\sqrt{LC}},$$

$$|H(j\omega)| = 0$$

d) False. L_1 and L_2 are in series, so their combination is equivalent to one inductor of value $L_1 + L_2$.

Thus the system is second order and cannot have 3 natural frequencies.

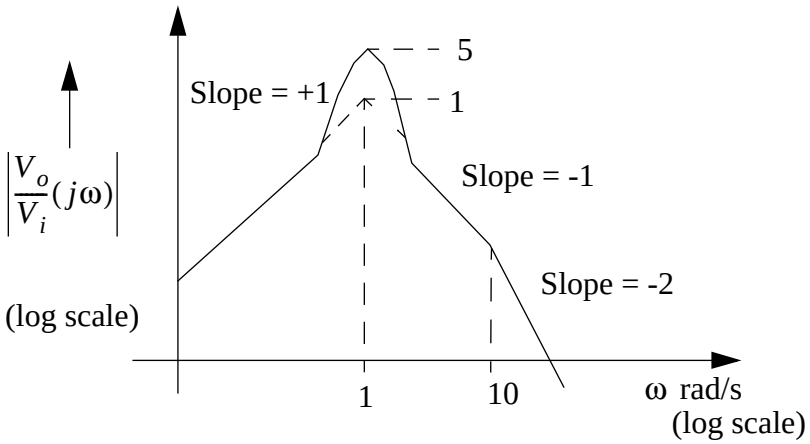


Figure 14.11:

ANS:: (a) False (roots are real and negative), (b) False (Q = 1.3), (c) True (at $s = \frac{j}{\sqrt{LC}}, |H(j\omega)| = 0$), (d) False. (system is second order)

Exercise 14.8 The voltage transfer ratio of a certain network is shown in Figure 14.11 in Bode-plot form.

This transfer ratio can be expressed in the form

$$\frac{V_o(s)}{V_i(s)} = \frac{Ks}{(s^2 + s\omega_0/Q + \omega_0^2)(\tau s + 1)} \tag{14.3}$$

Determine the parameters K, Q, ω_0, and τ.

Solution:

$\omega_o = 1rad/s$; it is the resonant peak frequency.

The pole at $\omega = 10$ is due to $(\tau s + 1)$ factor in the denominator.

At $\omega = 10$, $\omega\tau = 1$ so that $|\tau s + 1| = \sqrt{2}$.

$\tau = 1/10$

Q is the ratio of the resonant peak to the asymptotic intersection, $Q = 5$.

$$|H(j \cdot 1)| = 5 = \frac{K\omega}{\sqrt{(\omega_o{}^2 - \omega^2)^2 + (\frac{\omega\omega_o}{Q})^2} \cdot \sqrt{1 + (\tau\omega)^2}}$$

$$K = 1.005$$

ANS:: $K = 1.005, Q = 5, \omega_o = 1rad/s, \tau = 1/10$

Exercise 14.9

a) In the circuit in Figure 14.12, find an expression for the complex amplitude V_o as a function of V_i after transients have died out, assuming v_i is a sinusoid: $v_i = V_i \cos \omega t$.

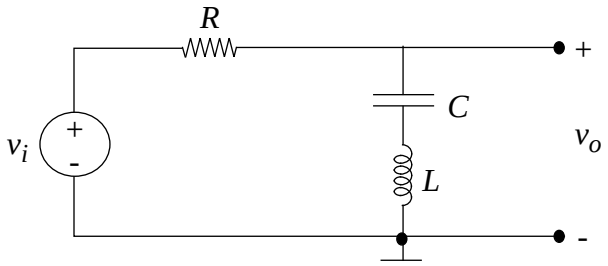


Figure 14.12:

b) Find $v_o(t)$ at the frequency $\omega_0 = \frac{1}{\sqrt{LC}}$.

Solution:

a)

$$V_o(s) = \frac{1 + LCs^2}{1 + RCs + LCs^2} \cdot V_i(s)$$

b) At $\omega_o = \frac{1}{\sqrt{LC}}$, $v_o(t) = 0$.

ANS:: (a) $V_o(s) = \frac{1+LCs^2}{1+RCs+LCs^2} V_i(s)$, (b) $v_o(t) = 0$

Exercise 14.10 The impedance of the network shown in Figure 14.13 is found to be $2k\Omega$ and is purely real at all frequencies. The value of the inductor is one mH as shown. What are the values of R and C?

Solution:

$$Z = \frac{(R + \frac{1}{Cs})(R + Ls)}{2R + \frac{1}{Cs} + Ls} = \frac{R(LCs^2 + (\frac{L}{R} + RC)s + 1)}{LCs^2 + 2RCs + 1}$$

In order for Z to always be purely real,

$$\left(\frac{L}{R} + RC\right) = 2RC$$

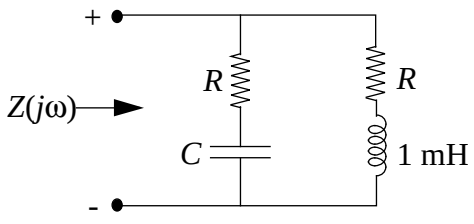


Figure 14.13:

$$L = R^2 C$$

Then

$$Z = R = 2000$$

independent of ω.

$$.001 = 2000^2\ C$$

$$C = 2.5 \cdot 10^{-10} Farads$$

ANS:: $R = 2000$ and $C = 2.5 \cdot 10^{-10}$ Farads

Problems

Problem 14.1 For the series-resonant circuit in Figure 14.14, draw the impedance model, and find the transfer function V_o/V_i. Sketch the Bode plot of log magnitude and phase of this function versus log frequency by sketching the asymptotes, then sketching the function. This is a second-order low-pass filter.

For this topology, the maximum amplitude does not occur at the resonant frequency ω_0 (prove this, but don't work out all the math). However, this is a small effect for all but very low Q. Find expressions for the resonant frequency (defined as the frequency where the s^2 and the s^0 terms cancel in the denominator) and the Q.

Solution:

Impedance Model (Figure 14.15):

Transfer Function:

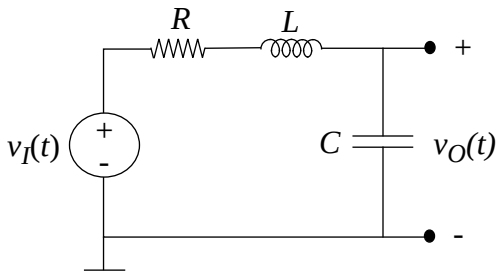


Figure 14.14:

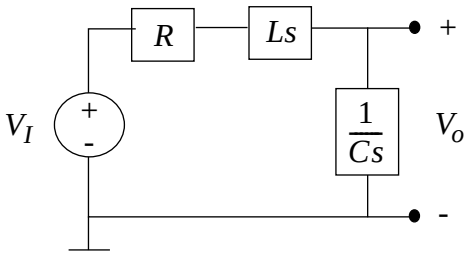


Figure 14.15:

$$\frac{V_O}{V_I} = \frac{\frac{1}{Cs}}{Ls + R + \frac{1}{Cs}} = \frac{1}{LCs^2 + RCs + 1} = \frac{1}{(1 - \omega^2 LC) + j\omega RC}$$

Bode Plot:

$$\varphi = -\tan^{-1}(\frac{\omega RC}{1 - \omega^2 LC})$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

See Figure 14.16 for plot.

Resonant Frequency:

$$\omega_O = \frac{1}{\sqrt{LC}}$$

Check if max amplitude occurs at ω_0:

$$\frac{\partial}{\partial \omega}\left(\frac{V_O}{V_I}\right) = \frac{-jRC + 2\omega LC}{[(1 - \omega^2 LC) + j\omega RC]^2}$$

at ω_0:

$$\frac{\partial}{\partial \omega}\left(\frac{V_O}{V_I}\right)\Big|_{\omega_O} = \frac{-jRC + 2\sqrt{LC}}{[jR\sqrt{\frac{C}{L}}]^2} \neq 0$$

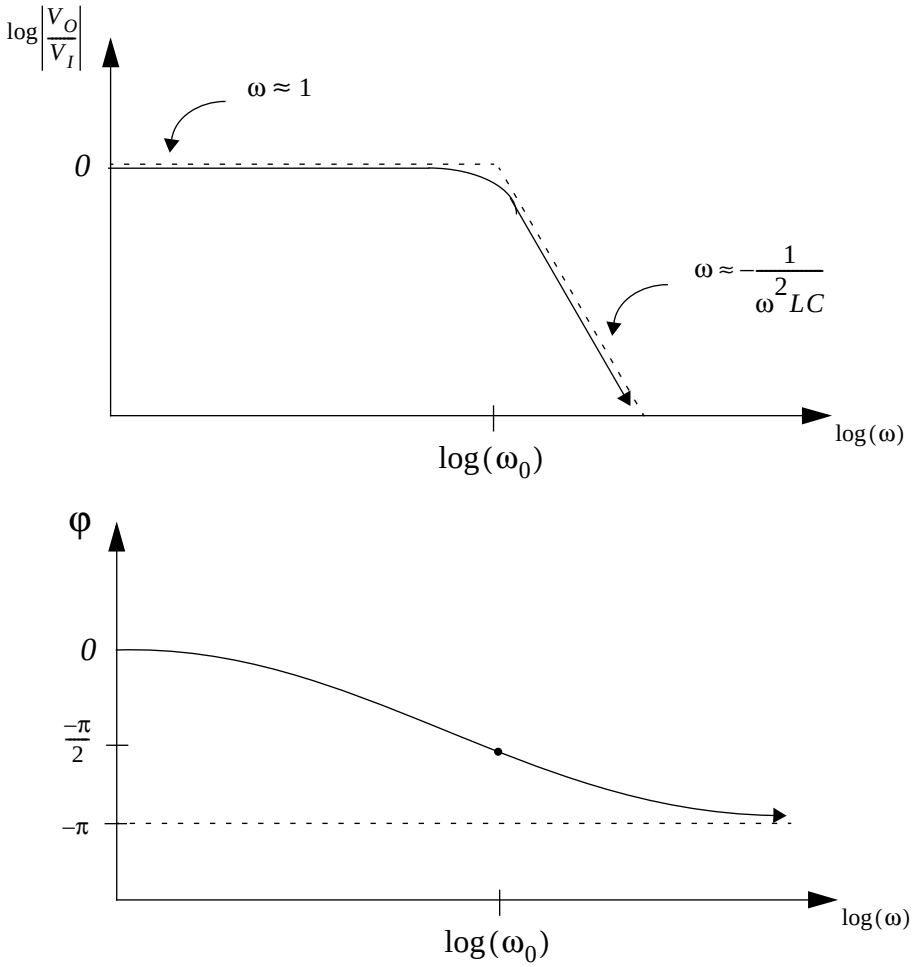


Figure 14.16:

So, ω_0 not maximum amplitude.

$$Q = \frac{\omega L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

ANS:: $\frac{V_O}{V_I} = \frac{1}{(1-\omega^2 LC)+j\omega RC}$, $\omega_0 = \frac{1}{\sqrt{LC}}$, $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$

Problem 14.2 Consider the circuit in Figure 14.17.

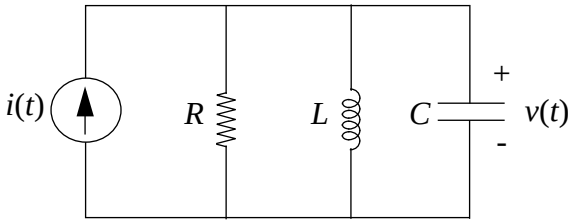


Figure 14.17:

a) Draw the Bode plot of $|Z(w)|$ for $R = L = C = 1$. What is the resonant frequency?

b) Draw the Bode plot of $|Z(w)|$ for $R = 1, L = C = 2$. What is the resonant frequency?

c) Comment on the results of part a) and part b).

Solution:

Find $|Z(\omega)|$:

$$Z(\omega) = \frac{1}{Cs + \frac{1}{R} + \frac{1}{Ls}} = \frac{RLs}{RLCs^2 + Ls + R} = \frac{j\omega RL}{R(1-\omega^2 LC) + j\omega L}$$

$$|Z(\omega)| = \frac{\omega RC}{\sqrt{R^2(1-\omega^2 LC)^2 + \omega^2 L^2}}$$

a) $R = 1, L = 1, C = 1$

$$|Z(\omega)| = \frac{\omega}{\sqrt{(1-\omega^2)^2 + \omega^2}}$$

$$\omega_0 = 1$$

Bode Plot: see Figure 14.18

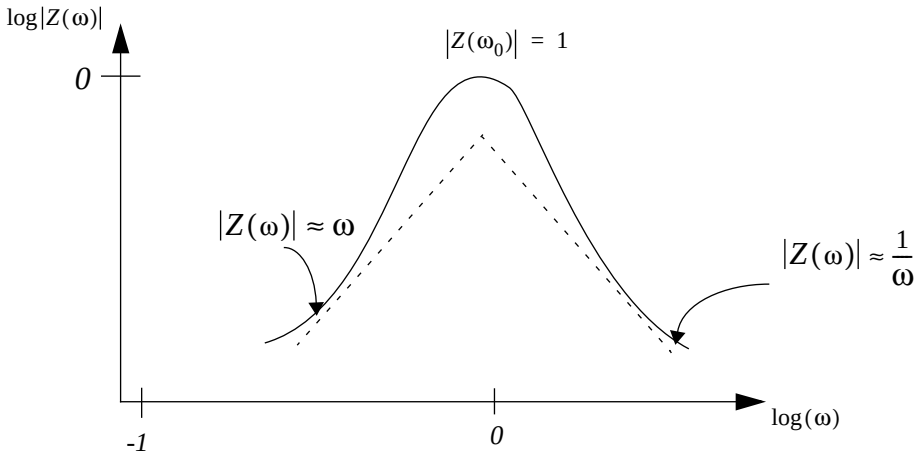


Figure 14.18:

b) $R = 1, L = 2, C = 2$

$$|Z(\omega)| = \frac{2\omega}{\sqrt{(1-4\omega^2)^2 + 4\omega^2}}$$

$$\omega_0 = \frac{1}{2}$$

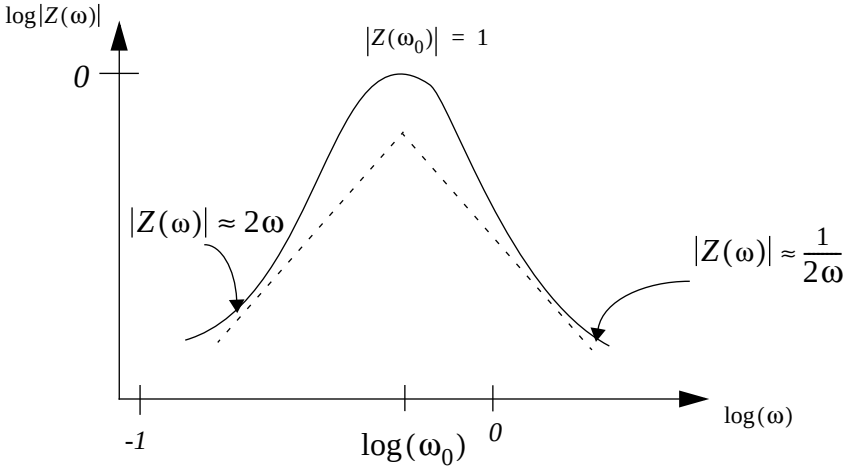


Figure 14.19:

Bode Plot: see Figure 14.19

c) The resonant frequency drops from 1 to $\frac{1}{2}$. As a result, the Bode plot for $|Z(\omega)|$ just shifts to the left by an amount $log(\frac{1}{2})$.

ANS:: (a) $\omega_0 = 1$, (b) $\omega_0 = \frac{1}{2}$

Problem 14.3 The circuit shown in Figure 14.20 has an input voltage $v_{in1}(t) = V_1 \cos 120\pi t$, and $L = 500mH, C = 80\mu f, R = 50\Omega$.

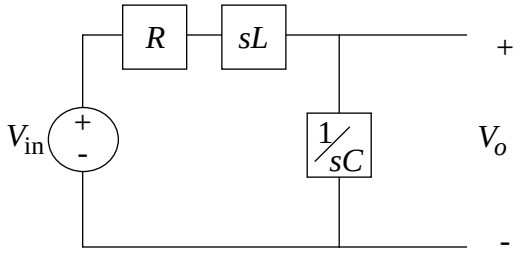


Figure 14.20:

a) Compute the transfer function $H(s) = V_o(s)/V_{in1}(s)$.

b) Set $v_{in1}(t) = 0$. What is the equivalent complex impedance of the circuit evaluated between V_o and ground?

c) Parts a) and b) might lead you to believe that Thévenin's Theorem also applies to complex impedances. If this is true then we can replace the circuit between V_o and ground by a complex Thévenin impedance (Z_{th}) and a complex open circuit voltage (V_{oc}). Taking $v_{in1}(t) = 10cos120\pi t$ compute Z_{th} and V_{oc}.

d) Having represented the circuit by its Thévenin's equivalent we wish to connect it to another circuit having $v_{in2}(t) = 10cos200t$ as shown in Figure 14.21.

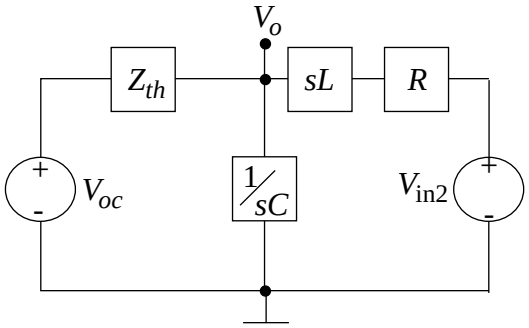


Figure 14.21:

1) Are there any problems with this approach? If so state them explicitly.

2) Compute the complex V_o for this circuit.

3) Now let $v_{in1} = v_{in2} = 10cos120\pi t$. Evaluate V_o for this case.

4) If $v_{in1}(t) = v_{in2}(t) = 10cos120\pi t$ compute the real output voltage $v_o(t)$.

Solution:

a)

$$H(s) = \frac{1}{LCs^2 + RCs + 1} = \frac{1}{(1 - \omega^2 LC) + j\omega RC}$$

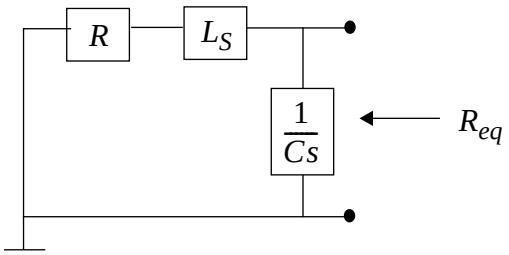


Figure 14.22:

b) See Figure 14.22

$$Z_{eq} = \frac{1}{\frac{1}{R+sL} + Cs} = \frac{R + sL}{LCs^2 + RCs + 1} = \frac{R + j\omega L}{(1 - \omega^2 LC) + j\omega RC}$$

c) $v_{in1}(t) = 10\cos(120\pi t)$

$$V_{oc} = H(s) \cdot V_{in1} = \frac{1}{(1 - \omega^2 LC) + j\omega RC} 10e^{j(120\pi t)}$$

$$= \frac{10e^{j(120\pi t - \tan^{-1}\frac{\omega RC}{1-\omega^2 LC})}}{\sqrt{(1 - \omega^2 LC)^2 + \omega^2 R^2 C^2}}$$

$$= \frac{10e^{j(120\pi t)}}{4.92e^{j(-0.311)}}$$

$$V_{oc} = 2.03e^{j(120\pi t + 0.311)}$$

$$Z_{th} = \frac{R + j\omega L}{(1 - \omega^2 LC) = j\omega RC}$$

for $\omega = 120\pi$:

$$Z_{th} = \frac{195e^{j(1.311)}}{4.92e^{j(-0.311)}} = 39.6e^{j(1.622)}$$

ANS:: (a) $\frac{1}{(1-\omega^2 LC)+j\omega RC}$ (b) $Z_{eq} = \frac{R+j\omega L}{(1-\omega^2 LC)+j\omega RC}$ (c) $V_{oc} = 2.03e^{j(120\pi t+0.311)}$, $Z_{th} = 39.6e^{j(1.622)}$

Problem 14.4

a) Determine $\omega_o, \alpha, \omega_d, Q_1$ for each of the circuits in Figure 14.23 ($Q_1 = \omega_o/2\alpha$).

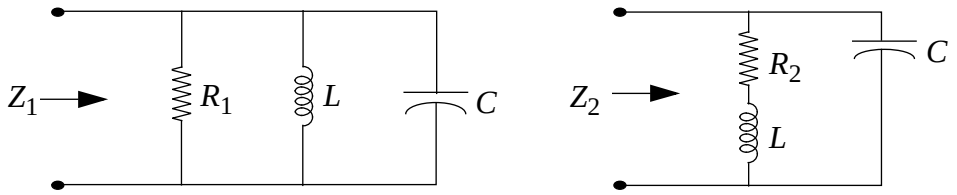


Figure 14.23:

b) Assume $L = 1mH, C = 10\mu F$. Find values of R_1 and R_2 that will yield $Q_1 = 10$. What is the ratio of R_1 to R_2?

c) Make a parallel $L' - R'$ equivalent circuit for the $L - R_2$ series combination (as in Exercise 14.1) and use this equivalent circuit to calculate what the ratio of R_1 and R_2 in part b should be for $Q_1 = 10$ in both circuits. How large is the discrepancy, if any?

d) Using the values for R_1 and R_2 found in part b), make plots of $|Z_1|$ and $|Z_2|$ versus frequency and $\angle Z_1$ and $\angle Z_2$ versus frequency. Identify the following features of your plot:

   i) The maximum impedance, the frequency ω_r at which this occurs, and the phase angle at ω_r.

   ii) The frequencies ω_1 and ω_2 at which $|Z|$ is $1/\sqrt{2}$ smaller than the maximum, and the phase angles at ω_1 and ω_2. Calculate the quantity $Q_2 = \omega_r/(\omega_2 - \omega_1)$.

e) Now suppose that you have just been given a "parallel resonant" circuit Z, but you don't know whether it is of the Z_1 form or the Z_2 form. Suggest a step-by-step experimental procedure based on measurements of $|Z|$ and perhaps $\angle Z$ as a function of frequency to determine

   i) which of the two forms of parallel resonant circuit is the best model, and

   ii) specific values for the three elements, R, L, C.

Solution:

a) 1) First circuit:

$$i(t) = CV' + \frac{V}{R} + i_L$$

$$i'(t) = CV'' + \frac{V'}{R} + i_L' = CV'' + \frac{V'}{R} + \frac{V}{L}$$

$$\frac{1}{C}i'(t) = V'' + \frac{V'}{RC} + \frac{V}{LC}$$

General form: $s^2 + 2\alpha s + \omega_0^2 = 0$, so:

$$s^2 + \frac{1}{RC}s + \frac{1}{LC} = 0$$

$$\alpha = \frac{1}{2RC}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$\omega_d = \omega_0^2 - \alpha^2 = \frac{1}{LC} - \frac{1}{4R^2C^2}$$

$$Q_1 = \frac{\omega_0}{2\alpha} = \omega_0 RC = R\sqrt{\frac{C}{L}} = \frac{R}{\omega_0 L}$$

2) Second Circuit:

$$i(t) = CV' + i_L$$

Find V':

$$i_L' = \frac{V - Ri_L}{L}$$

$$V = Li_L' + Ri_L$$

$$V' = Li_L'' + Ri_L'$$

Substitute:

$$i(t) = CLi_L'' + RCi_L' + i_L$$

$$\frac{1}{LC}i(t) = i_L'' + \frac{R}{L}i_L' + \frac{1}{LC}i_L$$

General form: $s^2 + 2\alpha s + \omega_0^2 = 0$, so:

$$\alpha = \frac{R}{2L}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$\omega_d = \frac{1}{LC} - \frac{R^2}{4L^2}$$

$$Q_1 = \frac{\omega_0}{2\alpha} = \frac{\omega_0 L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

b) From part (a), the values of R_1 and R_2 that yield $Q_1 = 10$ are: $R_1 = 100\Omega$ and $R_2 = 1\Omega$. The ratio is then: $\frac{R_1}{R_2} = 100$.

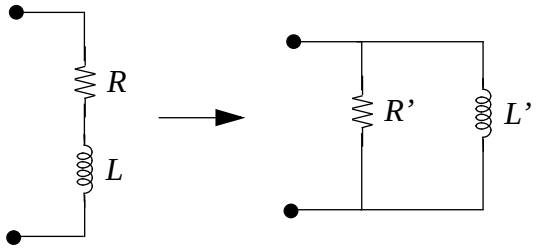


Figure 14.24:

c) See Figure 14.24

$$Z_{th} = R_2 + j\omega L$$

$$Z'_{th} = \frac{1}{\frac{1}{R} + \frac{1}{j\omega L'}} = \frac{j\omega L' R'}{j\omega L' + R'} = \frac{\omega^2 L'^2 R' + j\omega L' R'^2}{\omega^2 L'^2 + R'^2}$$

We want $Z_{th} = Z'_{th}$, so:

$$R_2 = \frac{\omega^2 L'^2 R'}{\omega^2 L'^2 + R'^2}$$

$$L = \frac{L' R'^2}{\omega^2 L'^2 + R'^2}$$

$$\frac{\omega^2 L'}{R'} = \frac{R_2}{L}$$

$$R' = \frac{\omega^2 L' L}{R_2}$$

Substituting:

$$R_2 = \frac{\omega^2 L'^2 (\frac{\omega^2 L' L}{R_2})}{\omega^2 L'^2 + \frac{\omega^4 L'^2 L^2}{R_2^2}} = \frac{R_2 \omega^2 L' L}{R_2^2 + \omega^2 L^2}$$

$$L' = \frac{R_2^2 + \omega^2 L^2}{\omega^2 L}$$

$$R' = \frac{R_2^2 + \omega^2 L^2}{R_2}$$

Find new Q_1:

$$Q_1 = \frac{R'}{\omega_0 L'}$$

$$Q_1 = \frac{\omega^2 L}{\omega_0 R_2} = \frac{\omega_0 L}{R_2}$$

$R_1 = 100\Omega$ and $R_2 = 1\Omega$. The ratio is unchanged at $\frac{R_1}{R_2} = 100$, so there is no discrepancy from part (b).

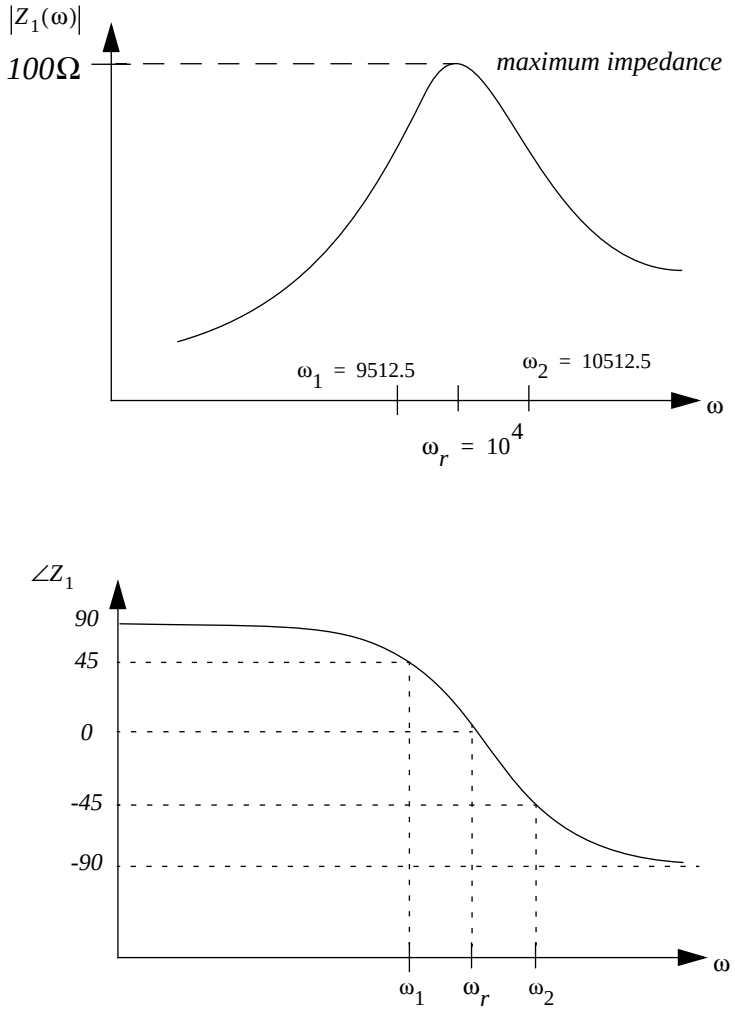


Figure 14.25:

d) See Figure 14.25 for plots.

$$Z_1 = \frac{1}{\frac{1}{R_1} + \frac{1}{j\omega L} + j\omega C}$$

$$Z_1 = \frac{j\omega L R_1}{R_1(1-\omega^2 LC) + j\omega L} = \frac{\omega L R_1 e^{j(\frac{\pi}{2})}}{\sqrt{R_1^2(1-\omega^2 LC)^2 + \omega^2 L^2} e^{j\tan^{-1}(\frac{\omega L}{R_1(1-\omega^2 LC)})}}$$

$$= \frac{\omega L R_1}{\sqrt{R_1^2(1-\omega^2 LC)^2 + \omega^2 L^2}} e^{j\tan^{-1}(\frac{R_1(1-\omega^2 LC)}{\omega L})}$$

$$|Z_1| = \frac{0.1\omega}{\sqrt{10^4(1-10^{-8}\omega^2)^2 + 10^{-6}\omega^2}} = \frac{\omega}{\sqrt{(10^3 - 10^{-5}\omega^2)^2 + 10^{-4}\omega^2}}$$

$$\angle Z_1 = \tan^{-1}\left[\frac{100(1-10^{-8}\omega^2)}{1 \cdot 10^{-3}\omega}\right] = \tan^{-1}\left[\frac{10^5(1-10^{-8}\omega^2)}{\omega}\right]$$

See Figure 14.26 for plots.

$$Z_2 = \frac{1}{\frac{1}{R_2 + j\omega L} + j\omega C} = \frac{R_2 + j\omega L}{(1-\omega^2 LC) + j\omega R_2 C}$$

$$= \frac{\sqrt{R_2^2 + \omega^2 L^2} e^{j\tan^{-1}(\frac{\omega L}{R})}}{\sqrt{(1-\omega^2 LC)^2 + \omega^2 R_2^2 C^2} e^{j\tan^{-1}(\frac{\omega R_2 C}{1-\omega^2 LC})}}$$

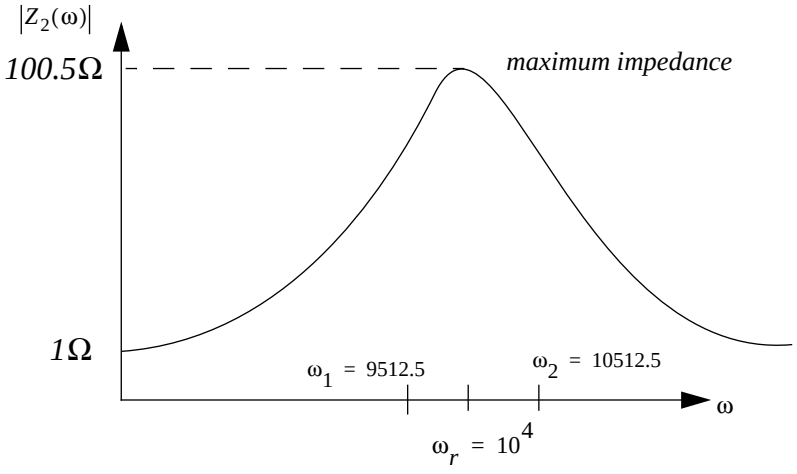
$$|Z_2| = \sqrt{\frac{1 + 10^{-6}\omega^2}{(1-10^{-8}\omega^2)^2 + 10^{-10}\omega^2}}$$

$$\angle Z_2 = \tan^{-1}(10^{-3}\omega) - \tan^{-1}\left(\frac{10^{-5}\omega}{1-10^{-8}\omega^2}\right)$$

e) i) Measure $\angle Z$ close to $\omega = 0$. If $\angle Z \approx 90°$, then Z_1 is the best model, if $\angle Z \approx 0$, then Z_2 is the best model.

ii) Measure $|Z|$ to find ω_0 and Q, then solve the resulting system of equations for R, L, C:
if Z_1: $\omega_0 = \frac{1}{\sqrt{LC}}$, $Q = \frac{R}{\omega_0 L}$, $R = Z_{max}$
if Z_2: $\omega_0 = \frac{1}{\sqrt{LC}}$, $Q = \frac{\omega_0 L}{R}$, $\tan(Q) - 90 = \angle Z(\omega = \omega_0)$

ANS:: (a) (i) $\alpha = \frac{1}{2RC}$, $\omega_0 = \frac{1}{\sqrt{LC}}$, $\omega_d = \frac{1}{LC} - \frac{1}{4R^2C^2}$, $Q_1 = \frac{R}{\omega_0 L}$ (ii) $\alpha = \frac{R}{2L}$, $\omega_0 = \frac{1}{\sqrt{LC}}$, $\omega_d = \frac{1}{LC} - \frac{R^2}{4L^2}$, $Q_1 = \frac{1}{R}\sqrt{\frac{L}{C}}$ (b) $\frac{R_1}{R_2} = 100$ (c) $\frac{R_1}{R_2} = 100$



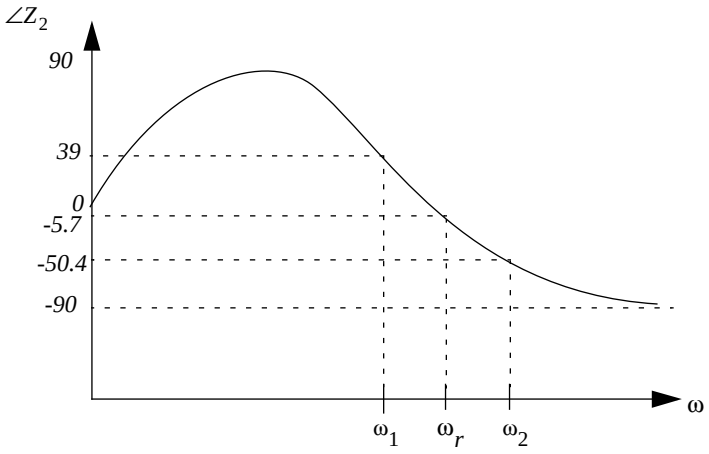


Figure 14.26:

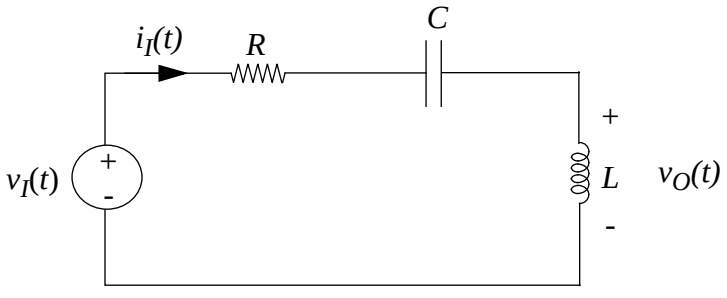


Figure 14.27:

Problem 14.5

a) Write down the differential equation describing the circuit in Figure 14.27.

b) Write the transfer function $V_o(s)/V_i(s)$.

c) Solve for $i_I(t)$ assuming $v_I(t) = cos\omega t$ (let $\omega = 1$).

d) Plot the roots of the characteristic polynomial (from part b) on the complex s-plane (Assume $R^2C^2 < 4CL$.)

Solution:

a)

$$v_I(t) = Ri + \frac{Q}{C} + Li'$$

$$v_I'(t) = Li'' + Ri' + \frac{i}{C}$$

$$\frac{1}{L}v_I'(t) = i'' + \frac{R}{L}i' + \frac{1}{LC}i$$

b) Transfer function:

$$\frac{V_O(s)}{V_I(s)} = \frac{Ls}{R + \frac{1}{Cs} + Ls} = \frac{LCs^2}{LCs^2 + RCs + 1}$$

c) $v_I = \cos\omega t = e^{jt}$, and $\omega = 1$

$$Z = R + \frac{1}{Cj} + Lj$$

$$i(t) = \frac{e^{jt}}{R + \frac{1}{Cj} + Lj}$$

$$= \frac{Cje^{jt}}{(1 - LC) + RCj} = \frac{Ce^{j(\frac{\pi}{2})}e^{jt}}{\sqrt{(1 - LC)^2 + R^2C^2}e^{j\tan^{-1}(\frac{RC}{1-LC})}}$$

$$i(t) = \frac{C}{\sqrt{(1 - LC)^2 + R^2C^2}}e^{j(t + \frac{\pi}{2} - tan^{-1}(\frac{RC}{1-LC}))}$$

$$i(t) = \frac{C}{\sqrt{(1 - LC)^2 + R^2C^2}}\cos\left[t + tan^{-1}\left(\frac{1 - LC}{RC}\right)\right]$$

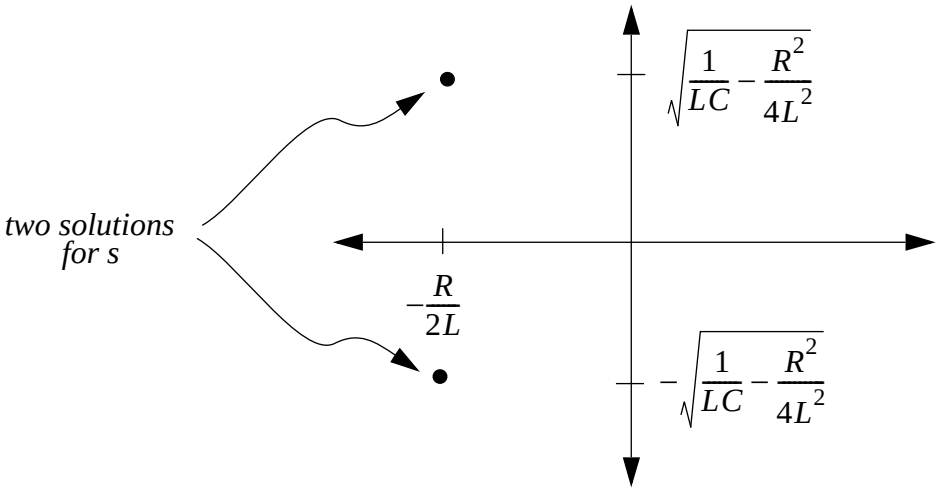


Figure 14.28:

d) See Figure 14.28

$$s^2+\frac{R}{L}s+\frac{1}{LC}=0$$

$$s=-\frac{R}{2L}\pm\frac{1}{2}\sqrt{\frac{R^2}{L^2}-\frac{4}{LC}}=-\frac{R}{2L}\pm i\sqrt{\frac{1}{LC}-\frac{R^2}{4L^2}}$$

ANS:: (a) $\frac{1}{L}v_I'(t)=i''+\frac{R}{L}i'+\frac{1}{LC}i$ (b) $\frac{LCs^2}{LCs^2+RCs+1}$ (c) $i(t)=\frac{C}{\sqrt{(1-LC)^2+R^2C^2}}\cos\left[t+tan^{-1}\left(\frac{1-LC}{RC}\right)\right]$ (d) $-\frac{R}{2L}\pm i\sqrt{\frac{1}{LC}-\frac{R^2}{4L^2}}$

Problem 14.6

a) In the circuit in Figure 14.29, given that $v_S=V_S\cos\omega t$, where $\omega=10^6$ rad/sec. Design a lossless coupling network containing one inductor and one capacitor that will maximize the power transferred to the antenna at frequency ω.

b) Now suppose that $v_S=V_S\cos\omega t+\epsilon cos3\omega t$, where ϵ represents a small amount of third harmonic distortion introduced by nonlinearities somewhere in the transmitter. Since the FCC forbids the broadcast of harmonics, it is important to check that coupling networks do not inadvertently favor the coupling of harmonics to the transmitter. For your design in a), calculate how much third harmonic reaches the antenna.

Solution:

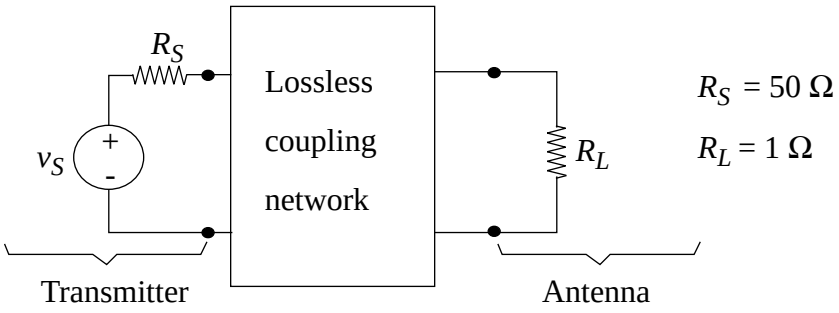


Figure 14.29:

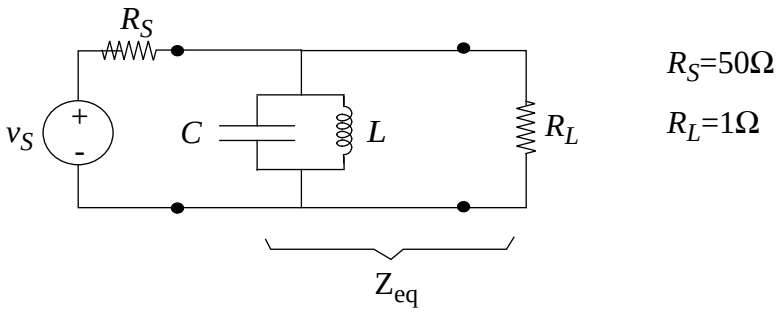


Figure 14.30:

a) $v_S = V_S \cos \omega t$, $\omega = 10^6$ See Figure 14.30 for network structure.

Specify L, C:

$$Z_{eq} = \frac{1}{\frac{1}{R} + \frac{1}{Ls} + Cs} = \frac{RLs}{R(LCs^2 + 1) + Ls}$$

make $LCs^2 + 1 = 0$ so that $Z_{eq} = R$, then:

$$1 - LC\omega^2 = 0$$

$$LC = \frac{1}{\omega^2} = 1 \times 10^{-12}$$

$$L = 1mH = 1 \times 10^{-3} H$$

$$C = 1nF = 1 \times 10^{-9} F$$

b) $v_S = V_S \cos \omega t + \epsilon \cos 3\omega t$

See Figure 14.31 for equivalent circuit.

$$Z_{th} = \frac{1}{\frac{1}{Ls} + Cs} = \frac{Ls}{LCs^2 + 1}$$

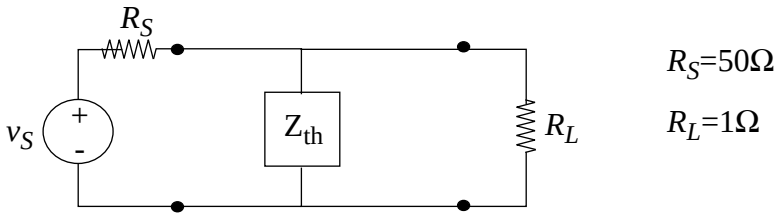
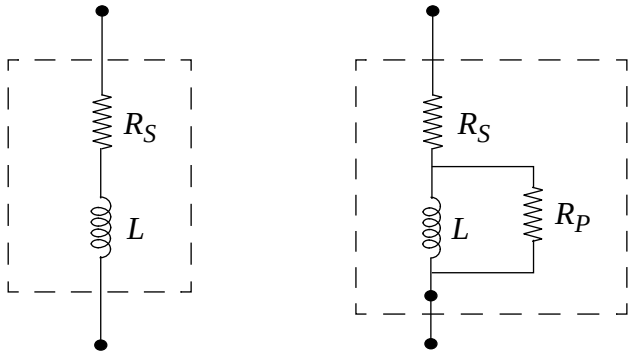


Figure 14.31:



Simple model of a physical inductor

More complex model

Figure 14.32:

From (a), $LC = \frac{1}{\omega^2}$. At $s = j3\omega$,

$$Z_{th} = \frac{j3\omega L}{-9\omega^2 LC + 1}$$

$$Z_{th} = \frac{3000j}{-8} = -375j = 375 \underbrace{e^{-j(\frac{\pi}{2})}}_{\text{phaseshift}}$$

Amount that reaches the antenna: use $|Z_{th}|$:

$$\frac{\epsilon}{R_S + \frac{Z_{th}R_L}{Z_{th}+R_L}} \cdot \left(\frac{Z_{th}R_L}{Z_{th}+R_L}\right) = \frac{15\epsilon}{767}$$

ANS:: (b) $\frac{15\epsilon}{767}$

Problem 14.7 Refer to the figure in Figure 14.32 for this problem.

The Q of a physical energy storage element may be defined as

$$Q_1 = \frac{Im(Z)}{Re(Z)} \tag{14.4}$$

where Z is the terminal impedance of the element. The Q may also be defined in terms of energy as

$$Q_2 = \frac{2\pi < W >}{E_{diss/cycle}} \tag{14.5}$$

where $< W >$ is the average stored energy and $E_{diss/cycle}$ is the energy dissipated per cycle.

a) For the simple inductor model, calculate and compare Q_1 and Q_2 as functions of frequency.

b) For the more complex model, and assuming $R_P >> R_S$, sketch Q_1 as a function of ω making reasonable approximations.

c) Suppose two inductors with the same Q_1 and (Q_{10}) are connected in series. Express Q_1 for the series combination in terms of Q_{10}.

Solution:

a) Simple Model: Find Q_1:

$$Z = R_S + Lj\omega$$

$$Q_1 = \frac{Im(Z)}{Re(Z)} = \frac{L\omega}{R_S}$$

Find Q_2:

$$W = \frac{1}{2}LI_i^2$$

$$< W >= \frac{\frac{1}{2}L\int_{period} I_i^2 dt}{Period}$$

where the Period = $\frac{2\pi}{\omega}$:

$$< W >= \frac{L\omega}{4\pi}\int_{period} I_i^2 dt$$

$$E_{diss} = I_i^2 R_S$$

$$E_{diss/cycle} = R_S \int_{period} I_i^2 dt$$

$$Q_2 = \frac{2\pi < W >}{E_{diss/cycle}} = \frac{L\omega}{2R_S}$$

To compare Q_1 and Q_2, find the ratio $\frac{Q_1}{Q_2} = 2$.

b) More complex model:

$$Z = R_S + \frac{1}{\frac{1}{j\omega L} + \frac{1}{R_P}} = R_S + \frac{j\omega R_P L}{R_P + j\omega L}$$

$$Z = R_S + \frac{j\omega R_P L(R_P - j\omega L)}{R_P^2 + \omega^2 L^2} = R_S + \frac{R_P L^2 \omega^2}{R_P^2 + L^2\omega^2} + j\frac{R_P^2 L\omega}{R_P^2 + \omega^2 L^2}$$

$$Q_1 = \frac{Im(Z)}{Re(Z)} = \frac{R_P^2 L\omega}{R_S R_P^2 + R_S L^2\omega^2 + R_P L^2\omega^2}$$

assuming $R_P \gg R_S$:

$$Q_1 \approx \frac{R_P L\omega}{R_S R_P + L^2\omega^2}$$

See Figure 14.33

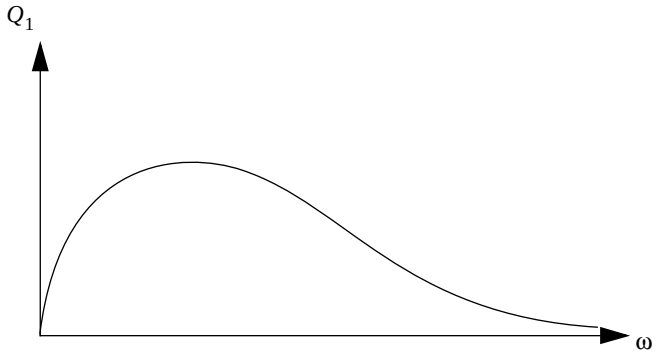


Figure 14.33:

c)

ANS:: (a) $Q_1 = \frac{L\omega}{R_S}$, $Q_2 = \frac{L\omega}{2R_S}$ (b) $Q_1 \approx \frac{R_P L\omega}{R_S R_P + L^2\omega^2}$

Problem 14.8 Communications receivers require high-Q circuits to separate signals broadcast on adjacent channels. Due to losses, modeled by the parallel resistance r, there is a limit to the Q that can be achieved with passive components. In the amplifier circuit in Figure 14.34, a variable resistor R_F has been added which has the effect of increasing the Q of the passive tuned circuit.

$R_S = 1k\Omega, r = 10000\Omega, \quad L = \frac{100}{\pi}\mu H, \quad \beta = 11, \quad R_F$ and C variable

a) Consider first the tuned circuit by itself, disconnected from the amplifier. If C is chosen so that the circuit has a $1MHz$ resonant frequency, what is its Q?

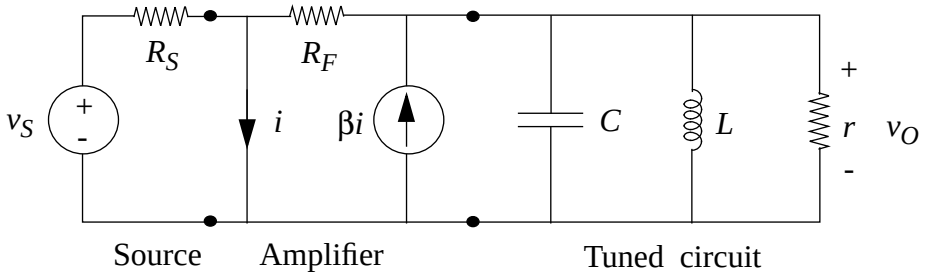


Figure 14.34:

b) Determine the overall transfer function $H(s) = V_o/V_s$.

c) Select values for C and R_F so that the overall frequency response is peaked at a frequency $1MHz$ and has a half-power band width of $2kHz$. (Note, the half-power bandwidth = 2α). What is the Q in this case?

Solution:

a)

$$Q = \omega_0 r C = \frac{r}{L\omega_0} = 50$$

b) See Figure 14.35 for reference.

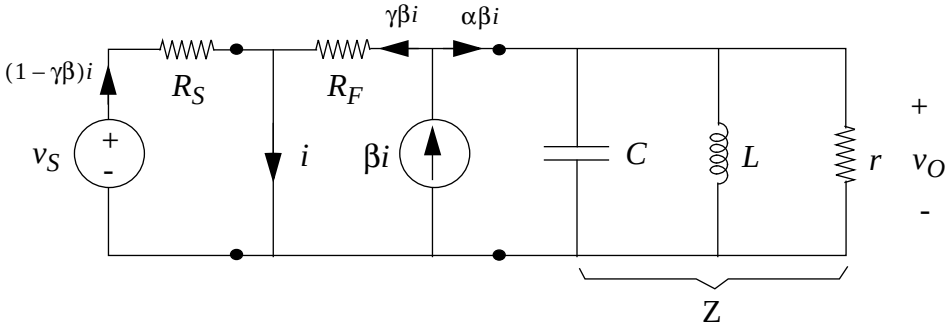


Figure 14.35:

$$Z = \frac{1}{\frac{1}{r} + \frac{1}{j\omega L} + j\omega C} = \frac{j\omega r L}{r(1-\omega^2 LC) + j\omega L}$$

$\alpha = \frac{R_F}{R_F+Z}$, $\gamma = \frac{Z}{R_F+Z}$

Find V_o:

$$V_o = \gamma\beta i R_F$$

Find i:

$$V_s = (1 - \gamma\beta) i R_S$$

$$i = \frac{V_s}{(1 - \gamma\beta) R_S}$$

Substitute:

$$V_o = \frac{\gamma\beta R_F V_s}{(1 - \gamma\beta) R_s}$$

$$\frac{V_o}{V_s} = \frac{\gamma\beta R_F}{(1 - \gamma\beta) R_S}$$

$$\gamma = \frac{j\omega r L}{R_F r(1 - \omega^2 LC) + j\omega R_F L + j\omega r L}$$

$$H(s) = \frac{V_o}{V_s} = \frac{j\omega\beta R_F r L}{R_S R_F r(1 - \omega^2 LC) + j\omega R_S R_F L + j\omega R_S r L - j\omega\beta R_S r L}$$

c)

$$2\alpha = \frac{1}{R'C}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$C = \frac{2.5}{\pi} \times 10^{-9} F = 7.96 \times 10^{-10} F$$

$$R' = 100,000\Omega$$

$$R_F \approx 89k\Omega$$

With these values, $Q = 500$

ANS:: (a) $Q = 50$ (b) $H(s) = \frac{j\omega\beta R_F r L}{R_S R_F r(1-\omega^2 LC)+j\omega R_S R_F L+j\omega R_S r L-j\omega\beta R_S r L}$ (c) $C = 7.96 \times 10^{-10} F$, $R_F \approx 89k\Omega$, $Q = 500$

Problem 14.9

a) Consider the two circuits in Figure 14.36.

Determine the transfer functions

$$H_1(s) = I_1/I_s \text{ and } H_2(s) = I_2/I_s$$

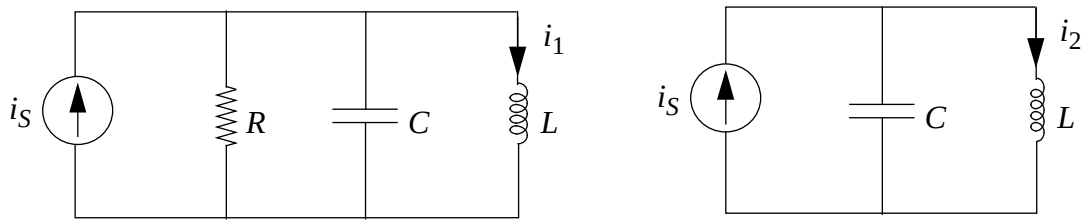


Figure 14.36:

b) Given $i_s(t) = u_{-1}(t)$, draw the circuits as they would appear in steady-state. (Recall that $u_{-1}(t)$ represents a unit step at time $t = 0$). What are the "forced responses" i_1^F and i_2^F?

c) Calculate the "natural responses" i_1^N and i_2^N. Assume:

$$i_L(0) = 0, \quad v_C(0) = 0, \quad R >> \sqrt{L/4C}$$

Why is i_2^F not the complete steady-state response of the second circuit?

d) Write the step response $i_1 = i_1^F + i_1^N$ and $i_2 = i_2^F + i_2^N$ in terms of ω_0 and Q.

Answer:

$$\begin{aligned} i_1(t) &= 1 - e^{-\omega_o t/2Q}(\frac{1}{2Q}\sin\omega_o T + \cos\omega_o t) \\ i_2(t) &= 1 - \cos\omega_o t \end{aligned}$$

e) $i_2(t)$ reaches maxima/minima at $t = \frac{n\pi}{\omega_o}, n = 0, 1, 2, ...$ For what value of n does $i_1^N(\frac{n\pi}{\omega_o} = \frac{1}{5}i_2^N(\frac{n\pi}{\omega_o})$.

For $Q = 5, 50, 500$ calculate

$$\frac{i_1^N(\frac{2\pi}{\omega_o})}{i_2^N(\frac{2\pi}{\omega_o})} \tag{14.6}$$

Sketch $i_1(t)$ for $Q = 50$.

Solution:

a) First Circuit:

$$H_1(s) = \frac{i_1}{i_S} = \frac{\frac{1}{\frac{1}{R}+Cs}}{\frac{1}{\frac{1}{R}+Cs} + Ls} = \frac{\frac{R}{1+RCs}}{\frac{R}{1+RCs} + Ls}$$

$$H_1(s) = \frac{R}{R + RLs + RLCs^2}$$

Second Circuit:

$$H_2(s) = \frac{i_2}{i_S} = \frac{\frac{1}{Cs}}{\frac{1}{Cs} + Ls} = \frac{1}{1 + LCs^2}$$

b) $i_S = u_{-1}(t)$

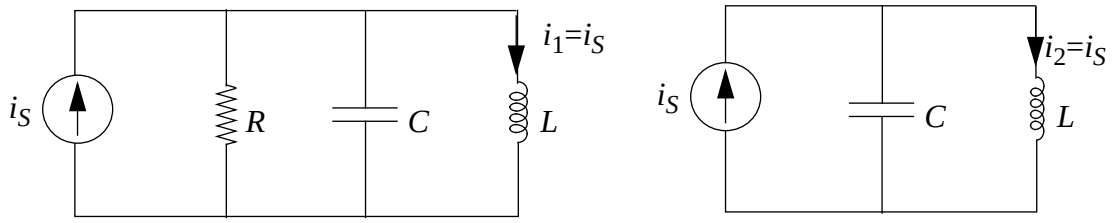


Figure 14.37:

See Figure 14.37 for circuit diagrams
First Circuit: $i_1^F = 1$
Second Circuit: $i_2^F = 1$

c) First Circuit:

$$\frac{i'}{C} = V'' + \frac{V'}{RC} + \frac{V}{LC}$$

Since $R \gg \sqrt{\frac{L}{4C}} \Rightarrow \omega \approx \omega_0$:

$$V = e^{-\alpha t}(A \sin \omega_0 t + B \cos \omega_0 t)$$
$$i_1^N = e^{-\alpha t}(A \sin \omega_0 t + B \cos \omega_0 t)$$
$$i_1^N(0) = -1 \Rightarrow B = -1$$
$$i_1'^N(0) = 0 = -\alpha B + A\omega_0 = 0$$

Since $\alpha = \frac{\omega_0}{2Q}$:

$$A = -\frac{\alpha}{\omega_0} = -\frac{1}{2Q}$$
$$i_1^N = -e^{-\alpha t}(\frac{1}{2Q} \sin \omega_0 t + \cos \omega_0 t)$$

Second Circuit:

$$i_2^N = A \sin \omega_0 t + B \cos \omega_0 t$$
$$i_2^N(0) = -1 \Rightarrow B = -1$$
$$i_2'^N(0) = 0 = A\omega_0 \Rightarrow A = 0$$
$$i_2^N = -\cos \omega_0 t$$

d) With $\alpha = \frac{\omega_0}{2Q}$:

$$i_1(t) = i_1^F + i_1^N = 1 - e^{-\omega_o t/2Q}(\frac{1}{2Q}\sin\omega_o t + \cos\omega_o t)$$

$$i_2(t) = i_2^F + i_2^F = 1 - \cos\omega_o t$$

e) ???

ANS:: (a) $H_1(s) = \frac{R}{R+RLs+RLCs^2}$, $H_2(s) = \frac{1}{1+LCs^2}$ (b) $i_1^F = 1$, $i_2^F = 1$ (c) $i_1^N = -e^{-\alpha t}(\frac{1}{2Q}\sin\omega_0 t + \cos\omega_0 t)$, $i_2^N = -\cos\omega_0 t$ (d) $i_1(t) = 1 - e^{-\omega_o t/2Q}(\frac{1}{2Q}\sin\omega_o t + \cos\omega_o t)$, $i_2(t) = 1 - \cos\omega_o t$

Problem 14.10 The circuit in Figure 14.38a is to be used as a bandpass filter having the magnitude-frequency curve shown in Figure 14.38b (linear coordinates). The input voltage is

$$\begin{aligned} v_s(t) &= V_s\cos\omega t \\ \text{and} & \\ w_c &= 1\times 10^6 radians/sec \\ w^+ &= 1.05\times 10^6 \\ w^- &= 0.95\times 10^6 \end{aligned} \tag{14.7}$$

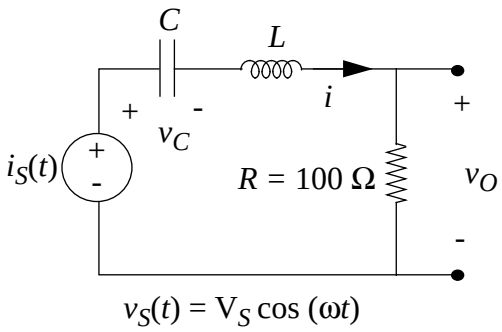
a) Find the appropriate values of L and C.
Using the values found in a):

i) Sketch $Ang\ V_o$ vs. ω.

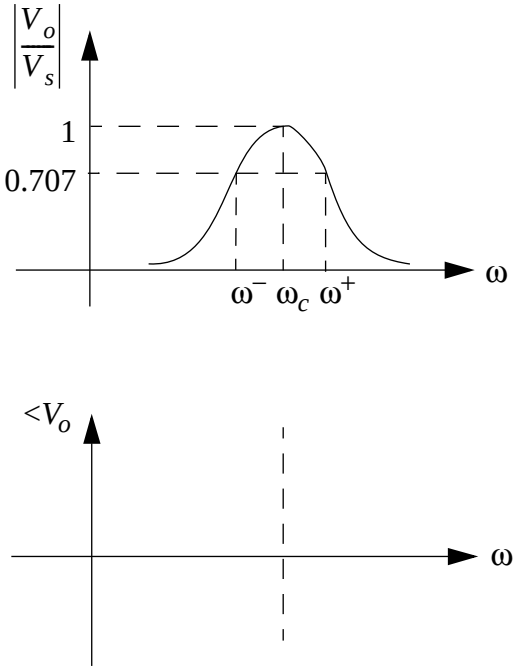
ii) Let $v_S = 10\cos 10^6 t$. Calculate $v_C(t), i(t), v_O(t)$.

iii) For $v_S = 10\cos 10^6 t$, determine the total stored energy W_s and the time-averaged power dissipated.

Solution:



(a)



(b)

Figure 14.38:

a)

$$Q = \frac{\omega_c}{\omega^+ - \omega^-} = 10$$

$$\omega_0 = \frac{1}{\sqrt{LC}} = 1 \times 10^6$$

$$Q = \frac{\omega_0 L}{R}$$

Solve for L and C:

$$L = 1mH$$

$$C = 1 \times 10^{-9} F$$

i) See Figure 14.39 for plot

$$\frac{V_O}{V_I} = \frac{R}{\frac{1}{j\omega C} + j\omega L + R} = \frac{j\omega RC}{(1 - \omega^2 LC) + j\omega RC}$$

$$= \frac{\omega RC e^{j(\frac{\pi}{2} - \tan^{-1}\left(\frac{\omega RC}{1-\omega^2 LC}\right))}}{\sqrt{(1-\omega^2 LC)^2 + (\omega RC)^2}}$$

$$\angle V_O = \tan^{-1}\left(\frac{1 - \omega^2 LC}{\omega RC}\right)$$

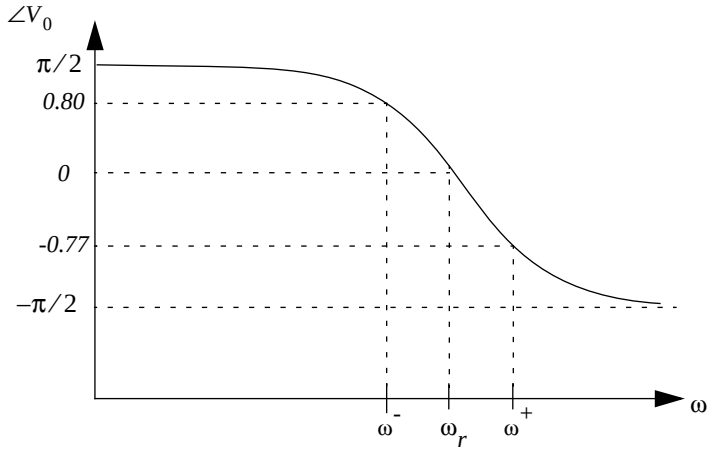


Figure 14.39:

ii) $v_S = 10\cos 10^6 t$ Find $v_c(t)$:

$$v_c(t) = \frac{10\cos(10^6 t - \frac{\pi}{2})}{\omega RC} = 100\cos(10^6 t - \frac{\pi}{2})$$

Find $i(t)$:

$$i(t) = \frac{v_S(t)}{Z} = \frac{10e^{j\omega t}}{\frac{1}{j\omega L} + j\omega L + R} = \frac{10(j\omega L)e^{j\omega t}}{(1-\omega^2 LC) + j\omega RC}$$

at ω_0:

$$i(t) = \frac{10e^{j\omega t}}{R} = 0.1\cos(10^6 t)$$

Find $v_O(t)$:

$$v_O(t) = 10\cos(10^6 t)$$

iii) Total stored energy:

$$W = \frac{1}{2}CV^2 + 12LI^2 = 5\times 10^{-6}\cos^2(10^6 - \frac{\pi}{2}) + 5\times 10^{-6}\cos^2(10^6 t)$$

$$W = 5\times 10^{-6} J$$

Average power dissipated:

$$P = I^2 R = \cos^2(10^6 t)$$

$$< P >= 0.5$$

ANS:: (a) $L = 1mH$, $C = 1\times 10^{-9}F$ (i) $\angle V_O = \tan^{-1}\left(\frac{1-\omega^2 LC}{\omega RC}\right)$ (ii) $v_c(t) = 100\cos(10^6 t - \frac{\pi}{2})$, $i(t) = 0.1\cos(10^6 t)$, $v_O(t) = 10\cos(10^6 t)$ (iii) $W = 5\times 10^{-6} J$, $< P >= 0.5$

Problem 14.11 An RLC circuit is shown in Figure 14.40.

The magnitude of $\frac{I_i}{V_i}(j\omega)$ is measured and is as plotted in Figure 14.41 (on log-log coordinates).

a) What is the value of C?

b) What is the value of R?

c) What is the value of $\Delta\omega$?

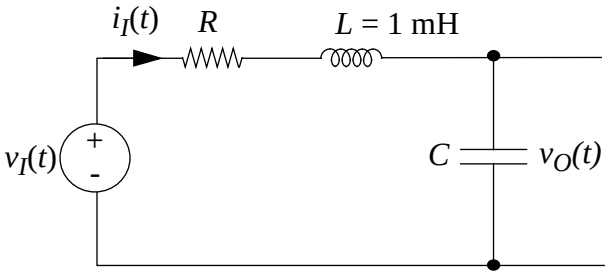


Figure 14.40:

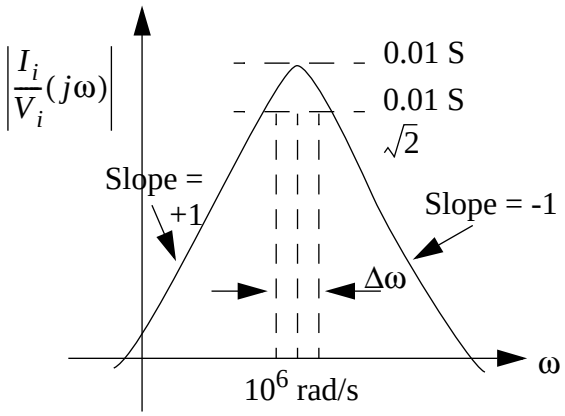


Figure 14.41:

d) The circuit is now excited with a unit step of voltage. The values of $i_I(t)$ and $v_O(t)$ are zero prior to time $t = 0$.

Sketch the signal $v_O(t)$ for t greater than zero, labeling important features.

Solution:

a)

$$\omega_0 = 10^6$$

$$C = 10^{-9} F$$

b) at resonance:

$$R = \left\| \frac{V_i}{I_i} \right\| = 100\Omega$$

c)

$$Q = \frac{\omega_0 L}{R} = 10$$

$$Q = \frac{\omega_0}{\Delta\omega} = 10$$

$$\Delta\omega = 100,000 \frac{rad}{s}$$

d) See Figure 14.42 for plot of v_O

$$\frac{1}{L} v_I'(t) = i'' + \frac{R}{L} i' + \frac{1}{LC} i$$

$$s^2 + \frac{R}{L} s + \frac{1}{LC} = 0$$

$$s = -\frac{R}{2L} \pm j\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} = -5000 \pm j \underbrace{(998,749)}_{\omega}$$

$$i = A^{st+B}$$

$$v_O = \frac{\int i dt}{C} = \frac{A}{Cs} e^{st+B} + D = 1 - e^{-5000t}[A \sin(\omega t) + B \cos(\omega t)]$$

$$v_O(0) = 0 \Rightarrow B = 1$$

$$v_O'(0) = 0 \Rightarrow 5000B - A\omega = 0 \Rightarrow A = 0.005$$

$$v_O(t) = 1 - e^{-5000t}[0.005 \sin(998,749t) + \cos(998,749t)]$$

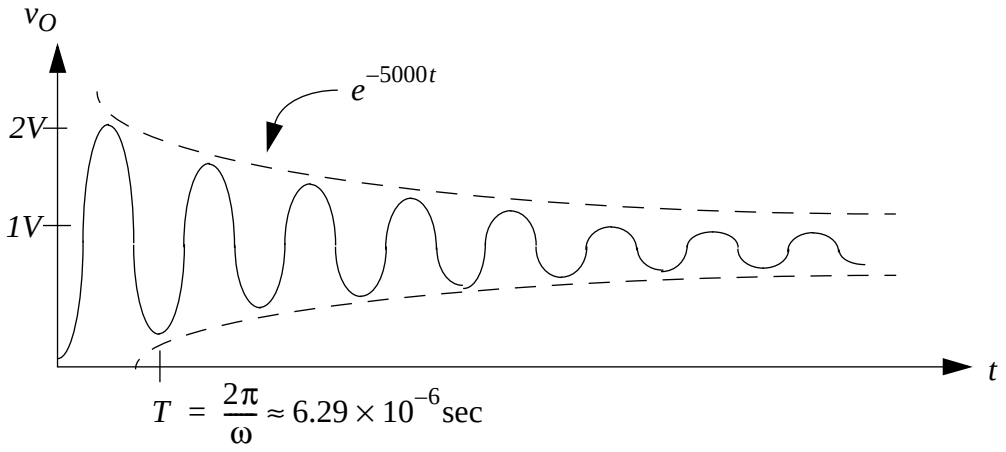


Figure 14.42:

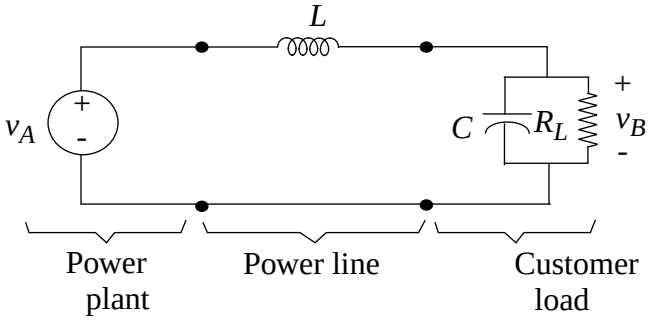


Figure 14.43:

ANS:: (a) $C = 10^{-9}F$ (b) $R = 100\Omega$ (c) $\Delta\omega = 100,000\frac{rad}{s}$ (d) $v_O(t) = 1 - e^{-5000t}[0.005\sin(998,749t) + \cos(998,749t)]$

Problem 14.12 Refer to Figure 14.43 for this problem.

$v_A = A\cos 400t \quad A = 141 kilovolts, \quad L = 0.25H$

This problem examines a simple model of an electric power system. The source v_A represents the generator in the power plant. The inductance L represents the net effect of all power lines and transformers. The customer's load is represented by resistance R_L to which the capacitor C is added in parts b) and c).

a) No capacitor. $R_L = 100\Omega$. Find the magnitude of v_B and the average power dissipated in R_L.

b) In an attempt to improve on the situation in part a), the customer adds a capacitor in parallel with his load. He finds that a $25\mu F$ capacitor works well. Find the magnitude of v_B and the power dissipated in R_L for $R_L = 100\Omega$ and $C = 25\mu F$.

c) The customer is now very happy. However, before going home for the night, he turns off 90% of his load (making $R_L = 1k\Omega$), at which point sparks and smoke begin to appear in the equipment still connected to the power line. The customer calls you in as a consultant to straighten things out:

   i) Why did sparks appear when the customer tried to turn off 90% of the load?

   ii Assuming a variable R_L in the range $100 \leq R_L \leq 1000\Omega$ provide the customer with a simple formula he can use to calculate the right value of C so that the magnitude of v_B is always equal to $141kV$.

Solution:

a) No capacitor:

$$Z = j\omega L + R_L$$

$$i = \frac{V_A}{R_L + j\omega L}$$

$$v_B = \frac{R_L V_A}{R_L + j\omega L} = \frac{R_L A e^{j\omega t}}{R_L + j\omega L}$$

$$|v_B| = \frac{R_L A}{\sqrt{R_L^2 + \omega^2 L^2}} = 99.7kV$$

Average power dissipated:

$$< P >= \frac{1}{2}\frac{|v_B|^2}{R_L} = \frac{1}{2}\frac{R_L A^2}{R_L^2 + \omega^2 L^2} = 49.7MW$$

b) Capacitor, with $C = 25\mu F$

$$Z = j\omega L + \frac{1}{\frac{1}{R_L} + j\omega C} = j\omega L + \frac{R_L}{1 + j\omega R_L C} = \frac{R_L(1 - \omega^2 LC) + j\omega L}{1 + j\omega R_L C}$$

Let i be the total current entering the load R-C circuit, and i_R be the current through the resistor:

$$i = \frac{(1 + j\omega R_L C)}{R_L(1 - \omega^2 LC) + j\omega L} v_A$$

From the current divider law:

$$i_R = \frac{\frac{1}{j\omega c}}{\frac{1}{j\omega C} + R_L} i = \frac{1}{1 + j\omega R_L L} i$$

$$i_R = \frac{v_A}{R_L(1 - \omega^2 LC) + j\omega L}$$

Since $|v_B| = R_L \cdot |i_R|$, and $|v_A| = A$:

$$|v_B| = \frac{R_L \cdot A}{\sqrt{R_L^2(1 - \omega^2 LC) + \omega^2 L^2}} = 141kV$$

Power dissipated:

$$< P >= \frac{1}{2} \frac{|v_B|^2}{R_L} = 99.4MW$$

c) i) Immediately after the customer changes the load, the voltage on the capacitor cannot change, so the voltage across the resistor also stays the same. As a result, the current increases by a factor of 100, and so the power dissipated in the resistor increases by a factor of 100 briefly, overloading the resistor.

ii) From the expression for $|v_B|$ derived in part (b), we see that for $|v_B| = 141kV = A$, we require that:

$$\frac{R_L}{\sqrt{R_L^2(1 - \omega^2 LC) + \omega^2 L^2}} = 1$$
$$R_L^2(1 - \omega^2 LC) + \omega^2 L^2 = R_L^2$$
$$R_L^2 - (\omega^2 L R_L^2)C + \omega^2 L^2 = R_L^2$$
$$(\omega^2 L R_L^2)C = \omega^2 L^2$$
$$C = \frac{L}{R_L^2}$$

With $L = 0.25H$:

$$C = \frac{1}{4R_L^2}$$

ANS:: (a) $|v_B| = 99.7kV, < P >= 49.7MW$ (b) $|v_B| = 141kV, < P >= 99.4MW$ (ii) $C = \frac{1}{4R_L^2}$

Problem 14.13 Refer to Figure 14.44 for this problem.

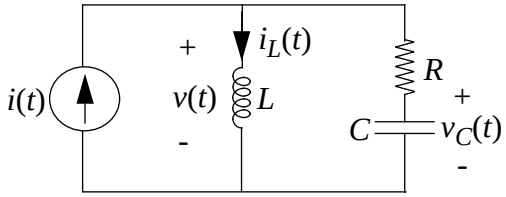


Figure 14.44:

$\frac{R}{2L} = 1 \quad \frac{1}{LC} = 2 \quad R = 5 \quad \frac{1}{RC} = 1$

a) Assume that $i(t) = 0$ for $t > 0$, and that $i_L(0) = 0, v_C(0) = V_o$. Find $v_C(t)$ for $t > 0$. Simplify your answer, and make a rough sketch of $v_C(t)$ showing its behavior.

b) Find the transfer function (system function) relating $V(s)$ to $I(s)$.

c) When $i(t) = 2e^{-3t}$, it is known that the voltage $v(t)$ can be expressed as

$$v(t) = Ae^{s_1 t} + Be^{s_2 t} + De^{-3t} \tag{14.8}$$

Find s_1, s_2 and D. (You need not find A and B).

Solution:

a) See Figure 14.45 for plot

Given: $\frac{1}{LC} = 16$; $\frac{R}{L} = 10$; $R = 25$

$$\Rightarrow \omega_0^2 = 16; 2\alpha = 10 \Rightarrow \alpha = 5$$

$$s = -5\sqrt{25 - 16} = \{-8, -2\}$$

$$v_C = Ae^{-2t} + Be^{-8t}$$

$$v_C(0) = A + B = V_0 \Rightarrow -3B = V_0 \Rightarrow B = -\frac{V_0}{3}$$

$$\frac{dv_C(0)}{dt} = 0 = -2A - 8B \Rightarrow A = -4B \Rightarrow A = \frac{4V_0}{3}$$

Substituting:

$$v_C = \frac{4V_0}{3}e^{-2t} - \frac{V_0}{3}e^{-8t}$$

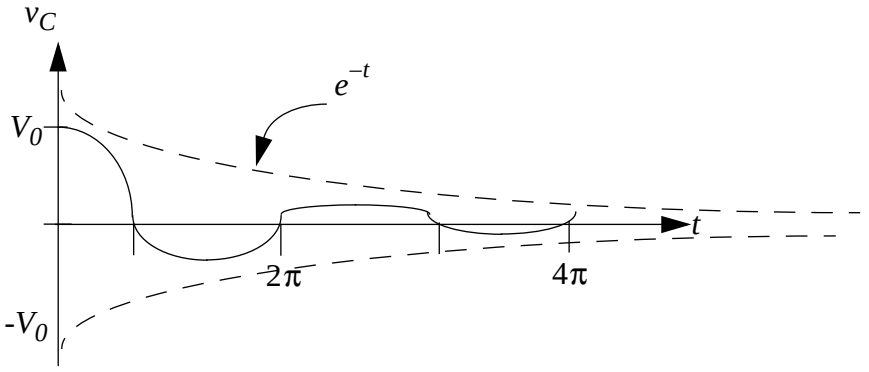


Figure 14.45:

b) Transfer function:

$$\frac{V(s)}{I(s)} = Ls||(R + \frac{1}{Cs}) = \frac{Ls \cdot (R + \frac{1}{Cs})}{Ls + (R + \frac{1}{Cs})}$$

$$= \frac{Rs^2 + \frac{s}{C}}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$$

$$= \frac{RLCs^2 + Ls}{LCs^2 + RCs + 1}$$

c) From part (a), $s_1 = -2$, $s_2 = -8$. From the transfer function in part (b), we have that:

$$\frac{d^2v}{dt^2} + \frac{R}{L}\frac{dv}{dt} + \frac{1}{LC}v = R\frac{d^2i}{dt^2} + \frac{i}{C}$$

With the values given in the problem:

$$\frac{d^2v}{dt^2} + 10\frac{dv}{dt} + 16v = 25\frac{d^2i}{dt^2} + 40i$$

We also have:

$$i = 2e^{-3t}$$
$$v = De^{-3t}$$

We can find the first and second derivatives in a straightforward manner. Substituting, we then have:

$$9D + 10 \cdot (-3D) + 16D = 25 \cdot 18 + 40 \cdot (-6)$$

Solving for D:

$$D = -42$$

ANS:: (a) $v_C = \frac{4V_0}{3}e^{-2t} - \frac{V_0}{3}e^{-8t}$ (b) $\frac{RLCs^2+Ls}{LCs^2+RCs+1}$ (c) $s_1 = -2$, $s_2 = -8$, $D = -42$

Problem 14.14 Refer to Figure 14.46 for this problem.

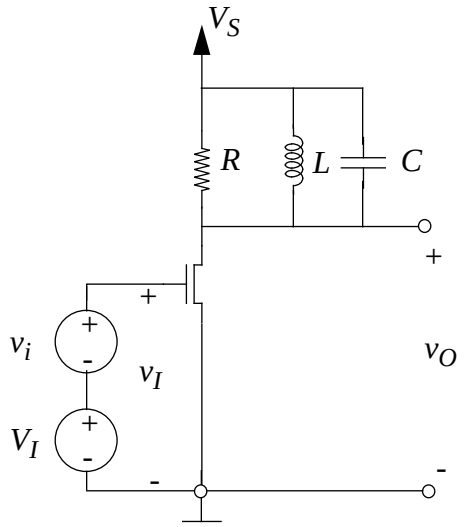


Figure 14.46:

$V_T = 1V \quad K = 1\ mA/V^2$

a) For $v_i(t)$ a small sinusoidal voltage, choose V_I, R, L and C to give a resonance at $\omega = 10^5$ radians/sec, $Q = 10$, and an incremental gain v_o/v_i at resonance of -2. Use the incremental model.

Solution:

MOSFET small signal model (Figure 14.47):

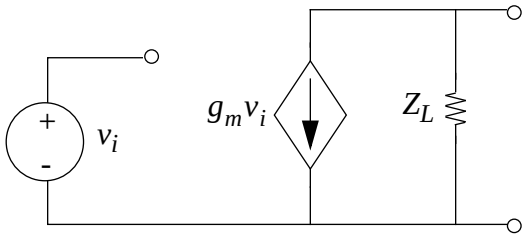


Figure 14.47:

$$g_m = K(V_I - V_T)$$

$$V_{out} = -Z_L K(V_S - V_T)$$

We need the following features: Resonance: $\omega_0 = \frac{1}{\sqrt{LC}} = 10^5 \frac{radians}{sec}$

Quality: $\omega_0 RC = 10$

Gain: $-|R_L|K(V_I - V_T) = -2$, at resonance

Calculate $|Z_L|$ first:

$$Z_L = R \| L_S \| \frac{1}{C_S}$$

$$\frac{1}{Z_L} = \frac{1}{R} + \frac{1}{Ls} + Cs = \frac{Ls + R + RCLs^2}{RLs}$$

$$Z_L = \frac{RLj\omega}{Lj\omega + R + RCL\omega^2}$$

$$|Z_L| = \frac{RL\omega}{\sqrt{(R - RCL\omega^2) + (L\omega)^2}}$$

Substitute in $\omega = \frac{1}{\sqrt{LC}}$:

$$|Z_L| = \frac{\frac{RL}{\sqrt{LC}}}{\sqrt{(R - \frac{RLC}{LC})^2 + (\frac{L}{\sqrt{LC}})^2}} = \frac{R\sqrt{\frac{L}{C}}}{\sqrt{\frac{L^2}{LC}}} = R$$

(Note: This is expected: at resonance, the effects of the capacitor and inductor cancel out perfectly.)

From the resonance constraint:

$$\frac{1}{\sqrt{LC}} = 10^5 \Rightarrow LC = 10^{-10}$$

Choose $L = 4.7 \times 10^{-3} H$, $C = 2.2 \times 10^{-8} F$. These are standard element values for inductors and capacitors, and as a result are readily available. (This was not asked for in the problem, so this is one of many possible answers). These choices give $LC = 1.034 \times 10^{-10}$, an error of 3.4%.

From the quality factor:

$$\omega_0 RC = 10$$

$$9.83 \times 10^4 \cdot R \cdot 2.2 \times 10^{-8} = 10 \Rightarrow 2.163 \times 10^{-3} \cdot R = 10$$

$$R = \frac{1}{2.163 \times 10^{-4}} \approx 4.6 \times 10^3 \Omega$$

To again choose a standard value, choose $R = 4.7 k\Omega$.

From the gain expression:

$$-4.7 \times 10^3(10^{-3})(V_I - 1) = 2$$

$$V_I - 1 = \frac{2}{4.7}$$

$$V_I \approx 1.426V$$

Summary of choices:

$$V_I \approx 1.426V, R = 4.7k\Omega, L = 4.7 \times 10^{-3}H, C = 2.2 \times 10^{-8}F$$

ANS:: $V_I \approx 1.426V, R = 4.7k\Omega, L = 4.7 \times 10^{-3}H, C = 2.2 \times 10^{-8}F$

Problem 14.15 The two networks shown in Figure 14.48 are driven in sinusoidal steady state by the voltage $v_{\rm I}(t) = V_{\rm I}\cos(\omega t)$. Their outputs take the form $v_{\rm O}(t) = V_{\rm O}\cos(\omega t + \phi)$.

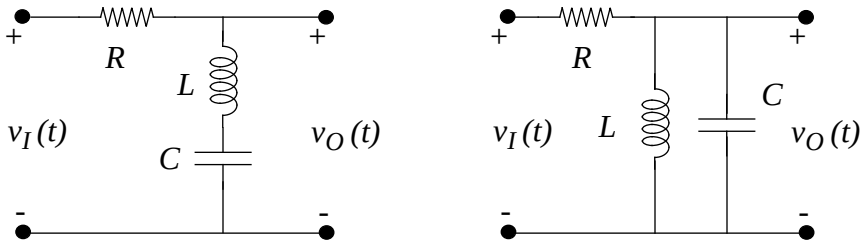


Figure 14.48:

a) For both networks, find $V_{\rm O}$ and ϕ as functions of $V_{\rm I}$ and ω using impedance methods.

b) For both networks, let $R = 1000\ \Omega$, $L = 47$ mH and $C = 4.7$ nF. Plot and clearly label $V_{\rm O}/V_{\rm I}$ for $2\pi \times 10^3$ rad/s $\leq \omega \leq 2\pi \times 10^5$ rad/s; use a linear axis for $V_{\rm O}/V_{\rm I}$, and a logarithmic axis for ω. You need only plot enough points to outline the dependence of $V_{\rm O}/V_{\rm I}$ on ω.

c) Describe the filtering function of each network, and how each network acts to perform its function.

Solution:

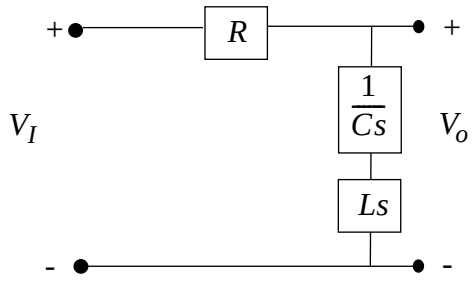


Figure 14.49:

a) First circuit:

Impedance model (Figure 14.49).

By voltage-divider:

$$V_O(s) = \Big(\frac{Ls + \frac{1}{Cs}}{Ls + \frac{1}{Cs} + R}\Big)V_I = \Big(\frac{LCs^2 + 1}{LCs^2 + RCs + 1}\Big)V_I(s)$$

$$V_O(j\omega) = \Big(\frac{1 - LC\omega^2}{(1 - LC\omega^2) + j\omega RC}\Big)V_I(j\omega)$$

Find magnitude $|V_O|$:

$$|V_O(j\omega)| = \frac{1 - LC\omega^2}{\sqrt{(1 - LC\omega^2)^2 + (\omega RC)^2}}|V_I(j\omega)|$$

Since $V_O(j\omega) = Re\{V_O e^{j(\omega t + \phi)}\}$, and $V_I(j\omega) = Re\{V_I e^{j(\omega t)}\}$:

$$V_O = \Big(\frac{1 - LC\omega^2}{\sqrt{(1 - LC\omega^2)^2 + (\omega RC)^2}}\Big)V_I$$

Find phase:

$$\phi = \angle V_O(j\omega) = \Big[tan^{-1}(0) - tan^{-1}\Big(\frac{\omega RC}{1 - LC\omega^2}\Big)\Big] + \angle V_I$$

$$\phi = -tan^{-1}\Big(\frac{\omega RC}{1 - LC\omega^2}\Big)$$

Second circuit:

Impedance model (Figure 14.50).

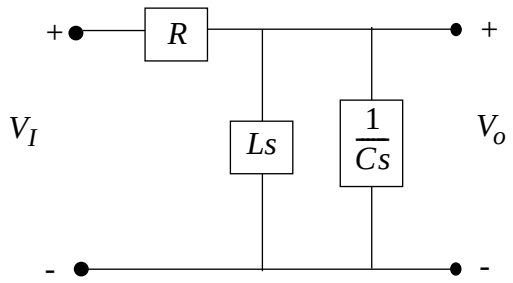


Figure 14.50:

By voltage-divider:

$$V_O(s) = \left(\frac{\frac{Ls}{1+LCs^2}}{\frac{Ls}{1+LCs^2}+R}\right)V_I(s) = \left(\frac{Ls}{Ls+R+RLCs^2}\right)V_I(s)$$

$$V_O(j\omega) = \left(\frac{j\omega L}{(R-RLC\omega^2)+j\omega L}\right)V_I(j\omega)$$

Magnitude:

$$V_O = |V_O(j\omega)| = \left(\frac{\omega L}{\sqrt{R^2(1-LC\omega^2)^2+(\omega L)^2}}\right)V_I$$

Phase:

$$\phi = \angle V_O(j\omega) = \frac{\pi}{2} - tan^{-1}\left(\frac{\omega L}{R(1-LC\omega^2)}\right)$$

b) First circuit: See Figure 14.51

$$\frac{V_O}{V_I} = \frac{LCs^2+1}{LCs^2+RCs+1}$$

$$\frac{|V_O|}{|V_I|} = \frac{1-LC\omega^2}{\sqrt{(1-LC\omega^2)^2+(\omega RC)^2}}$$

Second circuit: See Figure 14.52

$$\frac{V_O}{V_I} = \frac{Ls}{(RLC)s^2+Ls+R}$$

$$\frac{|V_O|}{|V_I|} = \left(\frac{\omega L}{\sqrt{R^2(1-LC\omega^2)^2+(\omega L)^2}}\right)$$

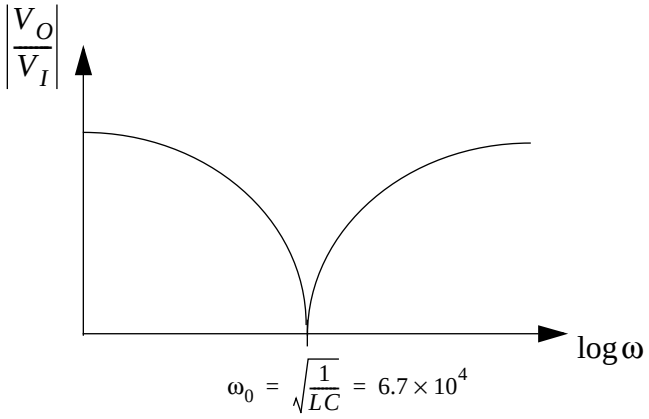


Figure 14.51:

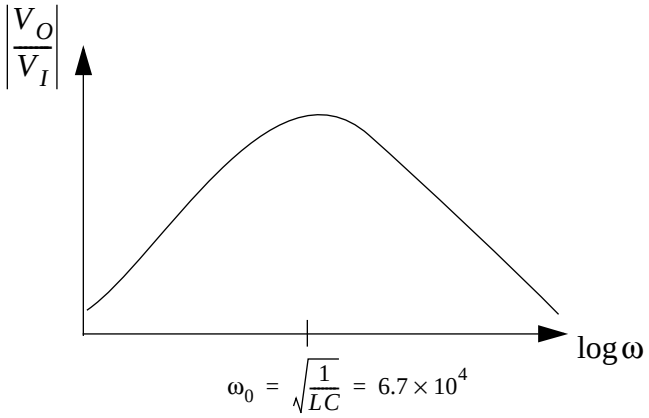


Figure 14.52:

c) First circuit: Notch filter. Takes voltage across 2 elements.

Second circuit: Band-pass filter.

ANS:: (a) (i) $V_O = \left(\frac{1-LC\omega^2}{\sqrt{(1-LC\omega^2)^2+(\omega RC)^2}}\right)V_I$, $\phi = -tan^{-1}\left(\frac{\omega RC}{1-LC\omega^2}\right)$ (ii) $V_O = |V_O(j\omega)| = \left(\frac{\omega L}{\sqrt{R^2(1-LC\omega^2)^2+(\omega L)^2}}\right)V_I$, $\phi = \angle V_O(j\omega) = \frac{\pi}{2} - tan^{-1}\left(\frac{\omega L}{R(1-LC\omega^2)}\right) = tan^{-1}\left(\frac{R(1-LC\omega^2)}{\omega L}\right)$ (c) (i) notch (ii) band-pass

Problem 14.16 This problem examines the very simple tuner for an AM radio shown in Figure 14.53. Here, the tuner is the parallel inductor and capacitor. The injection of radio signals into the tuner by the antenna is modeled by a current source, while the Norton resistance of the antenna in parallel with the remainder of the radio is modeled by a resistor. (You can learn more about antenna modeling in follow-on courses in Electromagnetic Waves.) The AM radio band extends from 540 kHz through 1600 kHz. The information transmitted by each radio station is constrained to be within ± 5 kHz of its center frequency. (You can learn more about AM radio transmission in courses in signals and systems.) To prevent frequency overlap of neighboring stations, the center frequency of each station is constrained to be a multiple of 10 kHz. Therefore, the purpose of the tuner is to pass all frequencies within 5 kHz of the center frequency of the selected station, while attenuating all other frequencies.

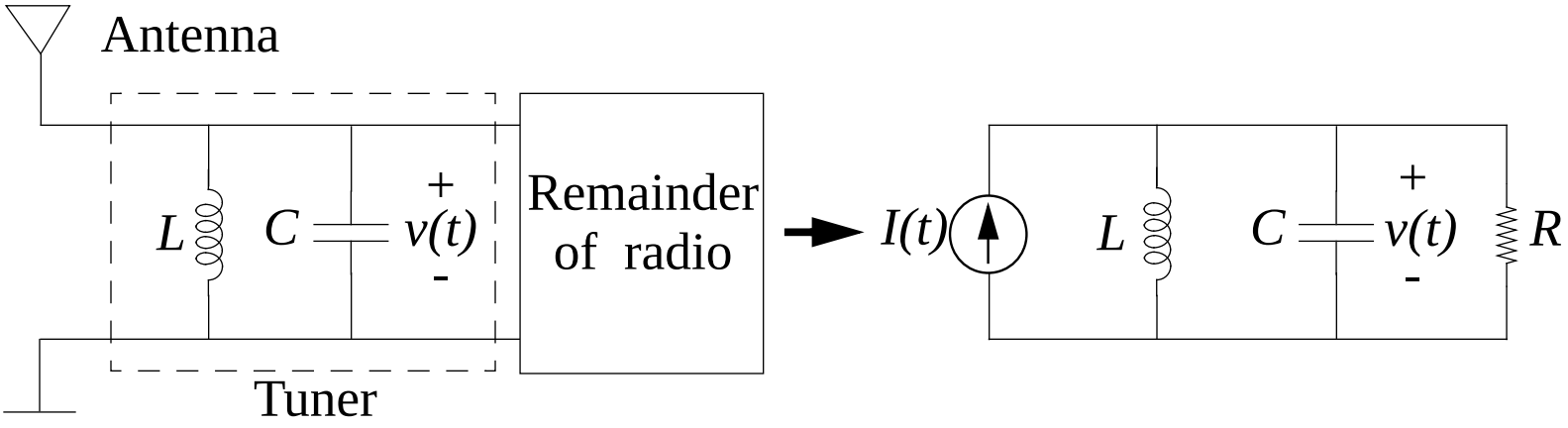


Figure 14.53:

a) Assume that $I(t) = I\cos(\omega t)$. Find $v(t)$ where $v(t) = V\cos(\omega t + \phi)$, and both V and ϕ are functions of ω. Note that $v(t)$ is the output of the tuner, namely the signal that is passed on to the remainder of the radio.

b) For a given combination of I, C, L and R, at what frequency is V maximized?

c) Assume that L = 365 μH. Over what range of capacitance must C vary so that the frequency of maximum V/I may be tuned over the entire AM band. Not that tuning the frequency of maximum V/I to the center frequency of a particular station tunes in that station.

d) As a compromise between passing all frequencies within 5 kHz of a center frequency and rejecting all frequencies outside that band, let the design of R be such that $V(1\text{ MHz } \pm \text{ 5 kHz})/V(1\text{ MHz}) \approx 0.25$ when the tuner is tuned to 1 MHz. Given this design criterion, determine R.

e) Given your design for R, determine $V(1\text{ MHz } \pm 10\text{kHz})/V(1\text{ MHz})$. Also, determine Q for the tuner and its load resistor when the tuner is tuned to 1 MHz.

Solution:

a) Impedance of each element: $Z_R = R$, $Z_L = Ls$, $Z_C = \frac{1}{Cs}$

Voltage across the capacitor: $V = I_C Z_C$

By the current divider law:

$$I_C = \frac{Z_L Z_R}{Z_L Z_C + Z_L Z_R + Z_C Z_R} \cdot I$$

$$V = I_C Z_C = \frac{Z_L Z_R Z_C}{Z_L Z_C + Z_L Z_R + Z_C Z_R} \cdot I = \frac{I R \frac{L}{C}}{\frac{L}{C} + RLs + \frac{R}{Cs}}$$

$$= \frac{I R \frac{L}{C} j\omega}{-RL\omega^2 + j\omega\frac{L}{C} + \frac{R}{C}}$$

$$V = \frac{RLj\omega}{-RLC^2 + Lj\omega + R} \cdot I$$

$$|V| = \frac{RL\omega}{\sqrt{(R - RLC\omega^2)^2 + (L\omega)^2}}$$

$$\phi = \frac{\pi}{2} - tan^{-1}\Big(\frac{L\omega}{R(1 - LC\omega^2)}\Big)$$

$$v(t) = |V| cos(\omega t + \phi)$$

b) By inspection, and from previous examples, the frequency at which V is maximized is: $\omega = \sqrt{\frac{1}{LC}}$. A more rigorous proof follows:

We are allowed to maximize only what is in the square-root, since the square-root function is monotonically increasing:

$$V = \frac{RL\omega}{\sqrt{(R - RLC\omega^2)^2 + (L\omega)^2}}$$

$$= \sqrt{\frac{R^2L^2\omega^2}{(R - RLC\omega^2)^2 + (L\omega)^2}}$$

This expression is maximized when its reciprocal is minimized:

$$[R^2(1 - LC\omega^2 + L^2\omega^2](R^{-2}L^{-2}\omega^{-2}) = (L^{-2}\omega^{-2})(1 - LC\omega^2)^2 + R^{-2}$$

$$= L^{-2}\omega^{-2}(1 - 2LC\omega^2 + L^2C^2\omega^4) + R^{-2}$$

$L^{-2}\omega^{-2} + 2\frac{C}{L} + C^2\omega^2 + R^{-2}$ is minimized when its derivative with respect to $\omega = 0$, so take derivative:

$$-2L^{-2}\omega^{-3} + 2C^2\omega = 0 \Rightarrow L^{-2}\omega^{-3} = C^2\omega \Rightarrow L^{-2}C^{-2} = \omega^4 \Rightarrow \omega = \sqrt{\frac{1}{LC}}$$

c) $L = 365\mu H$, AM band: 540 kHz to 1600 kHz.

We want ω_0 to vary over the AM band:

$$\omega_0 = \sqrt{\frac{1}{(365 \times 10^{-6}H) \cdot C}} = 2739.7\sqrt{\frac{1}{C}}$$

i) upper bound for C:

$$\omega_0 = 540 \times 10^3 Hz = 2739.7\sqrt{\frac{1}{C}} \Rightarrow C = 2.57 \times 10^{-5}F$$

ii) lower bound for C:

$$\omega_0 = 1600 \times 10^3 Hz = 2739.7\sqrt{\frac{1}{C}} \Rightarrow C = 2.93 \times 10^{-6}F$$

So:

$$2.93 \times 10^{-6} < C < 2.57 \times 10^{-5}$$

d) First, let us find values for L and C that give this tuning:

$$\frac{1}{\sqrt{LC}} = 10^7 \Rightarrow LC = 10^{-14}$$

Choose: $L = 10^{-4}$, $C = 10^{-10}$

Now, an expression for $\frac{V_{1MHz}}{V_{995kHz}}$:

$$\frac{V_{1000}}{V_{995}} = 1.005 \cdot \frac{\sqrt{R^2(1-0.99)^2 + 9.9 \times 10^5}}{\sqrt{10^6}} = \frac{1}{0.25}$$

Solve for R:

$$3.98 \times 10^3 = \sqrt{10^{-4}R^2 + 9.9 \times 10^{-5}}$$
$$1.485 \times 10^7 = 10^{-4} \cdot R^2$$
$$R = 1.22 \times 10^6 \Omega$$

e)

$$\frac{V_{990}}{V_{1000}} = 0.990 \cdot \frac{\sqrt{10^6}}{\sqrt{R^2(1-(10^{-14})(9.9 \times 10^6)^2) + (10^{-8})(9.9 \times 10^6)^2}}$$
$$= 0.990 \cdot \frac{10^3}{\sqrt{(1.22 \times 10^6)^2(1-0.98)^2 + (9.8 \times 10^5)}}$$
$$= \frac{990}{2.4 \times 10^4} = 0.0405$$

Quality factor:

$$Q = \omega_0 RC = (10^7)(1.22 \times 10^6)(10^{-10}) = 1.22 \times 10^4$$

ANS:: (a)$|V| = \frac{RL\omega}{\sqrt{(R-RLC\omega^2)^2+(L\omega)^2}}$, $\phi = \frac{\pi}{2} - tan^{-1}\left(\frac{L\omega}{R(1-LC\omega^2)}\right)$ (b) $\omega = \sqrt{\frac{1}{LC}}$ (c) $2.93 \times 10^{-6} < C < 2.57 \times 10^{-5}$ (d) $R = 1.22 \times 10^6 \Omega$ (e) 0.0405, $Q = 1.22 \times 10^4$

Chapter 15

The Operational Amplifier Abstraction

Exercises

Exercise 15.1 Find the Thévenin equivalent for the circuit in Figure 15.1. The circuit contains two resistors and a dependent current source.

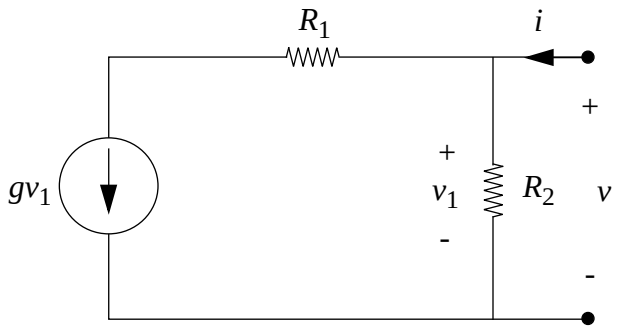


Figure 15.1:

Solution:

KCL:

$$-g \cdot \ v_1 + i + \frac{0 - v_1}{R_2} = 0$$

$$\frac{v_1}{i} = R_{th} = \frac{R_2}{gR_2 + 1}$$

$$v_{OC} = 0$$

ANS:: $R_{th} = \frac{R_2}{gR_2+1}, v_{th} = 0$

Exercise 15.2 Calculate v_O in terms of I_1, V_1, V_2, in Figure 15.2. You may assume the operational amplifier has ideal characteristics.

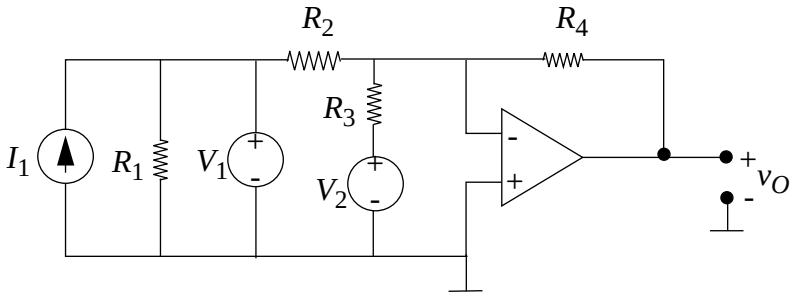


Figure 15.2:

Solution:

$$V_0 = -\frac{R_4}{R_2} \cdot V_1 - \frac{R_4}{R_3} \cdot V_2$$

ANS:: $v_O = -\frac{R_4}{R_2}V_1 - \frac{R_4}{R_3}V_2$

Exercise 15.3 Calculate the sensitivity of the gain, dG/G, as a function of fractional change in Op Amp gain, dA/A for the inverting Op Amp connection shown in Figure 15.3.

Solution:

$$\frac{dG}{G} = \frac{1}{1 + \frac{A \cdot R_A}{R_A + R_B}}$$

ANS:: $\frac{dG}{G} = \frac{1}{1+AR_A/(R_A+R_B)}$

Exercise 15.4 The circuit in Figure 15.4 is called a differential amplifier.

a) Using the ideal Op Amp model, derive an expression for the output voltage v_O in terms of v_1, v_2, R_1, R_2, R_3 and R_4.

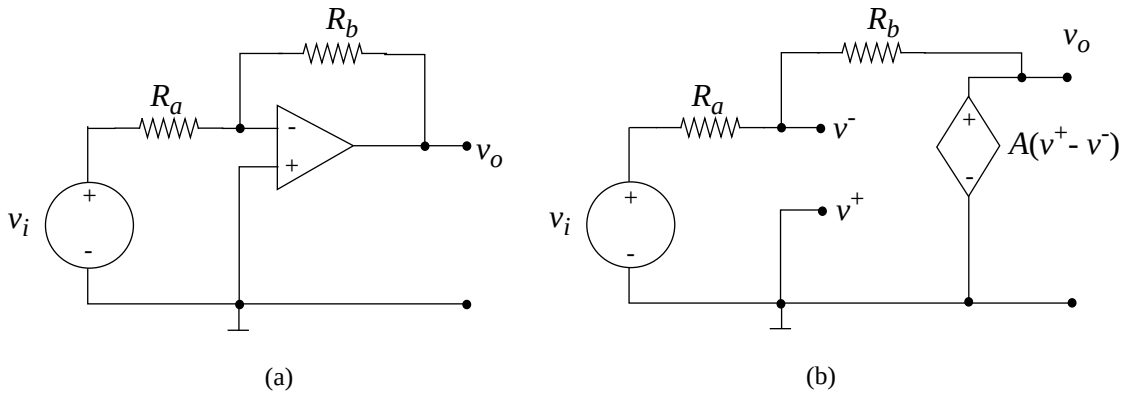


Figure 15.3: Inverting Op Amp

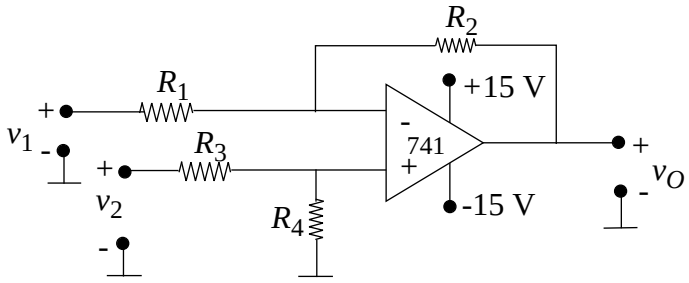


Figure 15.4:

b) Does connecting a load resistor R_L between the output and ground change the above expression for v_O? Why?

c) Let $v_1 = v_2$ and $R_1 = 1k\Omega, R_2 = 30k\Omega, R_3 = 1.5k\Omega$. Find R_4 so that $v_O = 0$.

d) Let $v_2 = 0$ and $v_1 = 1$ volt. Using the resistor values above (including that computed for R_4), find v_O.

Solution:

a) Assuming $v^+ \cong v^- = V_2 \cdot \left(\frac{R_4}{R_3+R_4}\right)$, KCL at node v^- yields:

$$\left(V_1 - \frac{V_2 R_4}{R_3 + R_4}\right)\frac{i}{R_1} + \left[V_0 - \left(\frac{V_2 R_4}{R_3 + R_4}\right)\right]\frac{1}{R_2} = 0$$

$$V_0 = \frac{(R_1 + R_2)\cdot R_4}{(R_3 + R_4)\cdot R_1} \cdot \ v_2 - \frac{R_2}{R_1} \cdot \ v_1$$

b) No. The derivation for V_0 is not affected by the addition of R_L.

c) $R_4 = 45k\Omega$

d) $V_0 = -15Volts$, since the op. amp. saturates here. V_0 cannot be more negative!

ANS:: (a) $v_O = \frac{(R_1+R_2)R_4}{(R_3+R_4)R_1}v_2 - \frac{R_2}{R_1}v_1$, (b) No, (c) $R_4 = 45k\Omega$, (d) $-15V$

Exercise 15.5 For the circuit shown in Figure 15.5, D is a silicon diode, where $i = I_S(e^{qv/nkT} - 1)$, $kT/q =$ 26mV, and n is between 1 and 2.

a) Find v_O in terms of v_1 and R_1.

b) Make a quick sketch of the answer to (a).

Solution:

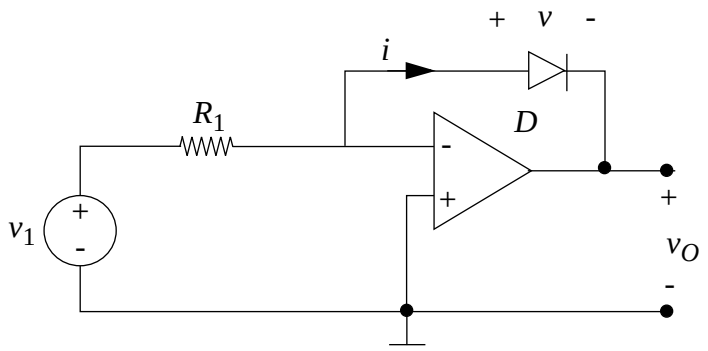


Figure 15.5:

a)

$$v_O = \frac{-n \cdot k \cdot T}{q} \cdot \ln\left(\frac{v_1}{I_s \cdot R_1} + 1\right)$$

b) See Figure 15.6.

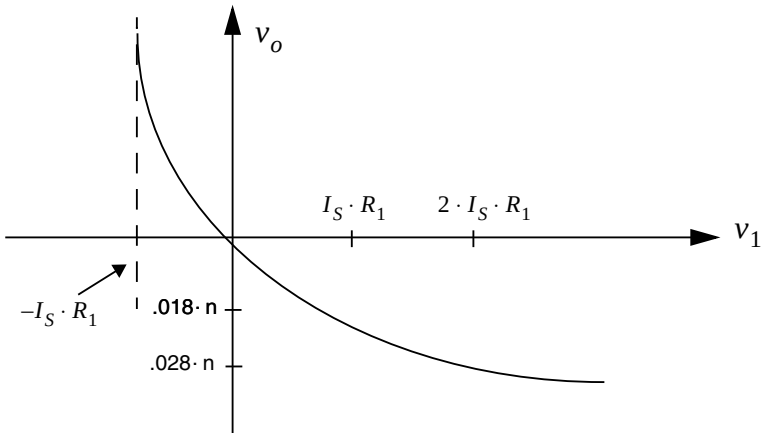


Figure 15.6:

ANS:: $v_O = \frac{-nkT}{q} ln\left(\frac{v_1}{I_S R_1} + 1\right)$

Exercise 15.6 Refer to the figure in Figure 15.7 for this problem.

$R_1 = 100k\Omega$, $R_2 = 9k\Omega$, $R_3 = 1k\Omega$.

Given that $v_S = 2cos\omega t$ (in volts), make a sketch of $v_O(t)$ through one complete cycle. Be sure to label the dimensions of the voltage and time axes and identify characteristic

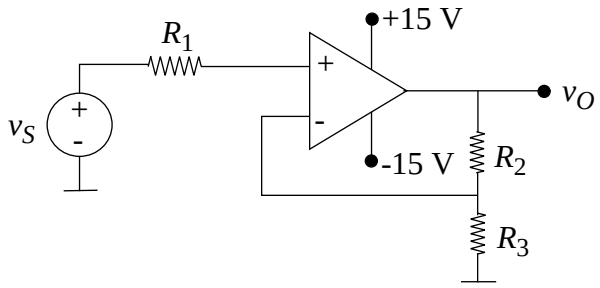


Figure 15.7:

waveform shapes with suitable expressions. (Make reasonable assumptions based on your lab experience.)

Solution:

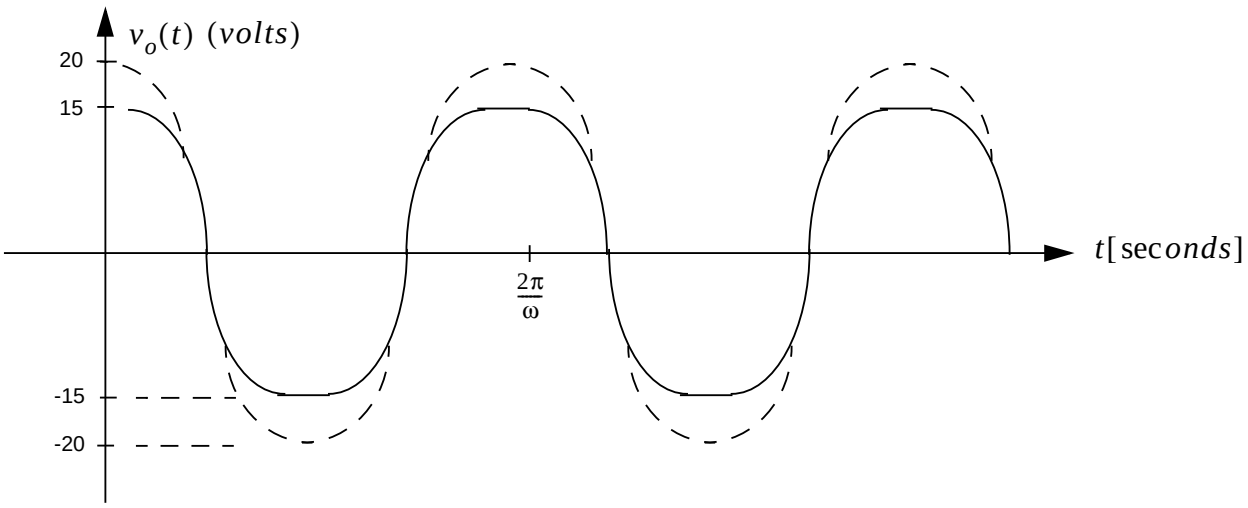


Figure 15.8:

$$v_S = V_0 \cdot \frac{R_3}{R_2 + R_3}$$

since no current flows through R_1 and $v^+ = v^- = v_S$

$v_0 = 10 \cdot v_S = 20 \cos \omega t$

ANS:: $v_0 = 10 \cdot v_S = 20 \cos \omega t$

Exercise 15.7 Refer to the figure in Figure 15.9 for this problem.

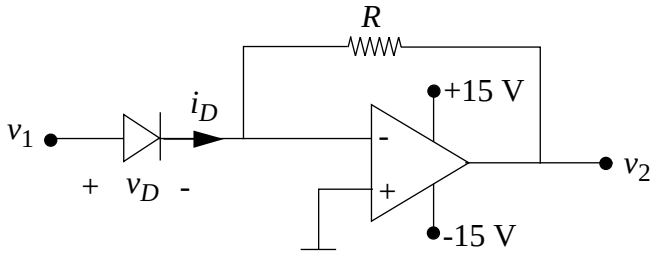


Figure 15.9:

Diode data $i_D = I_S(e^{qv_D/kt} - 1)$
where $I_S = 10^{-12}A$
and $kT/q = 25mV$

For v_1 in the range $|v_1| < .575$ volts, how should the value of R be chosen to keep the Op Amp in the linear region? Make reasonable approximations.

Solution:

Since $v^+ \cong v^- = 0$,

$$i_D = I_s\left(e^{qV_1/kT} - 1\right) = \frac{0 - V_2}{R}$$

*To stay in the linear region, $|V_2| \leq 15Volts$, or

$$R \cdot \ I_s\left(e^{qV_1/kT} - 1\right) \leq 15$$

$$V_1 < 0.575Volts$$

$$R \leq 1539\Omega$$

ANS:: $R \leq 1539\Omega$

Exercise 15.8 Find the Norton equivalent circuit to the left of terminal pair a-a' in Figure 15.10.

Solution:

$R_{TH} = 50\Omega$

$$i_a = \frac{v_a - 0}{100}$$

$$5i_a = \frac{v_a}{20}$$

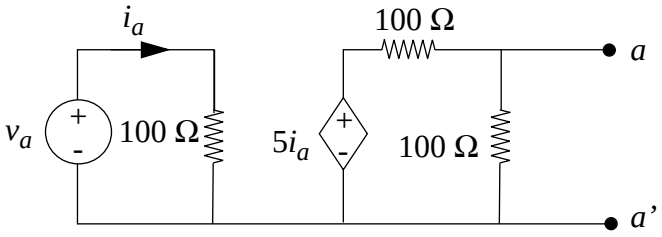


Figure 15.10:

$$I_{SC} = \frac{5i_a - 0}{100} = \frac{v_a}{2000}$$

ANS:: $R_{Th} = 50\Omega$, $I_{SC} = \frac{v_a}{2000}$

Exercise 15.9 In the circuits (a) and (b) shown in Figure 15.11 the operational amplifiers are ideal and have infinite gain. If the input to each amplifier is $v_I = 1$ volt, what is the output voltage v_O for (a) and for (b).

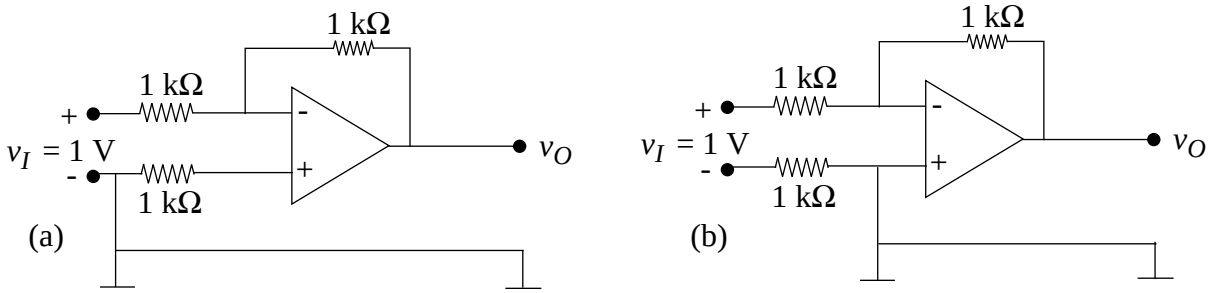


Figure 15.11:

Solution:

(a)

$v^+ \cong v^- = 0$

KCL:

$$\frac{v_I - 0}{1k\Omega} + \frac{v_O - 0}{1k\Omega} = 0$$

$$v_O = -v_I$$

(b)

KVL:

$$(1000) \cdot \ i + v_I + (1000) \cdot \ i = 0$$

$$i = \frac{-v_I}{2000} = \frac{0 - v_O}{1000}$$

$$v_O = \frac{1}{2} \cdot \ v_I$$

ANS:: (a) $v_O = -v_I$, (b) $v_O = -\frac{1}{2} v_I$

Exercise 15.10 You may assume that the operational amplifiers used in the connections shown in Figure 15.12 have very high gain and input resistance, and low output resistance when operating in the linear region.

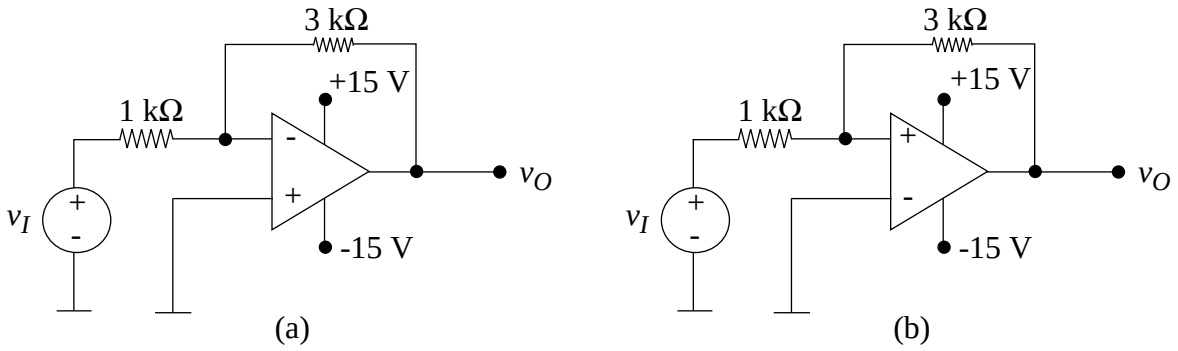


Figure 15.12:

The input signals have the form shown in Figure 15.13:

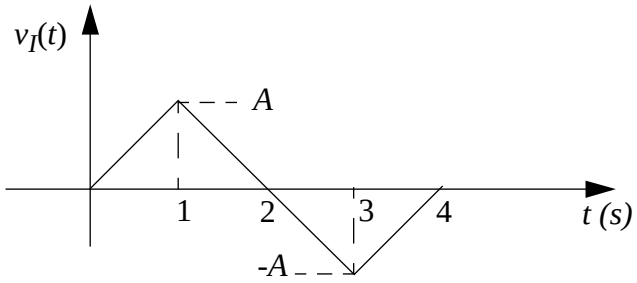


Figure 15.13:

a) Plot the output voltage v_O for the circuit of Figure 15.12a for A = 1 volt. Note: In all of your plots, be sure to clearly indicate peak values and times when signals change character abruptly.

b) Plot the output voltage v_O for the circuit of Figure 15.12a for A = 10 volts.

c) Plot the output voltage v_O for the circuit of Figure 15.12b for A = 10 volts.

Solution:

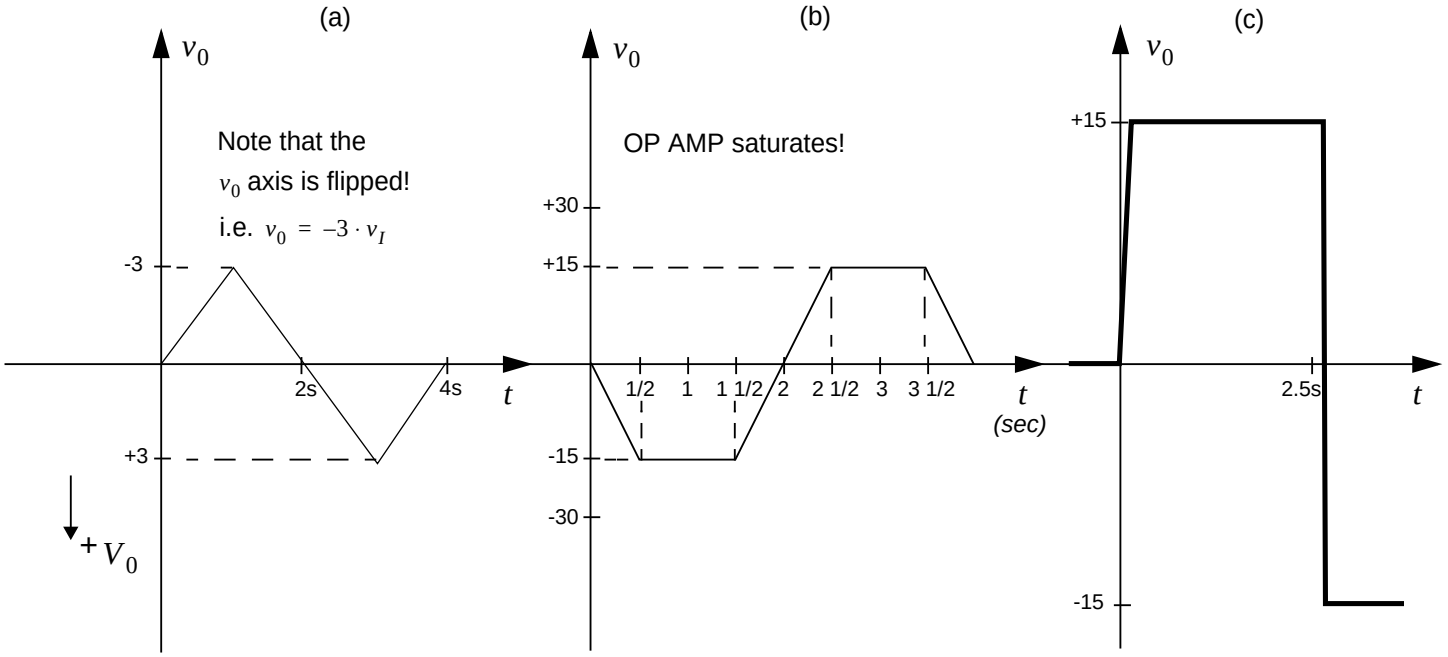


Figure 15.14:

a) See Figure 15.14

Note v_O axis is flipped!

b) See Figure 15.14

c) See Figure 15.14

Exercise 15.11 For the circuit shown in Figure 15.15 (which includes a voltage controlled voltage source) determine:

a) The input resistance v_I/i_I.

b) The Thévenin equivalent resistance at the terminals a b.

Solution:

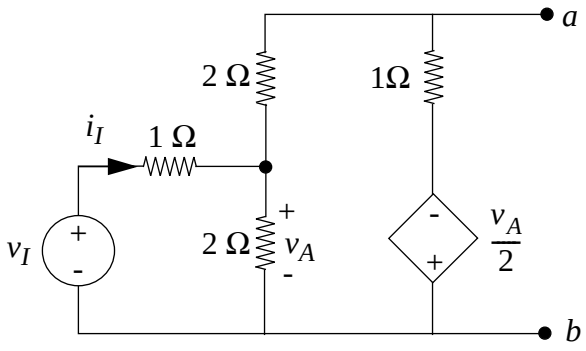


Figure 15.15:

a) KCL:

$$i_I + \frac{0 - V_A}{2} + \frac{\left(-\frac{V_A}{2} - V_A\right)}{(2+1)} = 0$$

$$i_I = V_A$$

KVL:

$$V_I - i_I(1\Omega) - V_A = 0$$

$$i_I = V_I - i_I$$

$$\frac{V_I}{i_I} = R_{INPUT} = 2\Omega$$

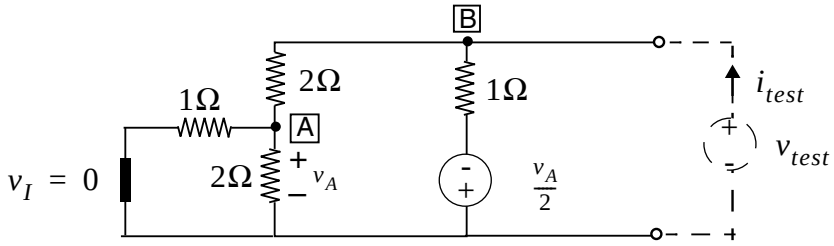


Figure 15.16:

b) Apply V_{test} at terminals $a - b$ and measure $\frac{V_{test}}{i_{test}} = R_{TH}$

KCL at A:

$$\frac{(V_{test} - V_A)}{2} + \frac{(0 - V_A)}{2} + \frac{(0 - V_A)}{1} = 0$$

$$V_A = \frac{V_{test}}{4}$$

KCL at B:

$$i_{test} + \frac{(-V_A/2 - V_{test})}{1} + \frac{(V_A - V_{test})}{2} = 0$$

$$V_A = \frac{V_{test}}{4}$$

$$\frac{V_{test}}{itest} = R_{TH} = \frac{2}{3}\Omega$$

ANS:: (a) 2Ω, (b) $2/3\Omega$

Exercise 15.12 Find and label clearly the Thévenin equivalent for the network in Figure 15.17.

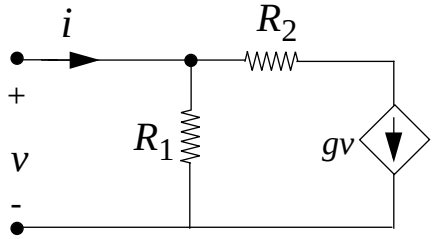


Figure 15.17:

Solution:

$$i - g \cdot\ v + \frac{0 - V}{R_1} = 0$$

$$\frac{V}{i} = R_{TH} = \frac{R_1}{1 + R_1 \cdot g}$$

$$V_{OC} = 0$$

ANS:: $R_{Th} = \frac{R_1}{1+R_1 g}$, $V_{OC} = 0$

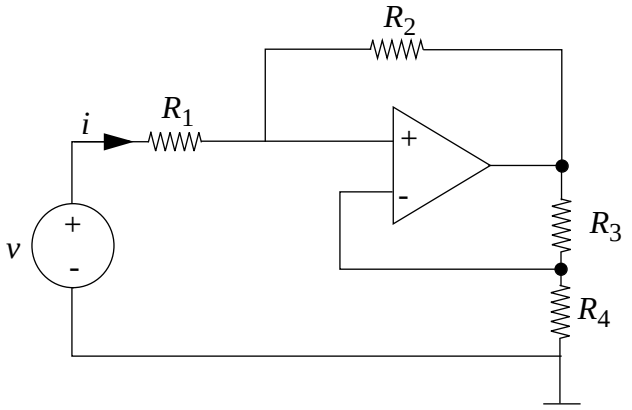


Figure 15.18:

Exercise 15.13 Find i in terms of v for the linear network in Figure 15.18. Assume an idealized operational amplifier.

Solution:

$$v^+ \cong v^- = v_0 \cdot \frac{R_4}{R_3 + R_4}$$

So,

$$v_0 = \frac{v^+(R_3 + R_4)}{R_4}$$

KCL:

$$\frac{v_0 - v^+}{R_2} + \frac{v - v^+}{R_1} = 0$$

Eliminating v_0 from the above two equations, we solve for v^+ to get

$$v^+ = v\frac{R_2 R_4}{R_2 R_4 - R_1 R_3}$$

$$i = \frac{v - v^+}{R_1} = v\frac{R_3}{R_1 R_3 - R_2 R_4}$$

ANS:: $i = v\frac{R_3}{R_1 R_3 - R_2 R_4}$

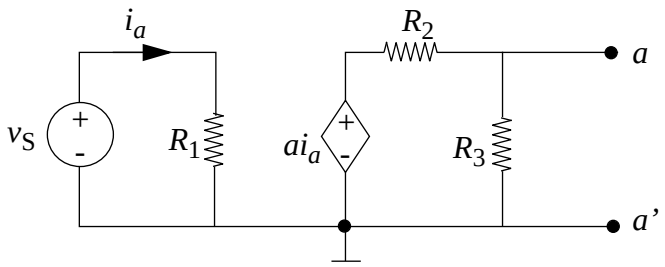


Figure 15.19:

Exercise 15.14 Determine the Thévenin equivalent for the circuit shown in Figure 15.19, to the left of terminal pair a-a'. The circuit contains a current-controlled *voltage* source.

Solution:

$$R_{TH} = \frac{R_2 R_3}{R_2 + R_3}$$

since $V_S = 0 = i_A$ in this case to find R_{TH}.

$$i_a = \frac{V_S - 0}{R_1}$$

$$V_{OC} = \alpha \; i_A \cdot \; \frac{R_3}{R_2 + R_3}$$

$$V_{OC} = \frac{v_S \cdot \alpha \;\; R_3}{R_1 \; (R_2 + R_3)}$$

ANS:: $R_{Th} = R_2 \parallel R_3, V_{OC} = \frac{v_S}{R_1} \alpha \frac{R_3}{R_2 + R_3}$

Exercise 15.15

a) Draw a circuit model for the Op Amp circuit in Figure 15.20.

b) Write the node equations for the v_a and the v^- nodes, and enough more independent relations to specify v_o in terms of v_i. Do not solve.

Solution:

a)

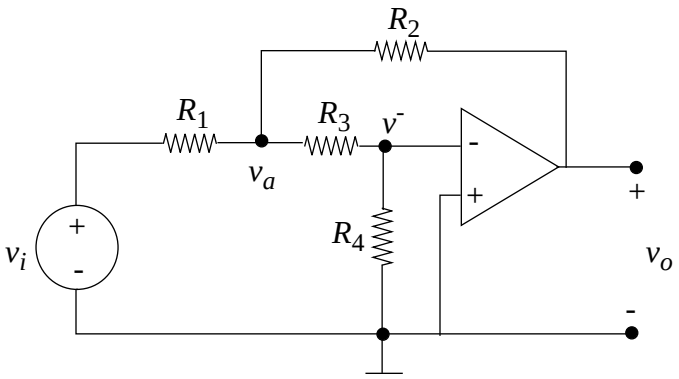


Figure 15.20:

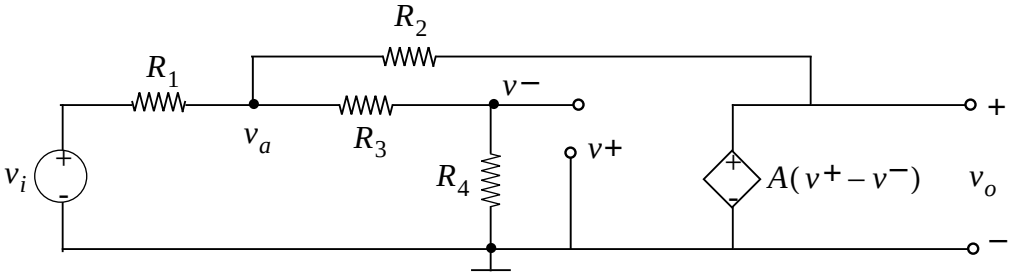


Figure 15.21:

b) (1)

$$\frac{(v_i - v_a)}{R_1} + \frac{(v^- - v_a)}{R_3} + \frac{(v_0 - v_a)}{R_2} = 0$$

(2)

$$\frac{(v_a - v^-)}{R_3} + \frac{(0 - v^-)}{R_4} = 0$$

Also: $v_0 = A(v^+ - v^-)$ and $v^+ = 0$

or, $v^+ \approx v^-$ and $v^+ = 0$

ANS:: $(v_i - v_a)g_1 + (v^- - v_a)g_3 + (v_O - v_a)g_2 = 0$ and $(v_a - v^-)g_3 + (0 - v^-)g_4 = 0$, and either $v_O = A(v^+ - v^-)$ and $v^+ = 0$, or $v^+ \approx v^-$ and $v^+ = 0$.

Exercise 15.16 For the circuit in Figure 15.22 find v_{out} as a function of v_1, v_2, R_a and R_b in the *limit of very high Op Amp gain*. Assume input resistance $r_i = \infty$, output resistance $r_t = 0$, and non-saturated operation.

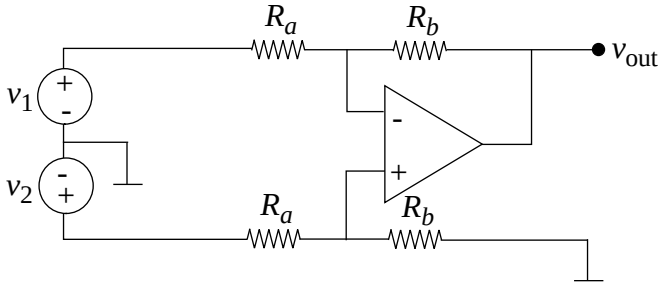


Figure 15.22:

Solution:

$$v^+ \approx v^- \approx V_2 \cdot \frac{R_b}{R_a + R_b}$$

$$\frac{V_1 - v^-}{R_a} + \frac{v_{out} - v^-}{R_b} = 0$$

$$v_{out} = \frac{R_b}{R_a}(v_2 - v_1)$$

ANS:: $v_{out} = \frac{R_b}{R_a}(v_2 - v_1)$

Exercise 15.17 For the circuit in Figure 15.23 find i_1 as a function of v_i, R_1, R_2 and the Op Amp gain A. Assume input resistance $r_i = \infty$, output resistance $r_t = 0$ and non-saturated operations.

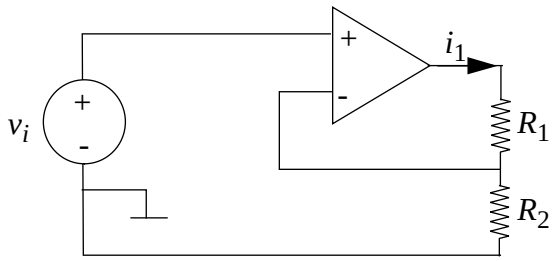


Figure 15.23:

Solution:

$$v^+ \approx v^- \approx v_i$$

$$\frac{v_0}{R_1 + R_2} = i_1$$

$$i_1 = \frac{v_i}{R_2}$$

assuming A is infinite.

$$v_i = \frac{R_2}{R_1 + R_2} \cdot v_0$$

With A finite,

$$i_1 = \frac{A(v^+ - v^-)}{R_1 + R_2}$$

$$v^+ = v_i$$

$$v^- = A(v^+ - v^-)\frac{R_2}{R_1 + R_2}$$

Therefore,

$$v^- = \frac{A \cdot v_i \cdot R_2}{R_1 + R_2 + AR_2}$$

$$i_1 = \frac{A \cdot v_i}{R_1 + (1 + A)R_2}$$

Note: limit as $A \to \infty$ checks with the above answer.

ANS:: $i_1 = \frac{A}{R_1 + (1+A)R_2} v_i$

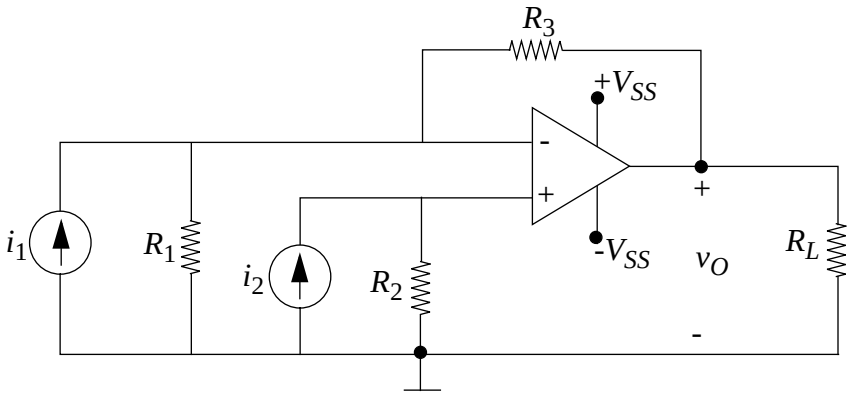


Figure 15.24:

Exercise 15.18 Consider the circuit illustrated in Figure 15.24.

Assume that the operational amplifier is ideal with input resistance r_i very large and output resistance r_t negligibly small, so that $i^+ \simeq 0, i^- \simeq 0$, and $v_O = A(v^+ - v^-)$, with A very large. Assume it is operating in its linear range.

a) Draw a linear equivalent circuit for this circuit valid for operation with the Op Amp in its linear range.

b) Derive an expression for v_O as a function of i_1, i_2, and the resistors in the circuit.

Solution:

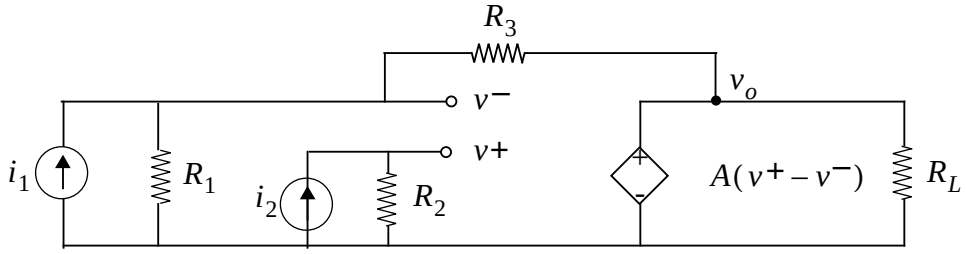


Figure 15.25:

a)

b) $v^+ \cong v^- = i_2 \cdot R_2$

KCL:

$$i_1 + \frac{(0 - i_2 R_2)}{R_1} + (v_0 - i_2 R_2) R_3 = 0$$

$$v_0 = -i_1 R_3 + i_2 \left[\frac{R_2(R_1 + R_3)}{R_1} \right]$$

ANS:: $v_0 = -i_1 R_3 + i_2 \left[\frac{R_2(R_1+R_3)}{R_1} \right]$

Exercise 15.19 In the circuit in Figure 15.26 determine the voltage gain $G = v_o/v_i$:

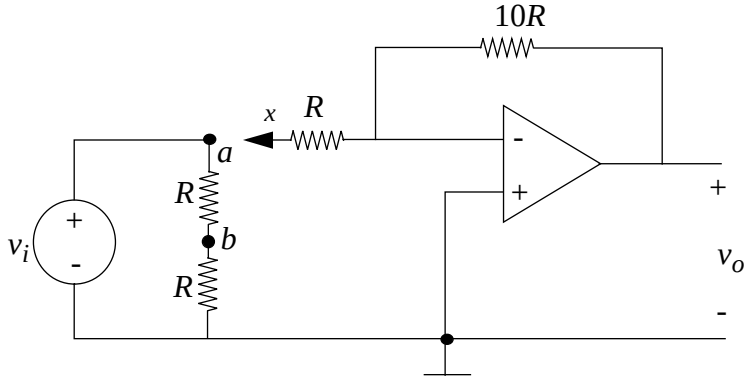


Figure 15.26:

a) when terminal x is connected to terminal a.

b) when terminal x is connected to terminal b. Assume the Op Amp is ideal.

Solution:

a)

$$\frac{(v_i - 0)}{R} + \frac{(v_0 - 0)}{10R} = 0$$

since $v^+ \cong v^- = 0$

$$G = \frac{v_0}{v_i} = -10$$

b) Since $v^+ \approx v^- \approx 0$,

$$e_1 = \frac{v - i \cdot R \,||\, R}{R + R \,||\, R}$$

$$R \,||\, R = R/2$$

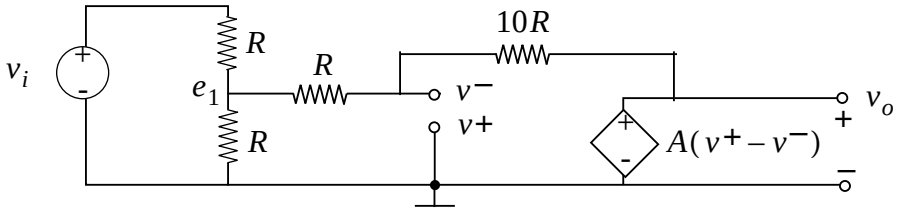


Figure 15.27:

$$e_1 = v_i/3$$

KCL:

$$\frac{\frac{v_i}{3} - 0}{R} + \frac{v_0 - 0}{10R} = 0$$

$$G = \frac{v_0}{v_i} = -\frac{10}{3}$$

ANS:: (a) $v_o = -10v_i$, (b) $v_o = -\frac{10}{3}v_i$

Exercise 15.20 For the amplifier shown in Figure 15.28, find the current transfer ratio i_o/i_s. Assume that the Op Amp is ideal.

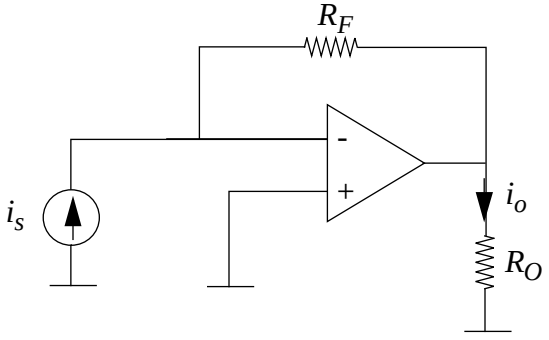


Figure 15.28:

Solution:

At node $v^- \cong v^+ \approx 0$,

KCL:

$$i_s + \frac{(i_o R_0 - 0)}{R_F} = 0$$

$$\frac{i_o}{i_s} = -\frac{R_F}{R_0}$$

ANS:: $i_o = -i_s \frac{R_F}{R_O}$

Exercise 15.21 Find the Theévenin output resistance of the circuit shown in Figure 15.29. That is, find the resistance seen looking in at the terminals X X, the terminals that drive the load resistance R_L. (Resistor R_L should not be included when you make this calculation.) DO NOT assume $v^+ \simeq v^-$, as it leads to trouble here. Now state a condition on the value of R_S to ensure that the circuit acts as a current source driving R_L.

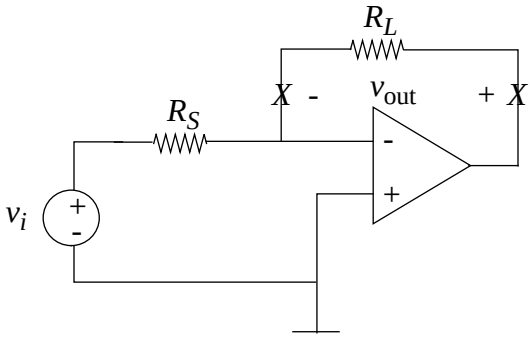


Figure 15.29:

Solution:

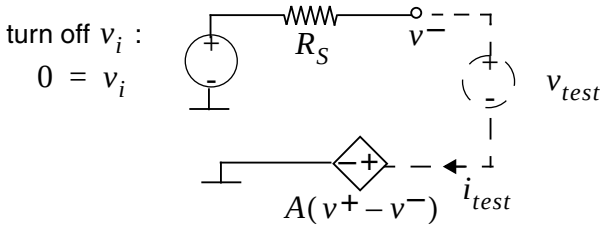


Figure 15.30:

Apply V_{test} and measure $\frac{V_{test}}{i_{test}} = R_{TH}$:

$$v^- = -v_{test} + A(v^+ - v^-)$$

$$v^+ = 0$$

$$* \quad v^-(1 + A) = -v_{test}$$

Therefore,

$$v^- = \frac{-v_{test}}{(1+A)}$$

$$i_{test} = \frac{0 - v^-}{R_s} = \frac{v_{test}}{(1+A)R_s}$$

$$\frac{v_{test}}{i_{test}} = (1+A)\, R_s = R_{TH}$$

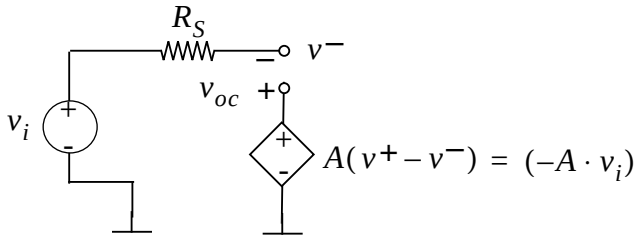


Figure 15.31:

Now find V_{OC}:

$v^- = v_i$, since no current flows through R_S

$$V_{OC} = -Av_i - v_i$$

$$V_{OC} = -v_i(A+1)$$

Now connect R_L to the Thévenin Equivalent of the circuit:

*I is current driving R_L:

$$I = \frac{-v_i(1+A)}{R_S(1+A) + R_L}$$

For the circuit to act as current source (i.e. current is constant regardless of R_L),

$$R_S(1+A) \gg R_L$$

ANS:: $R_{TH} = (1+A)\, R_S$,

$$R_S(1+A) \gg R_L$$

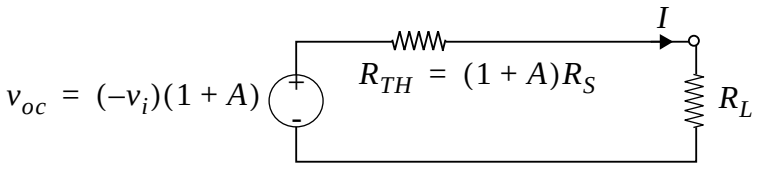


Figure 15.32:

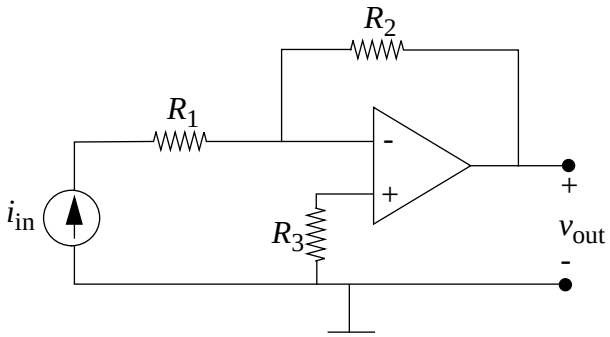


Figure 15.33:

Exercise 15.22 For the Op Amp circuit in Figure 15.33:

a) Assume that the Op Amp is ideal (very large gain A, zero output resistance, infinite input resistance, operating in the linear region) and find v_{out} as a function of i_{in}, R_1, R_2 and R_3.

b) Draw the circuit model, assuming the Op Amp has finite A, keeping the other assumptions from a).

c) Analyze the circuit and find an expression for v_{out} as a function of i_{in}, R_1, R_2 and R_3 and (finite) A.

Solution:

a) $v_{out} = -i_{IN} \cdot R_2$ since no current flows through R_3

b) Circuit model:

c) KCL:

$$i_{in} + \frac{A(v^+ - v^-) - v^-}{R_2} = 0$$

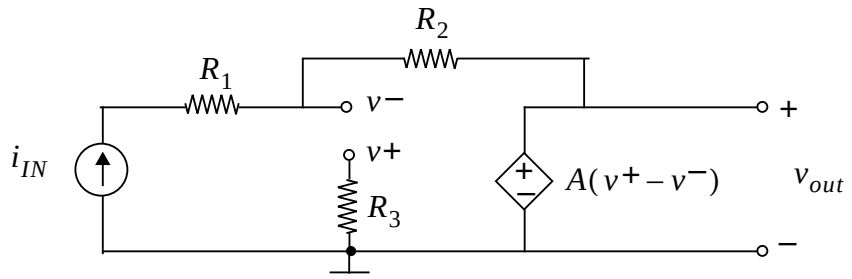


Figure 15.34:

$$v^+ = 0$$

Therefore,

$$v^- = \frac{i_{in} \cdot R_2}{1+A}$$

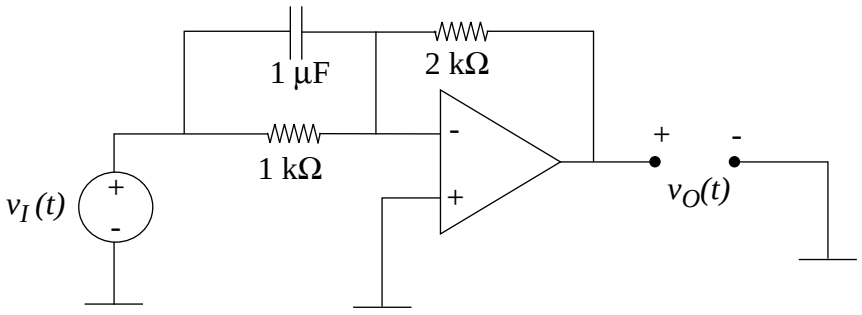
$$v_{out} = A(v^+ - v^-) = -Av^-$$

$$v_{out} = \frac{-A\ i_{in} \cdot R_2}{1+A}$$

Note: The answer in (c) checks with the answer in (a) in the limit as $A \to \infty$.

ANS:: (a) $v_{out} = -i_{in}R_2$, (c) $v_{out} = \frac{-Ai_{in}R_2}{1+A}$

Exercise 15.23 The operational amplifier circuit shown in Figure 15.35 is driven with a ramp:



$$v_I(t) = 0, \quad t < 0$$

$$v_I(t) = 10^3\ s^{-1}\ t\ \text{V}, \quad t < 0$$

Figure 15.35:

You may assume that the operational amplifier has infinite open-loop gain, zero output resistance, and infinite input resistance, and that the capacitor voltage is zero for $t < 0$. What are the value of $v_O(t)$ at $t = 0^+$ and $t = 1ms$?

Solution:

KCL at node v^-:

$$\frac{v_I(t) - 0}{1000} + C\frac{dv_I(t)}{dt} + \frac{v_0(t) - 0}{2000} = 0, \text{ since } v^- = v^+ = 0$$

$$\text{Therefore, } \; v_I(t) = 1000t, \; \frac{dv_I(t)}{dt} = 1000, \text{ so}$$

$$v_0(t) = -2000 \cdot t - 2 \; [volts]$$

$v_0(t = 0^+) = -2Volts$

$v_0(t = 1ms) = -4Volts$

ANS:: $v_0(t = 0^+) = -2Volts$ and $v_0(t = 1ms) = -4$ Volts

Exercise 15.24 An operational amplifier is connected as shown in Figure 15.36.

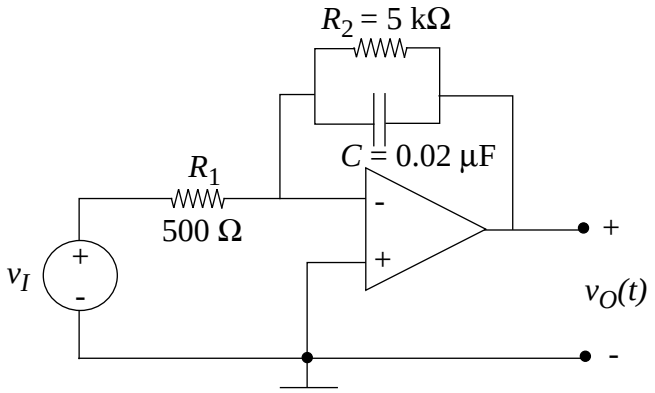


Figure 15.36:

a) What is the gain of the amplifier for $\omega = 0$.

b) Find the expression for $V_o(j\omega)/V_i(j\omega)$.

c) At what frequency does $|V_o|$ fall to 0.707 of its low-frequency value?

Solution:

a) The input is in the form of $Ae^{j\omega t}$. When $\omega = 0$, the input is a DC signal A.
For DC inputs, we may treat the capacitor as an open circuit:

$$\frac{v_i}{500} + \frac{v_o}{5000} = 0$$

$$\frac{v_o}{v_i} = -10$$

b)

$$\frac{V_o}{V_i} = \frac{-R_2 \,||\, \frac{1}{Cs}}{R_1}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{R_2}{R_1(j\omega R_2 C + 1)}$$

c) $|V_o|$ has the low frequency value of $\frac{R_2}{R_1}$, so ω_{cutoff} is such that

$$0.707\frac{R_2}{R_1} = |\frac{R_2}{R_1(j\omega R_2 C + 1)}|$$

$$\sqrt{2} = \sqrt{(\omega R_2 C)^2 + 1}$$

$$\omega_{cutoff} = \frac{1}{R_2 C}$$

ANS:: (a) $\frac{v_o}{v_i} = -10$, (b) $\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{R_2}{R_1(j\omega R_2 C+1)}$, (c) $\omega_{cutoff} = \frac{1}{R_2 C}$

Exercise 15.25 For the circuit shown above, determine $V_{out}(s)$ in terms of $V_{in}(s)$.

Solution:

In general if we have the set-up shown in the figure,

we know from voltage dividers that

$$V_2 = \frac{Z_1}{Z_1 + Z_2} \cdot V_T$$

$$V_1 = \frac{Z_2}{Z_1 + Z_2} \cdot V_T$$

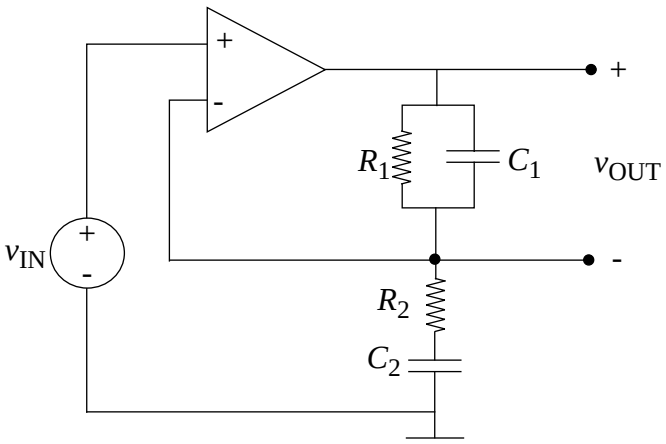


Figure 15.37:

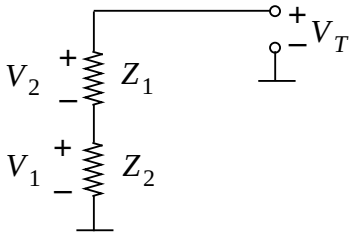


Figure 15.38:

Therefore

$$V_T = \frac{Z_1 + Z_2}{Z_1} V_2 = \frac{Z_1 + Z_2}{Z_2} V_1$$

So we may conclude here that

$$V_2 = \frac{Z_1}{Z_2} V_1$$

In this problem

$$Z_1 = \frac{\frac{R_1}{C_1 s}}{R_1 + \frac{1}{C_1 s}} = \frac{R_1}{R_1 C_1 s + 1}$$

$$Z_2 = R_2 + \frac{1}{C_2 s} = \frac{R_2 C_2 s + 1}{C_2 s}$$

and $V_{out} =$ "V_2'' above and $V_{in} =$ "V_1'' above.

Therefore,

$$V_{out} = \frac{R_1 C_2 s}{(R_1 C_1 s + 1)(R_2 C_2 s + 1)} \cdot V_{in}$$

since

$$V_{out} = \frac{Z_1}{Z_2} V_{in}$$

ANS:: $V_{out} = \frac{R_1 C_2 s}{(R_1 C_1 s + 1)(R_2 C_2 s + 1)} \cdot V_{in}$

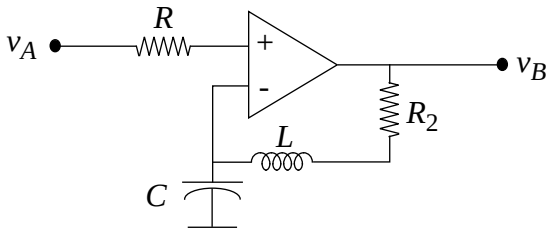


Figure 15.39:

Exercise 15.26 $R_1 = R_2 = 20\Omega \quad C = 2.4\mu F \quad L = 0.25mH$

Find the system function $H(s) = V_b/V_a$ for the circuit in Figure 15.39.

Solution:

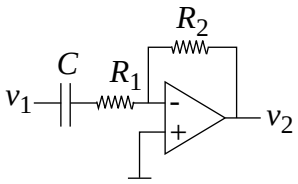
$$H(s) = \frac{V_b}{V_a} = LC\left(s^2 + \frac{R_2}{L}s + \frac{1}{LC}\right)$$

$v^+ = v^- = v_A$ since no current flows through R_1

ANS:: $H(s) = LC\left(s^2 + \frac{R_2}{L}s + \frac{1}{LC}\right)$

Exercise 15.27 For the circuit shown in Figure 15.40, select the magnitude of the frequency response for the system function given. It is not necessary to relate the critical frequencies to the circuit parameters.

Please note that the magnitude responses, except (7), are sketched on a log-log scale, with slopes labeled.



$$H(j\omega) = \frac{V_2(j\omega)}{V_1(j\omega)}$$

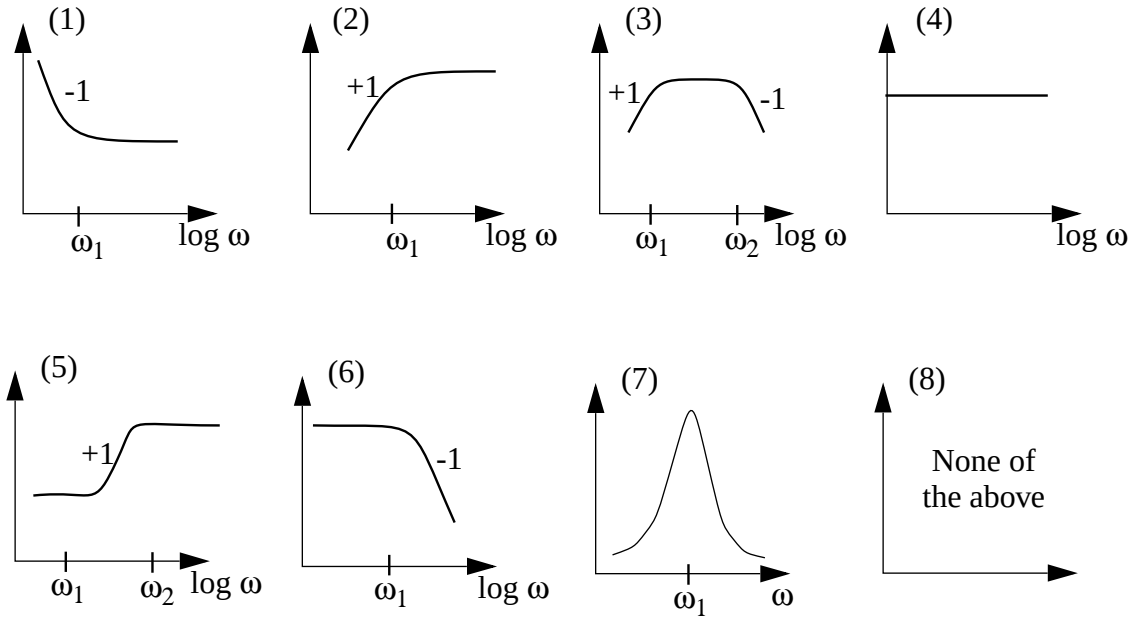


Figure 15.40:

Solution:

(2)

ANS:: (2)

Problems

Problem 15.1 The circuit shown in Figure 15.41 is very similar to the standard non-inverting Op Amp except that R_L is some external resistor, and we are interested in showing that the current through R_L is nearly constant, regardless of the value of R_L, that is, the circuit acts like a *current source* for driving R_L.

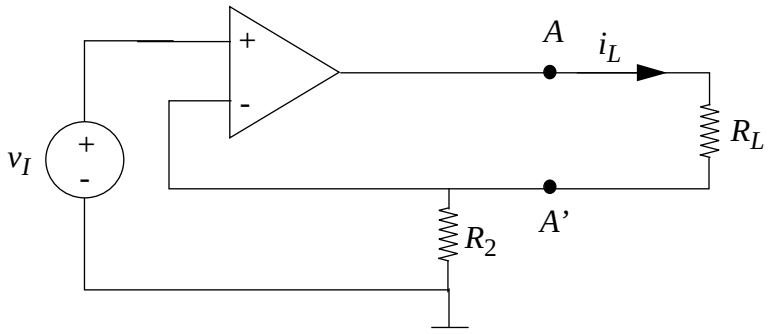


Figure 15.41:

a) Using the ideal Op Amp assumption of large gain, zero output resistance, infinite input resistance, show that the expression for i_L as a function of v_I is independent (or weakly dependent) on R_L.

b) To verify the "current source" action more directly, find the Thévenin equivalent resistance looking to the left of terminals AA', with R_L an open circuit.

Solution:

a) See Figure 15.42.

$i_L = \frac{v_O - i_L R_2}{R_L}$

$v_O = A(v_I - i_L R_2)$

$i_L R_L = A(v_I - i_L R_2) - i_L R_2$

$i_L = \frac{A v_I}{AR_2 + R_2 + R_L} \approx \frac{v_I}{R_2}$ ANS:: $i_L = \frac{A v_I}{AR_2 + R_2 + R_L} \approx \frac{v_I}{R_2}$

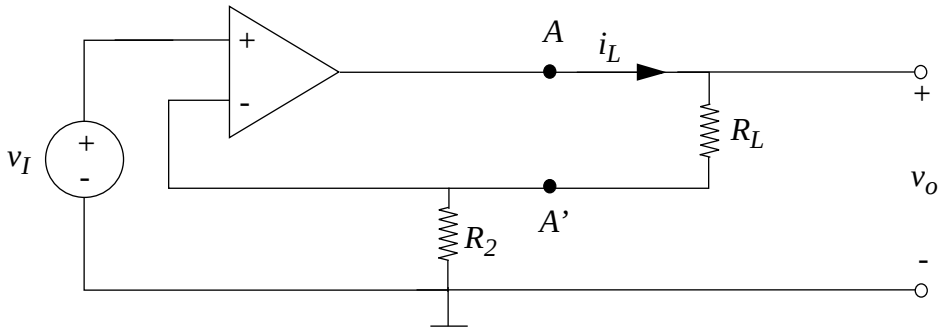


Figure 15.42:

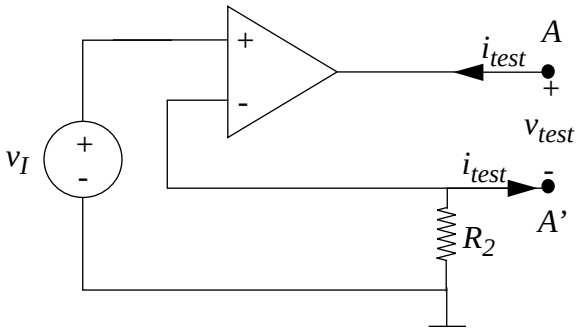


Figure 15.43:

b) See Figure 15.43.

$v_{TEST} = A(v_I + i_{TEST}R_2)$

Set independent sources to zero: $v_I = 0$

$v_{TEST} = Ai_{TEST}R_2$

$\frac{v_{TEST}}{i_{TEST}} = AR_2 = R_{THEVENIN}$ ANS:: AR_2

Problem 15.2 Zener diodes are most often used to establish stable reference voltages, independent of power supply variations, and independent of any lingering AC signals that may be present in the power supply.

a) For the characteristics shown in Figure 15.44, find v_O assuming v_A is a clean DC voltage of value $15V$.

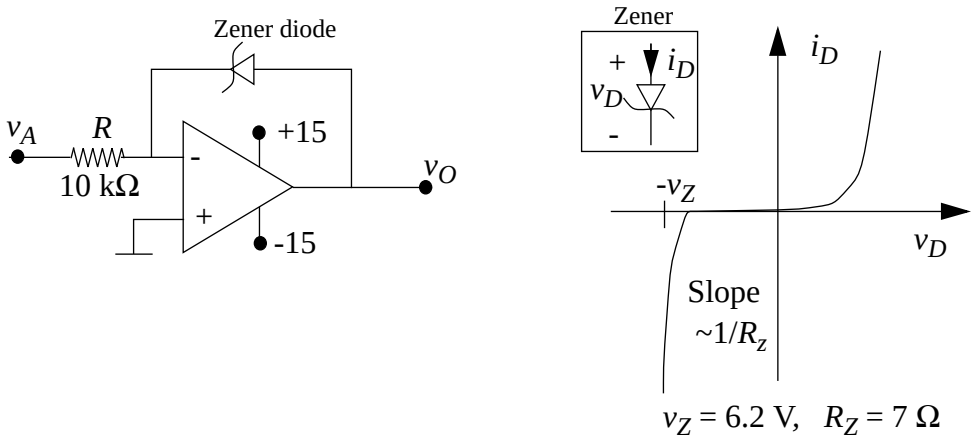


Figure 15.44:

b) Determine the sensitivity of v_O to changes in v_A. That is, find dv_O/dv_A. If v_A has $0.1V$ of DC drift or so of $120Hz$ AC ripple, how much drift or ripple shows up on v_O?

Solution:

a) $i_D = \frac{-v_A}{10k\Omega} = -1.5mA$ from graph: $v_O \approx -6.2V$

b) small signal model of diode is resistor $r = 7\Omega$

$\frac{dv_O}{dv_A} = \frac{-7}{10000}$

ripple is reduced to $7 \times 10^{-5}V$

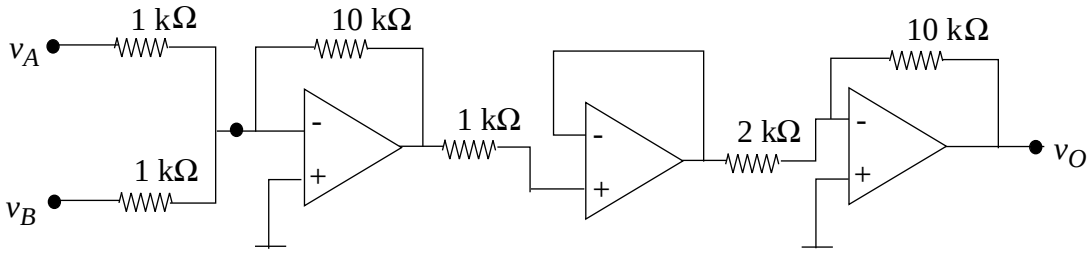


Figure 15.45: $v_A = 0.1V$ and $v_B = 0.2V$

ANS:: (a) $v_O \approx -6.2V$ (b) ripple is reduced to $\frac{7}{10000}$ of original value.

Problem 15.3 Consider the circuit in Figure 15.45.

Find v_O assuming that all Op Amps are ideal and operating in the linear region.

Solution:

$v_O = -5 \times (\frac{v_A}{1k\Omega} + \frac{v_A}{1k\Omega}) \times -10k\Omega$

$v_O = 50 \times (v_A + v_B) = 15$ volts

ANS:: 15 volts

Problem 15.4 You are faced with the problem of constructing a current transmitter, a circuit that forces a load current i_L into a load under accurate control of a source voltage v_S, independent of variations in load resistance. That is, you need a voltage-controlled current source.

The design requirements for your problem are to achieve

$$i_L = -Kv_S$$

where $K = 10mA/V$ for the ranges $|v_S| < 1V, R_L < 1k\Omega$.

While looking through a handbook of practical circuits, you come across the schematic in Figure 15.46 as a proposed solution to your problem. The question is, will it work?

a) As a first step, analyze the basic principle of operation of the above circuit. Show explicitly whether it is capable of performing the desired function.

b) Next, determine whether there will be any problems in selecting resistor values R_1 and R_2 to meet the specifications for your particular application. You should draw on experience with Op Amp limitations. Can you meet the specs?

NOTE: Part a) is easy. Part b) is endless, so look only for the *larger* issues, i.e., major sources of error or failure.

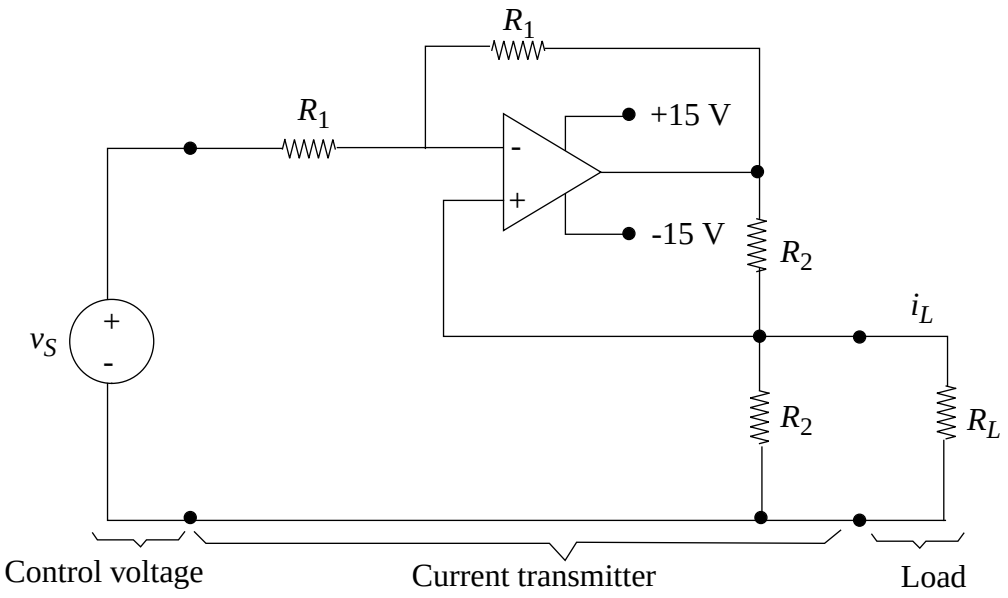


Figure 15.46:

Solution:

a) See Figure 15.47.

$i_L R_L = v^+$

$\frac{v^+}{R_2} = i_3 = \frac{i_L R_L}{R_2}$

$i_2 = i_L(1 + \frac{R_L}{R_2})$

$i_L R_L + i_2 R_2 = v_O$

$\frac{v_S - v^+}{R_1} = \frac{v^+ - v_O}{R_1}$

$i_L = \frac{-v_S}{R_2}$

b) Since $K = 10mA/V$, we must set $R_2 = 100\Omega$.

However, for the worst case ($v_S = 1V and R_L = 1k\Omega$), $v_O = 20V$. This will not work since the opamp can only output $\pm 15V$.

ANS:: (a) $i_L = \frac{-v_S}{R_2}$

Problem 15.5 Find the Norton equivalent of the circuit in Figure 15.48 looking into terminals A and A'.

Solution:

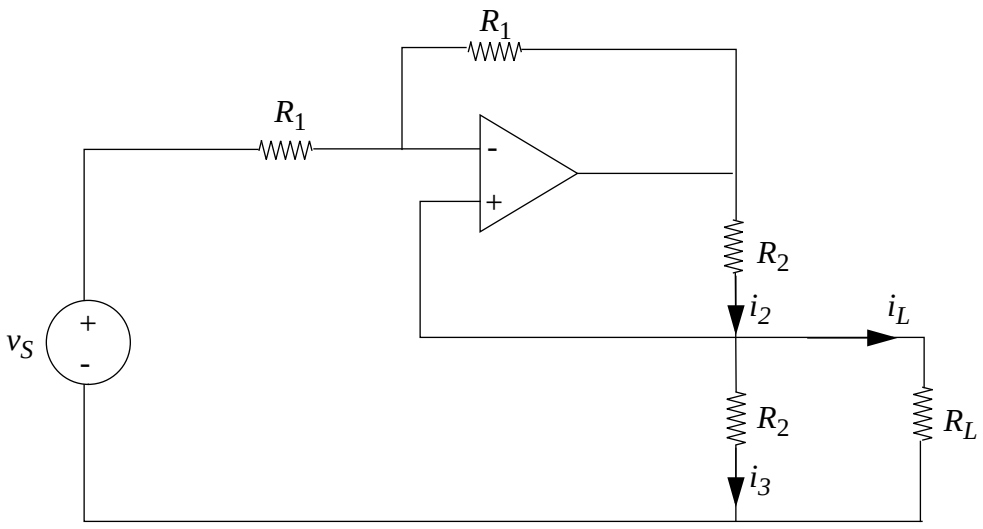


Figure 15.47:

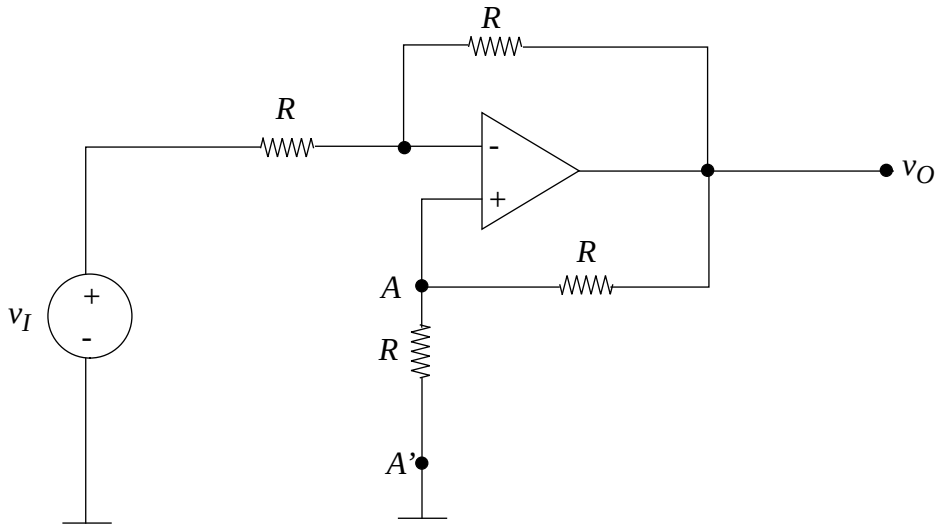


Figure 15.48:

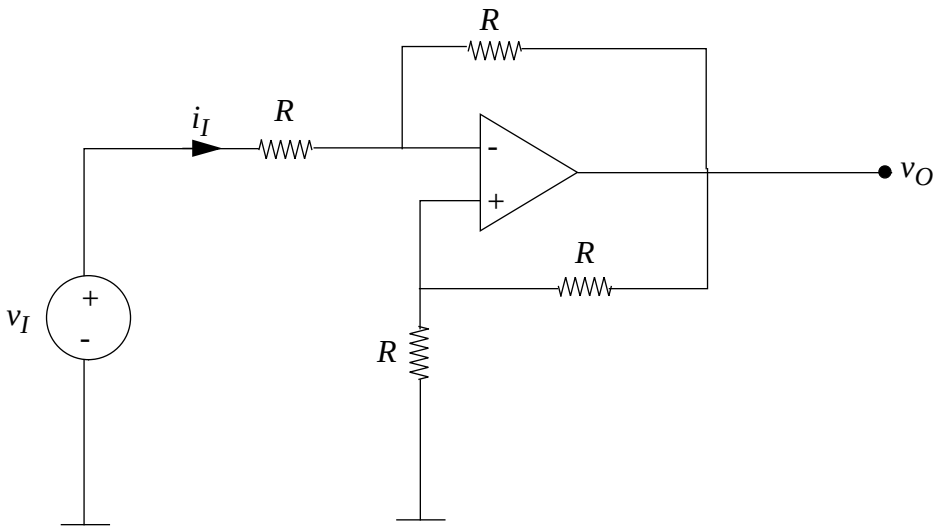


Figure 15.49:

See Figure 15.49.

$v^+ = v^- = v$

$i_I = \frac{v_I - v}{R}$

$v_O = v - i_I R = 2v - v_I$

$i = \frac{v - v_O}{R} = \frac{v_I - v}{R}$

$v_{OC} = v|_{i=0} = v_I$

$i_{SC} = i|_{v=0} = \frac{v_I}{R}$

$R_{TH} = \frac{v_{OC}}{i_{SC}} = R$

ANS:: $i_N = \frac{v_I}{R}, R_{TH} = R$

Problem 15.6 You are asked to design the circuit shown in Figure 15.50 so that the output voltage v_O is the weighted sum of v_1 and v_2; specifically.

$$v_O = 3v_1 + 5v_2$$

It is known that the magnitudes of v_1 and v_2 are never larger than 1 volt.

a) Determine the values for R_1, R_2, R_a, and R_b that will make the circuit perform that sum.

b) Given that the op amp is powered from $+15$ and -15 volts, and has output current limits of $+1mA$ and $-1mA$, redesign if necessary to meet these additional design constraints.

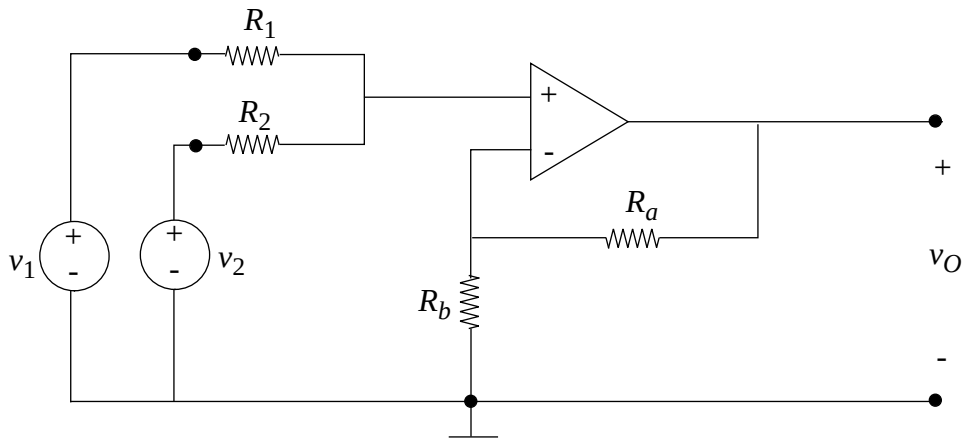


Figure 15.50:

c) How would you change the design to perform the sum:

$$v_O = -3v_1 - 5v_2$$

using only one Op Amp (given Figure 15.50, a two-op amp design is obviously trivial, but unnecessarily complicated).

Solution:

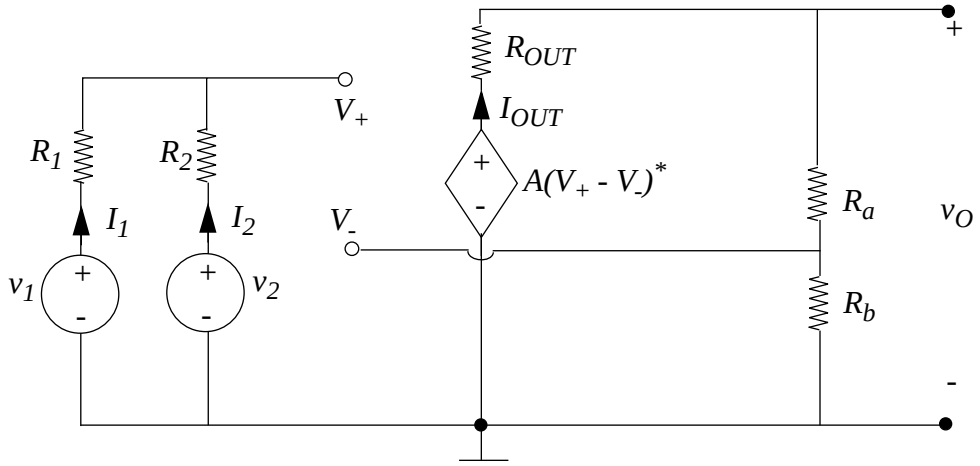


Figure 15.51:

First, draw the op-amp as a voltage-controlled voltage source, as shown in Figure 15.51. Then, find v^+, and from there find v^- and $v_{\rm OUT}$.

$$v_1 - i_1 R_1 = v_2 - i_2 R_2 = v^+.$$

$$i_1 = -i_2.$$

From here, one can eliminate i_1 and i_2, and solve for V^+, getting that

$$v^+ = \frac{v_1 R_2 + v_2 R_1}{R_1 + R_2}.$$

To find v^- and v_{OUT}, use the following voltage divider relations:

$$v_{OUT} = v_{AMP} \frac{r_A + r_B}{r_{OUT} + r_A + r_B}.$$

Then a voltage divider relationship:

$$v^- = v_{OUT} \frac{r_B}{r_{OUT} + r_A + r_B}.$$

To find v_{AMP}, use the definition of the operational amplifier:

$$v_{AMP} = A(v^+ - v^-).$$

We have expressions for v^+ and v^-, so plug in and solve for v_{AMP}, and then use the voltage divider to get the following:

$$v_{OUT} = \frac{A(R_A + R_B)(v_1 R_2 + v_2 R_1)}{(R_1 + R_2)(R_{OUT} + R_A + [A+1]R_B)}.$$

a) Assuming the op-amp is ideal, A is so high that any non-A terms can be omitted, and $R_{OUT} = 0$.

$$v_{OUT} = \frac{(R_A + R_B)(V_1 R_2 + V_2 R_1)}{(R_1 + R_2) R_B}.$$

We want to satisfy the following two criteria:

$$\frac{R_A + R_B}{R_B} \frac{R_2}{R_1 + R_2} = 3.$$

$$\frac{R_A + R_B}{R_B} \frac{R_1}{R_1 + R_2} = 5.$$

Anticipating the next parts, we choose values in a careful manner. The worst possible scenario for possible voltage or current overload is when $V_1 = 1$ and $V_2 = 1$. The following limiting situations occur.

$$\frac{1V(R_A + R_B)(R_1 + R_2)}{(R_1 + R_2)R_B} < 15V.$$

$$\frac{1V}{R_B} < 1mA.$$

This implies that $R_B > 1k\Omega$. Choose $1.5k\Omega$ for a healthy margin.

From dividing the other two equations, we get that $\frac{R_2}{R_1} = \frac{3}{5}$.

Using standard values, choose $R_2 = 4.114k\Omega$ (Use $4.7k\Omega||33k\Omega$) and $R_1 = 6.8k\Omega$. This gives a ratio of .60500, which is well within tolerance.

Solving further, we find that

$$\frac{R_A + R_B}{R_B} = 8.$$

This is well within tolerance. This also implies that $\frac{R_A}{R_B} = 7$, which means that $R_A = 10.5k\Omega$, which can be approximated quite well by $10k\Omega + 470\Omega$ in series.

b) Of course it meets the constraints - part A was done specifically with that in mind.

c) We need an inverting configuration, so start by grounding the positive terminal. Set up the configuration that is shown in Figure 15.52. If the op-amp is ideal, then $v_X = 0$. Use the following two node equations:

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} = i_{OUT}.$$

$$v_{OUT} = -R_X(\frac{v_1}{R_1} + \frac{v_2}{R_2}).$$

This implies that we need to set $\frac{R_X}{R_1} = 3$ and $\frac{R_X}{R_2} = 5$.

Let $R_X = 10k\Omega$. This allows us to set $R_1 = 3.3k\Omega$ with very small error, and $R_2 = 2k\Omega$, which can easily be attained either as $1k\Omega + 1k\Omega$ or $2.2k\Omega||22k\Omega$.

ANS:: (a) $R_1 = 6.8k\Omega, R_2 = 4.7k\Omega||33k\Omega, R_A = 10k\Omega + 470\Omega, R_B = 1.5k\Omega,$ c) $R_X = 10k\Omega, R_1 = 3.3k\Omega, R_2 = 1k\Omega + 1k\Omega.$

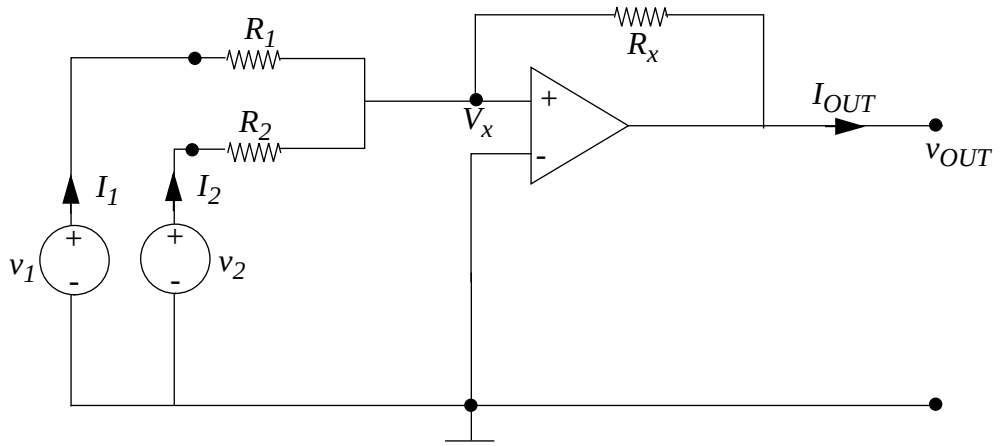


Figure 15.52:

Problem 15.7 For the circuit in Figure 15.53, assuming an ideal Op Amp with large A,

a) Calculate v_O in terms of v_I and the resistor values.

b) Find i in terms of v_I and the resistor values.

c) For what resistor values in a) will the voltage gain become infinite? Explain why this occurs (one sentence).

d) Find the limits on the solutions in the a) and b) imposed by using a real Op Amp.

Solution:

The best way to do the problem is to deal with a non-ideal op-amp, with finite gain and nonzero output resistance, so that part D may be analyzed correctly.

See the voltage-source model in Figure 15.54.

Four equations to start out with are:

$$i_1 + i_2 + i_3 = 0.$$

$$v^+ = \frac{R_1 v_{OUT} + R_2 v_{IN}}{R_1 + R_2}.$$

$$v^- = \frac{R_4 v_{OUT}}{R_3 + R_4}.$$

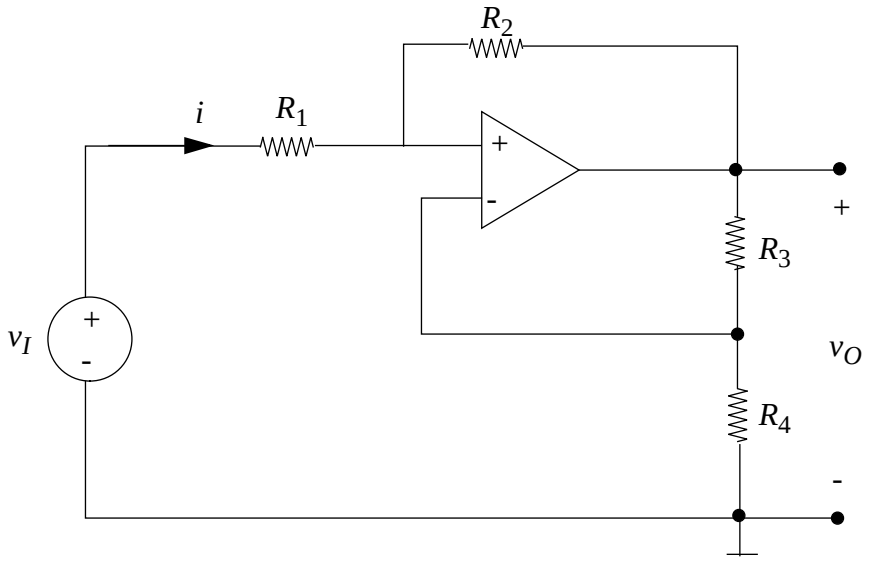


Figure 15.53:

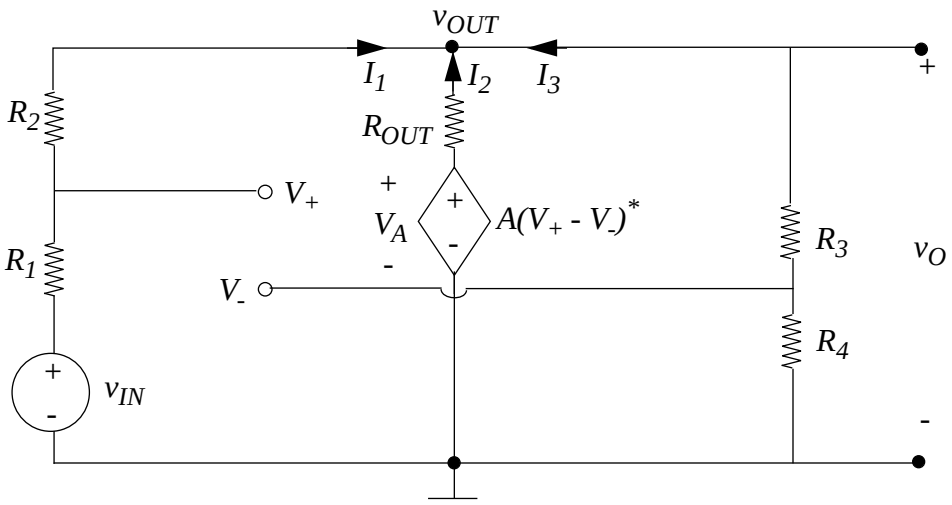


Figure 15.54:

$$v_{OUT} = A(v^+ - v^-) - I_2 R_{OUT}.$$

Then, some node equations to set up the currents in terms of voltages:

$$i_1 = \frac{v_{IN} - v_{OUT}}{R_1 + R_2}.$$

$$i_3 = \frac{v_{OUT}}{R_3 + R_4}.$$

From here, we can eliminate i_2, and substitute in for v^+ and v^-, getting v_{OUT} in terms of itself and v_{IN}.

We create the following definitions: $R_{12} = R_1 + R_2$, $R_{34} = R_3 + R_4$, and $R_T = R_1 + R_2 + R_3 + R_4$.

$$v_{OUT} = A\left(\frac{R_1 v_{OUT} + R_2 v_{IN}}{R_{12}} - \frac{R_4 v_{OUT}}{R_{34}}\right) - R_{OUT}\left(\frac{v_{OUT} - v_{IN}}{R_{12}} - \frac{v_{OUT}}{R_{34}}\right).$$

This can be solved for v_{OUT}.

$$v_{OUT} = v_{IN}\frac{AR_2R_{34} + R_{OUT}R_{34}}{R_{12}R_{34} - A(R_1R_{34} - R_4R_{12}) + R_{OUT}R_T}.$$

To find the current asked for, which is $-i_1$, use the equation

$$i = \frac{v_{OUT} - v_{IN}}{R_{12}}.$$

Substituting the previously derived expression for v_{OUT} and simplifying, one gets that

$$i = v_{IN}\frac{AR_3R_{12} - R_{OUT} - R_{12}}{A(R_4R_{12} - R_1R_{34}) + R_{12}R_{34} + R_{OUT}R_T}$$

a) Assuming that A is so large that any terms lacking it may be neglected, and that $R_{OUT} = 0$, we get the following value for v_{OUT}.

$$v_{OUT} = v_{IN}\frac{(R_2)(R_3 + R_4)}{-R_1(R_3 + R_4) + R_4(R_1 + R_2)}.$$

b) Finding the limiting case again, we get that:

$$i = v_{IN} \frac{R_3}{-R_1(R_3 + R_4) + R_4(R_1 + R_2)}.$$

c) The voltage gain becomes infinite when the denominator is zero. In the ideal case, this occurs when

$$R_1(R_3 + R_4) = R_4(R_1 + R_2).$$

This can be simplified to get that

$$R_1 R_3 = R_2 R_4$$

This occurs due to the presence of positive feedback.

d) For a non-ideal op-amp, the voltage will never actually exceed the supply voltage, and for a set of resistor parameter ranges, the op-amp will rail. This set of parameters may be calculated by finding the internal voltage of the op-amp (without the drop across the output resistance), and seeing for what values of R_1, R_2, R_3, R_4 and A it exceeds the supply voltage.

ANS:: (a) $v_{OUT} = v_{IN} \frac{(R_2)(R_3+R_4)}{-R_1(R_3+R_4)+R_4(R_1+R_2)}$, b) $i = v_{IN} \frac{R_3}{-R_1(R_3+R_4)+R_4(R_1+R_2)}$, c) $R_1 R_3 = R_2 R_4$

Problem 15.8 Choose values for R_1 through R_5 in Figure 15.55 so that

$$v_O = +2v_1 - 5v_2 - v_3 - 3v_4$$

You may assume the operational amplifier has ideal characteristics.

Solution:

See Figure 15.56.

$v^+ = v^- = \frac{v_1 R_5}{R_4+R_5}$

$i = \frac{v_4 - v^-}{R_1} + \frac{v_3 - v^-}{R_2} + \frac{v_2 - v^-}{R_3}$

$v_O = v^- - iR_6$

Combining these, we get:

$v_O = \frac{V_1 R_5}{R_4+R_5} \left(1 + \frac{R_6}{R_1} + \frac{R_6}{R_2} + \frac{R_6}{R_3}\right) - R_6 \left(\frac{V_4}{R_1} + \frac{V_3}{R_2} + \frac{V_2}{R_3}\right).$

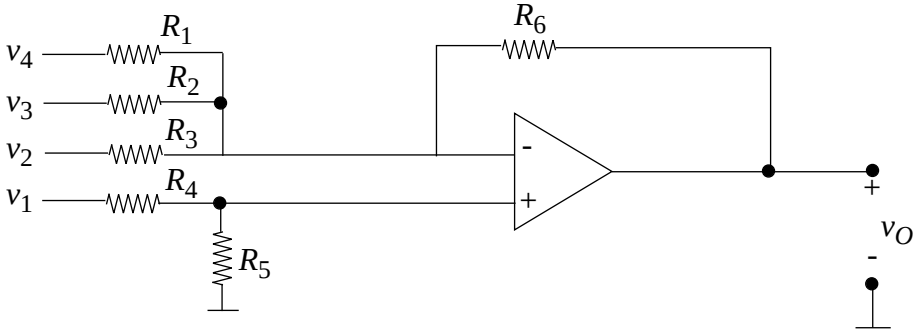


Figure 15.55:

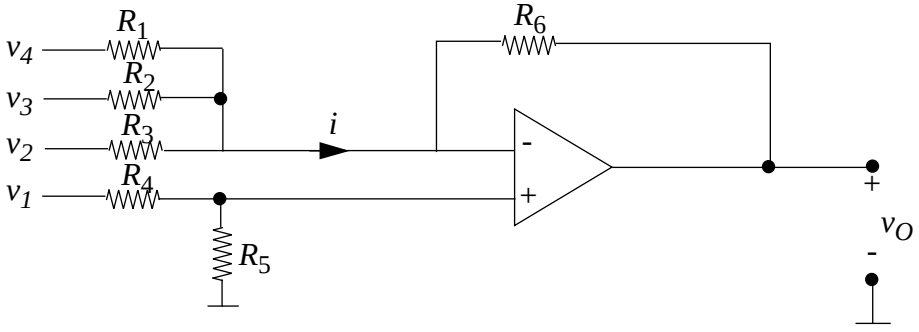


Figure 15.56:

One possible set of values is:

$R_1 = 10k\Omega, R_2 = 30k\Omega, R_3 = 6k\Omega, R_4 = 7k\Omega, R_5 = 2k\Omega, R_6 = 30k\Omega.$

These resistances can all be easily synthesized using common values.

ANS:: $R_1 = 10k\Omega, R_2 = 33k\Omega||330k\Omega, R_3 = 6.8k\Omega||47k\Omega, R_4 = 6.8k\Omega + 200\Omega, R_6 = 33k\Omega||330k\Omega$

Problem 15.9 For the circuit in Figure 15.57, find v_O in terms of v_I. Analyze with literal resistor values, then substitute numbers: $R_1 = R_2 = R_3 = 10$ kilohms. $R_4 = 100$ ohms.

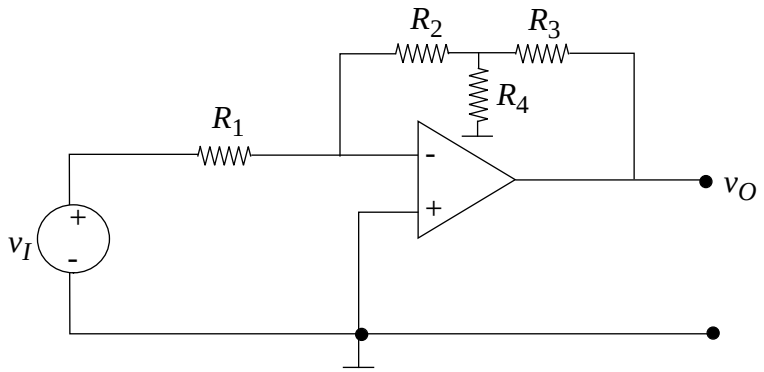


Figure 15.57:

Solution:

Since $v^+ = v^- = 0$, one can redraw the circuit as shown in Figure 15.58.

Note: ground shaded regions

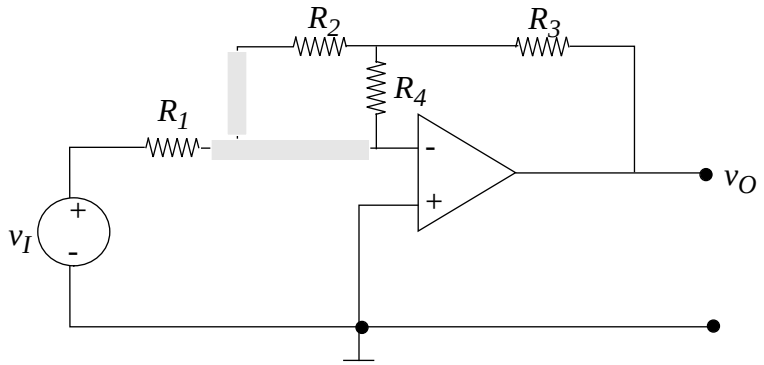


Figure 15.58:

From here, one can find the equivalent resistance of $R_3 + (R_2||R_4)$ and then realize that this is a simple inverting-amplifier configuration.

ANS::

$$\frac{V_{OUT}}{v_{IN}} = -\frac{(R2||R4)+R3}{R1} = -1.9091.$$

Problem 15.10 This question concerns the circuit illustrated in Figure 15.59:

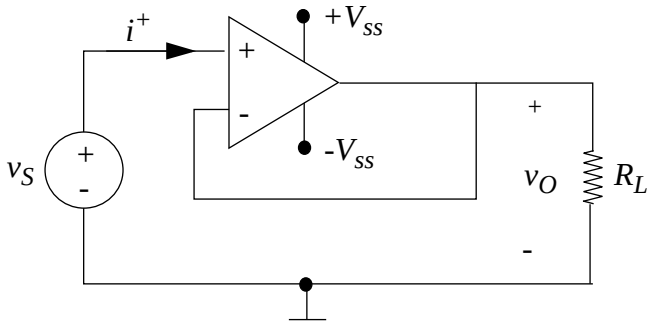


Figure 15.59:

The operational amplifier is a high gain unit ($A = 10^5$) with high input resistance, r_i, and negligibly low output resistance, r_t. Assume that it is operating in its linear region.

The following data is given:

$$\begin{aligned} v_S &= 1V \\ i^+ &= 10pA = 10^{-11}A \\ R_L &= 1k\Omega \end{aligned}$$

a) What is v_O? (Accurate to within 1%).

b) i) What is the power delivered by the source v_S?

ii) What is the power dissipated in the load resistor, R_L?

c) The power dissipated in the load resistor, R_L, is much larger than the power supplied by the source, v_S. Where does this additional power come from?

Solution:

a) $v_O \approx v_S = 1V$

b) i) $Power = v_S i^+ = 10^{-11} Watts$

ii) $Power = \frac{v_O^2}{R_L} = 10^{-3} Watts$

c) The additional power comes from the power supply!!! ($+V_{SS}$).

ANS:: (a) $v_O \approx v_S = 1V$, (b) i) $Power = v_S i^+ = 10^{-11} Watts$, ii) $Power = \frac{v_O^2}{R_L} = 10^{-3} Watts$, () from the op-amp power supply V_{SS}.

Problem 15.11 The equivalent circuit of an amplifier is shown in Figure 15.60.

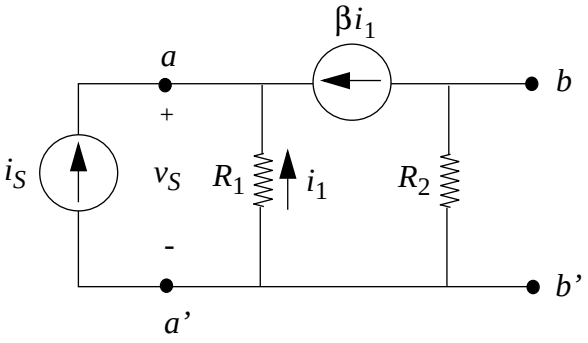


Figure 15.60:

a) Find the input resistance seen by the current source i_S at the input terminals $a - a'$.

b) Find the output resistance seen at the output terminals $b - b'$ (with the current source shut off).

Solution:

a) $R_{in} = \frac{v_S}{i_S}$
$v_S = -i_1 R_1$
$i_S + i_1 + \beta i_1$
$R_{IN} = \frac{R_1}{1+\beta}$

b) $i_S = 0$
$\beta i_1 = -i_1$
$i_1 = 0$
$R_{OUT} = R_2$

ANS:: (a) $R_{IN} = \frac{R_1}{1+\beta}$, (b) $R_{OUT} = R_2$

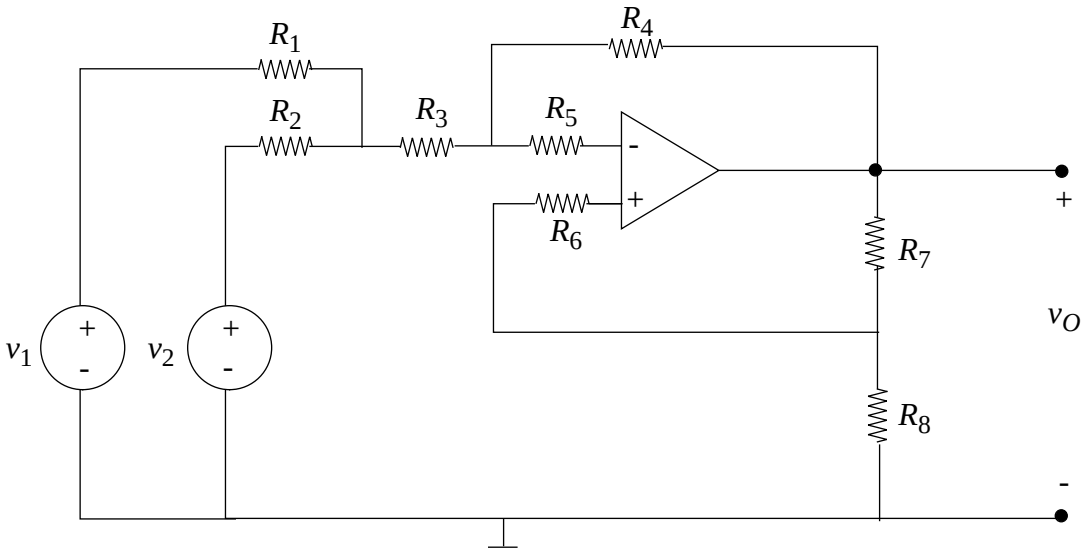


Figure 15.61:

Problem 15.12 For the circuit in Figure 15.61 find v_O in terms of v_1 and v_2. You can use in your analysis the ideal Op Amp model.

Solution:

Since the ideal opamp has infinite input impedance, $i^- = i^+ = 0$. The resistors R_5 and R_6 can thus be disregarded (set to 0).

We then find the Thevenin equivalent of the left side, as shown in Figure 15.62. From there, the problem is identical to Problem 15.7.

The open-circuit voltage was found in Problem 15.6, and is:

$$v_{TH} = \frac{v_1 R_2 + v_2 R_1}{R_1 + R_2}.$$

The Thevenin resistance is $(R_1||R_2) + R_3$.

$$r_{TH} = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_1 + R_2}.$$

We import the following formula from Problem 15.7, changing the parameter names to suit this exact configuration.

$$v_{OUT} = v_{TH} \frac{R_4(R_7 + R_8)}{R_8(R_{TH} + R_4) - R_{TH}(R_7 + R_8)}.$$

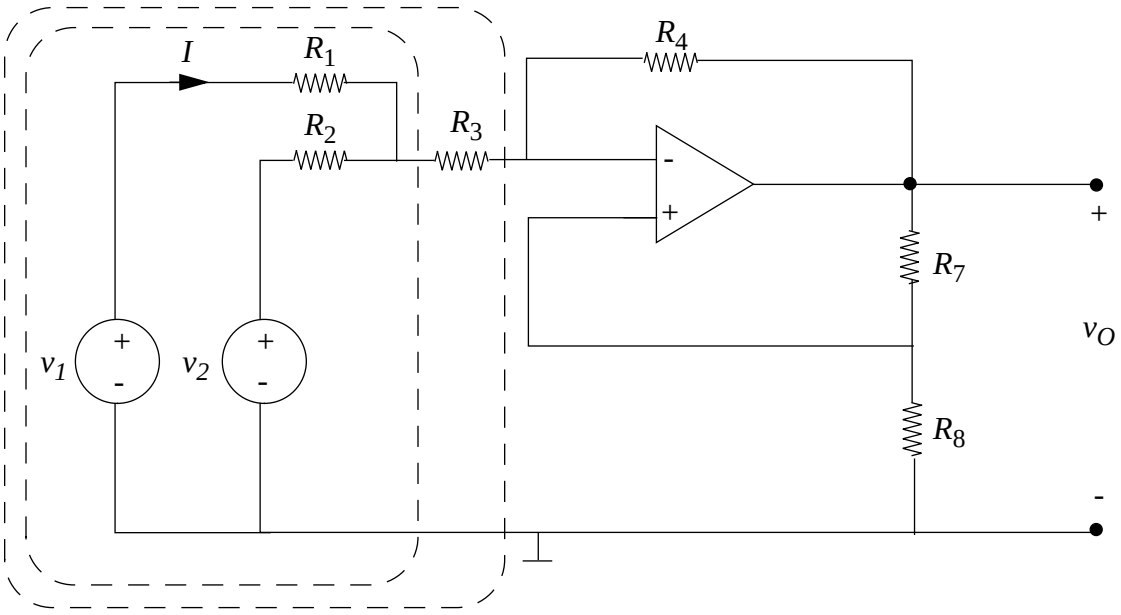


Figure 15.62:

Substituting and simplifying, one gets:

ANS:: $V_{OUT} = \frac{R_4(v_1 R_2 + v_2 R_1)(R_1 + R_2)}{R_1 R_4 R_8 + R_2 R_4 R_8 - R_1 R_2 R_7 - R_1 R_3 R_7 - R_2 R_3 R_7}$.

Problem 15.13 An operational amplifier circuit is shown in Figure 15.63.

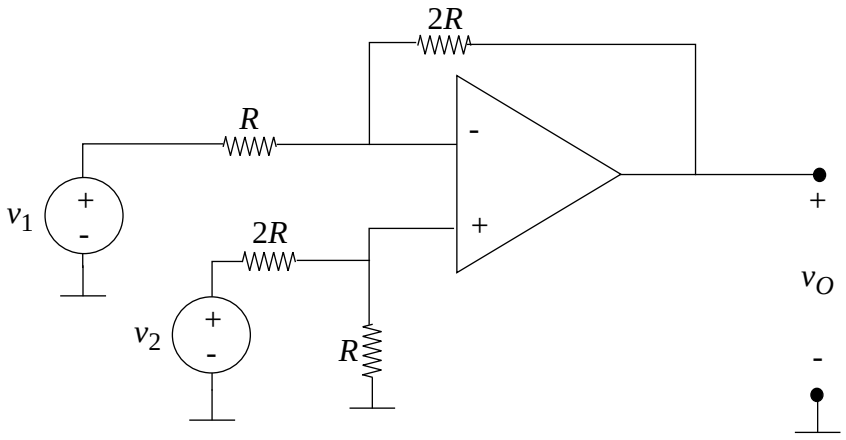


Figure 15.63:

You may assume that the operational amplifier has ideal characteristics, including zero input current and output resistance and further make the simplifying assumption that its open-loop gain is infinite. Also, assume that the amplifier does not saturate.

a) With $v_2 = 0$, what is the value of the gain v_O/v_1?

b) Voltage v_2 is now made 3 volts. Plot the v_O vs. v_1 characteristics. Be sure to show important values and slopes.

Solution:

The bias applied to the non-inverting terminal has a Thevenin voltage of $\frac{v_2}{3}$. Therefore, the voltage at the inverting terminal is also $\frac{v_2}{3}$. Use the following KVL equations.

$$v_1 - iR - 2iR = v_O.$$

$$v_1 - i_R = \frac{v_2}{3}.$$

Eliminating i, one gets that

$$v_O = -2v_I + 3.$$

a) We set $v_2 = 0$ and get a standard inverting amplifier, as is expected.

$$\frac{v_O}{v_1} = -2.$$

b) See Figure 15.64.

ANS:: (a) $\frac{v_O}{v_1} = -2$.

Problem 15.14 By combining Op Amps with RC circuits, we can make circuits which perform elementary mathematical operations, such as integration and differentiation. The circuit in Figure 15.65 is, over some range, an integrator.

a) Use the ideal Op Amp model to determiner the ideal function performed by this circuit.

b) Based on your knowledge of Op Amp limitations, indicate the constraints that must be placed on the component values R and C to achieve satisfactory operation, assuming that the input is a sine wave with angular frequency ω and peak amplitude A.

Express your answer as a constraint on the RC product imposed by the voltage limit, and a separate constraint imposed by the current limit.

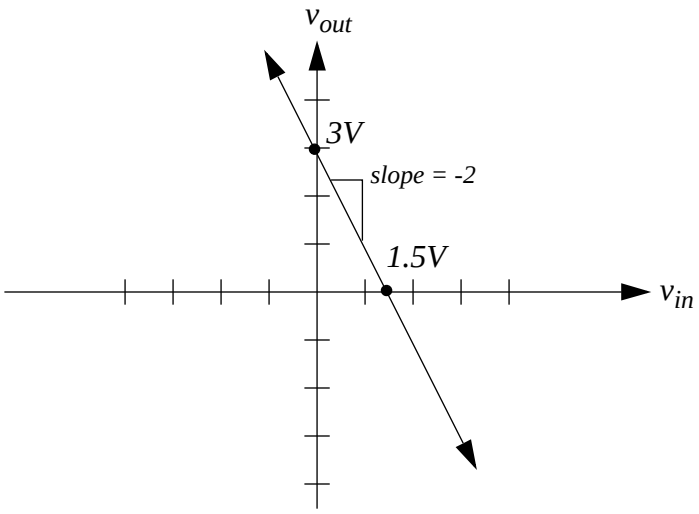


Figure 15.64:

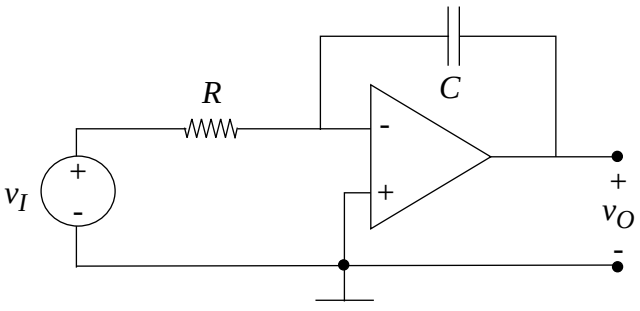


Figure 15.65:

c) For practical reasons, R usually should not be greater than 1 megohm. Calculate the value of C required to meet the voltage constraint listed above for operation at 20 Hz and above, and $A = 1$ volt.

Solution:

a) See Figure 15.66.

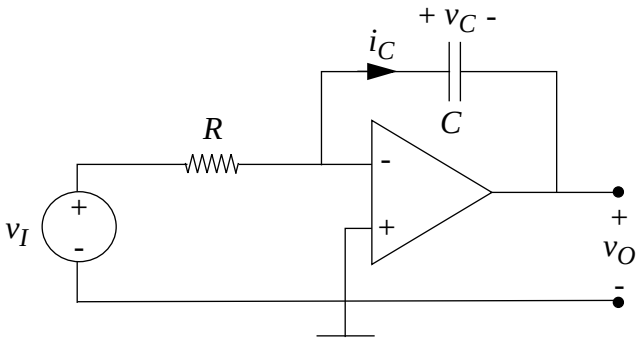


Figure 15.66:

$v^+ = v^- = 0$

$i_C = C\frac{dv_C}{dt} = -C\frac{dv_O}{dt} = \frac{v_I}{R}$

$v_O = \frac{-1}{RC}\int v_I dt$

b) $v_I = A\sin(\omega t)$

$v_O = \frac{-A}{\omega RC}\cos(\omega t)$

Assume opamp has voltage limit $\pm V_{LIM}$.

$RC > \frac{A}{\omega V_{LIM}}$

$i_C = \frac{A}{R}\sin(\omega t)$

Assume opamp has current limit $\pm I_{LIM}$.

$\frac{A}{R} < I_{LIM}$

c) $\omega = 2\pi f \geq 40\pi$

$R \leq 1M\Omega$

$C > \frac{A}{\omega R V_{LIM}}$

Assuming that V_{LIM} = 15 volts:

$C > 530pF$

ANS:: (a) $v_O = \frac{-1}{RC}\int v_I dt$, (b) $RC > \frac{A}{\omega V_{LIM}}$, (c) $C > 530pF$

Problem 15.15 The capacitor you calculated in Problem 15.14c is (or should be) much larger than the maximum capacitor that can be included on a VLSI chip. For this reason, the circuit in Figure 15.65 must usually be built of Op Amps, discrete R's and C's. To allow the circuit to be built on a chip, the resistor is replaced by a *switched capacitor*, which can produce a very large "effective resistor" with reasonable capacitor values. This circuit is shown in Figure 15.67.

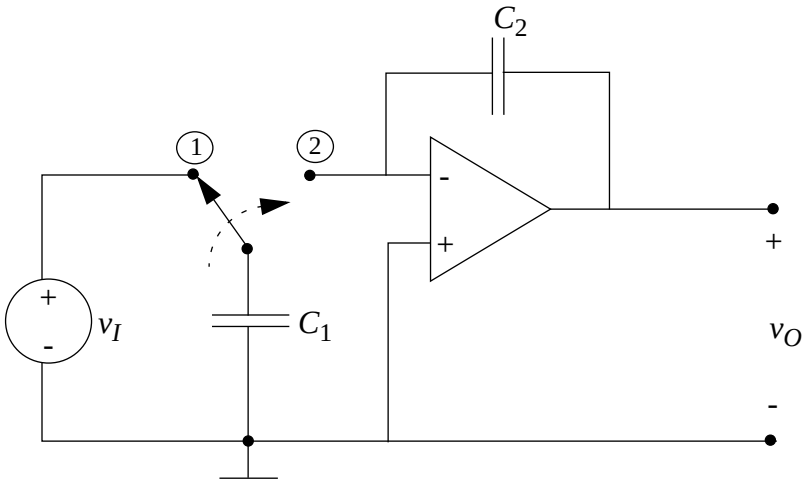


Figure 15.67:

At time $t = t_1$, the switch moves to position (1), and C_1 charges (instantly) to voltage $v_1(t_1)$. Then at time t_2, the switch moves to position (2), and C_1 discharges into C_2. Assuming that the usual Op Amp approximation of $(v^+ - v^-) \simeq 0$ can still be used, calculate the charge that is "dumped" at each cycle, hence the average current (a function of both v_I and the switching frequency f_c), and hence the effective resistance of the switched capacitor. Also, show that the overall system equation relating v_O to v_I is the same as in Problem 15.14.

Solution:

$Q_{dumped} = C_1 v_1 t_1$ If the switching frequency is much faster than the frequency of v_I, then:

$i_{AVG} = f_c C_1 v_I$

The effective resistance is then $\frac{1}{f_c C_1}$.

$v_O = \frac{-1}{C_2}\int i_{AVG} dt$

$v_O = \frac{-f_c C_1}{C_2}\int v_I dt$

This is the same function as in problem 14 when $\frac{1}{f_c C_1} = R$.

Problem 15.16 In Fig. 15.67, what are the constraints on C_1 and C_2 set by the Op Amp voltage and current limits? Calculate the appropriate values of C_1, C_2 and f_c for operation at 20 Hz and above. Can the circuit now be built on an IC chip if we replace the switch by MOS transistors, and $C_{max} = 100pF$?

Solution:

The effective resistance of the capacitor can be calculated as follows. The capacitor is instantly charged when the switch is set to connect it with the voltage source. The amount of charge on the capacitance can be calculated by the formula $Q = C_1 v_I$. When the switch is moved to the second position, all this charge is immediately released due to the capacitor now being connected to an effective ground. Therefore, the rate of current move is $i = Q f_C$, which is $i = C_1 v_I f_C$. From this, we can calculate the effective resistance $\frac{v_I}{i} = R_e f f = \frac{1}{C_1 f_C}$.

From here, we have a simple inverting amplifier configuration. The maximum voltage gain is equal to $\frac{1}{C_2 R_e f f s}$, which is equal to $\frac{C_1 f}{C_2 s}$. If our maximum voltage limit is V_{MAX}, our maximum current limit is I_{MAX} and our maximum input voltage is v_{IN-MAX}, then we have the following relations:

$$v_{IN-MAX} \frac{C_1 f_C}{40\pi C_2} < V_{MAX}.$$

$$v_{IN-MAX} C_1 f_C < I_{MAX}.$$

This can be simplified to the following:

A typical IC configuration will support an op-amp with a voltage rail of ± 2.5 volts, and a maximum current of 1 milliampere. The input signal that needs to be amplified can be assumed to be much less than the bias voltages necessary to make the op-amp work correctly, given only a $+5V$ supply and a ground. Therefore, we can assume V_{IN-MAX} to be $25mV$.

Given this, we can find the numerical values for the constraints on $C_1 f_C$.

$$C_1 f_C < 40, C_1 f_C < 4000\pi C_2.$$

Clearly the second criterion is much more restrictive. If we let C_2 be the maximum allowed value of 100 picofarads, this implies that

$$C_1 f_C < 4\pi 10^{-7}.$$

We would like this to run at a sufficiently high rate, of at least 100KHz, so we set $f_C = 100KHz$, which gives us $C_1 = 4\pi 10^{-13}$. This clock rate is very modest, and probably would not be effective for anything much higher than the 20Hz signals expected. It is difficult to design for both low and high frequency response simultaneously.

ANS:: $C_1 = 1.256 * 10^-12F, C_2 = 10^-10F, f_C = 100KHz.$

Problem 15.17 Design a differentiator circuit out of RC circuits and Op Amps.

Calculate the constraints as in Problem 15.14b.

Solution:

a) See Figure 15.68.

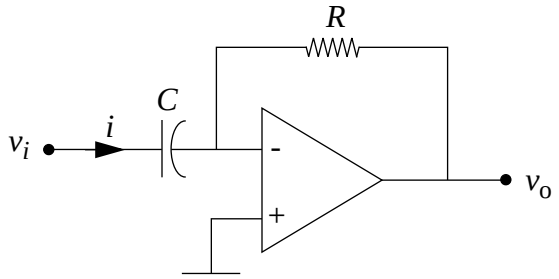


Figure 15.68:

$v^- = v^+ = 0$

$i = C\frac{dv_I}{dt}$

$v_O = -RC\frac{dv_I}{dt}$

b) Assume voltage limit V_L, current limit I_L.

$v_I = A\sin(\omega t)$

$\frac{dv_I}{dt} = A\omega\cos(\omega t)$

$I_{PEAK} = AC\omega < I_L$

$C < \frac{I_L}{A\omega}$

$V_{PEAK} = RCA\omega < V_L$

$RC < \frac{V_L}{A\omega}$

$C < \frac{I_L}{A\omega}; RC < \frac{V_L}{A\omega}$

ANS:: $C < \frac{I_L}{A\omega}; RC < \frac{V_L}{A\omega}$

Problem 15.18 This problem deals with switched-capacitor circuits introduced in Problem 15.15. Referring to Figure 15.69, assume both S_1 switches are closed for time $1/2f_0$ with S_2 open, and S_2 closed for $1/2f_0$ with s_1 open. Assume no overlap, i.e., and S_1 and S_2 switches are never both closed at the same time.

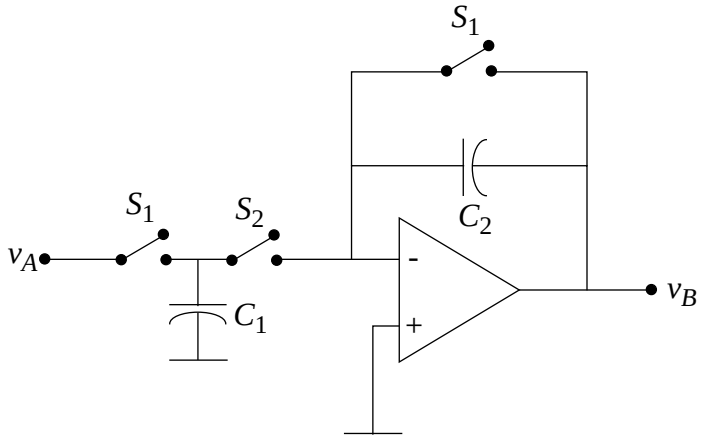


Figure 15.69:

a) For $v_A = A$ volts (constant), go through one complete clock cycle, identifying the charge on each capacitor and the voltage at each node.

b) Now assume $v_A = A \cos \omega t$ where $\omega << 2\pi f_0$. Sketch v_B. In the circuit as constructed, v_B is zero half the time. During the *other* half cycles, v_B and v_A are related by a simple gain expression, just as in a normal inverting amplifier. What is the "gain"?

Solution:

a) First, switch S_1 is closed, so the second capacitor is discharged to ground, and the first capacitor is charged to v_A. The output voltage is zero as well.

Then, when S_2 is closed, the first capacitor discharges onto the second one, so the voltage across the first capacitor is now 0, and the voltage across the second is $-v_B$. By the conservation of charge, $v_A C_1 = -v_B C_2$, so $v_B = -\frac{v_A C_1}{C_2}$.

b) See Figure 15.70.

From the previous expression, the gain can be calculated to be:

$$-\frac{-C_1}{C_2}.$$

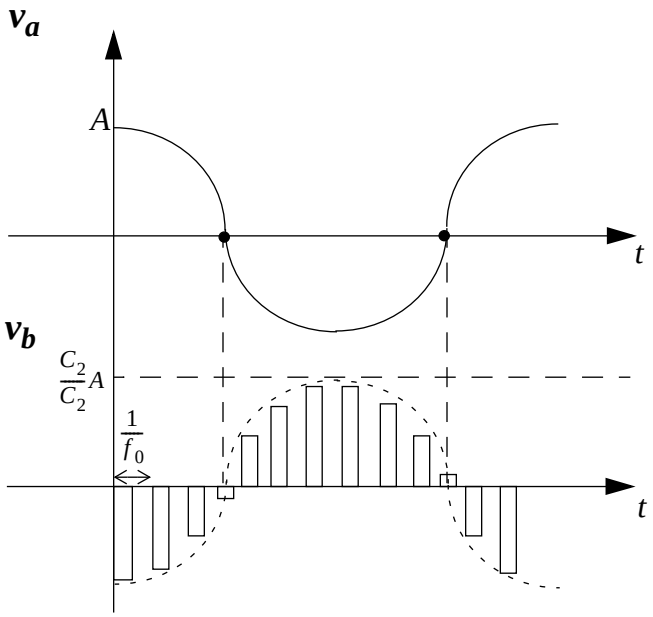


Figure 15.70:

ANS:: (b) $-\frac{-C_1}{C_2}$.

Problem 15.19 Figure 15.71 is a *practical* implementation of a switched capacitor circuit (see Problem 15.15). As in the previous problem, it is useful to examine the behavior of an "average v_B" over a clock cycle.

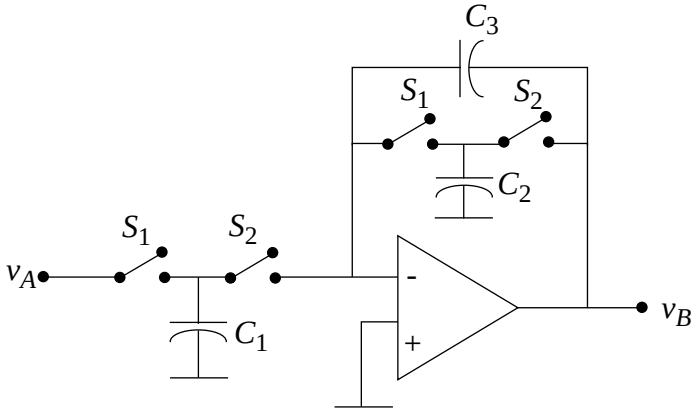


Figure 15.71:

a) Show that if $v_A = A$ volts (constant), the cycle-average of v_B has a steady-state value equal to $-(C_1/C_2)A$. In other words, for low-frequency signals, the circuit behaves like a non-inverting amplifier with gain $-(C_1/C_2)$.

b) Show, for v_A a step of amplitude A volts, and assuming v_B is initially zero, that the cycle average of v_B "charges up" to its steady-state value with time constant $\tau = c_3/f_0C_2$. That is, show that the cycle-average of v_B obeys a first order linear differential equation with time constant C_3/f_0C_2.

Solution:

a) Both switched capacitors can be modeled as resistors, and the impedance model drawn as shown in Figure 15.72. This is a standard inverting op-amp with effective gain:

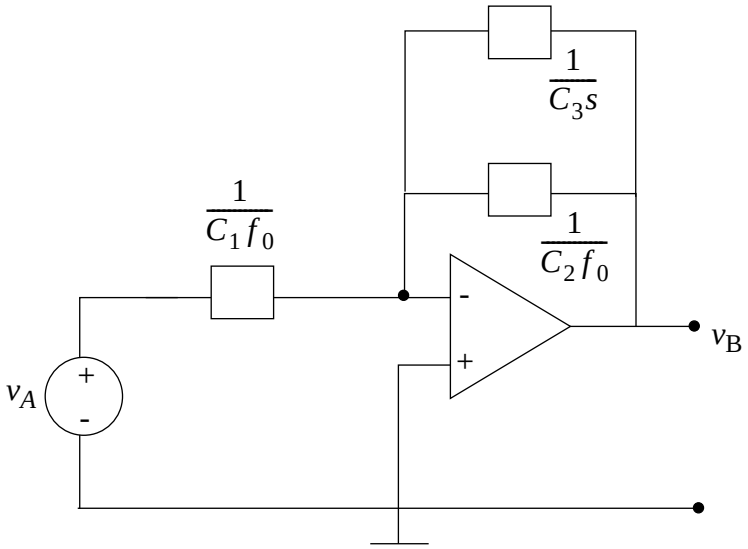


Figure 15.72:

$$gain = \frac{\frac{-1}{C_3 s + C_2 f_0}}{\frac{1}{C_1 f_0}} = \frac{-C_1 f_0}{C_3 s + C_2 f_0}.$$

For a low signal $s = j\omega << f_0$, the $C_3 s$ term drops out, and the device becomes an amplifier with gain $-\frac{C_1}{C_2}$.

b) The natural frequency in the denominator of the transfer function is $\frac{C_2 f_0}{c_3}$, which implies a time constant of $\frac{C_3}{C_2 f_0}$.

Problem 15.20 a) Use the ideal Op Amp model to determine the ideal function performed by the circuit in Figure 15.73.

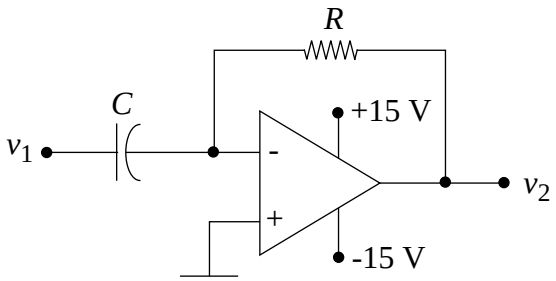


Figure 15.73:

b) Based on your knowledge of Op Amp limitations, discuss the accuracy with which the circuit will perform the intended function, or indicate any constraints that must be placed on the component values R and C to achieve satisfactory operation, assuming that the input is:

i: A sine wave with angular frequency ω and peak amplitude A.

ii: A triangle wave with period T and peak amplitude A.

iii: A square wave with period T and peak amplitude A.

c) The leakage of an actual capacitor can often be modeled by a large resistor in parallel with an ideal capacitor. What effects on circuit performance would capacitor leakage have?

Solution:

Model the capacitor as non-ideal by placing it in parallel with a leak resistor R_L. See Figure 15.74.

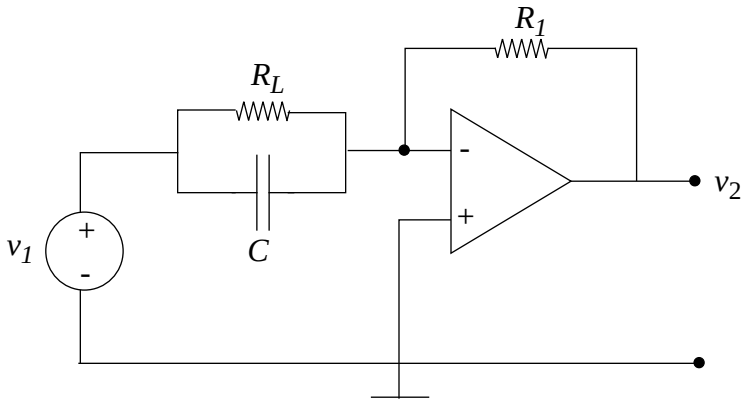


Figure 15.74:

The best way to do this problem is by superposition. We can place the voltage source onto the capacitor by itself, and then onto the resistor by itself. The resistor causes the

circuit to act as an inverting amplifier and the capacitor, as an inverter. The sum of them is as follows:

$$-R_L v_2(t) = RR_L C\frac{dv_1(t)}{dt} + Rv_1(t).$$

a) In the ideal case, the terms with no R_L factor may be dropped since the leak resistor is an open circuit with an infinite resistance.

$$v_2(t) = -RC\frac{dv_1(t)}{dt}$$

b) i) $v_1 = A\sin(\omega t)$
$i = AC\omega\cos(\omega t)$
$AC\omega < I_{LIMIT}$
$v_2 = -RCA\omega\cos(\omega t)$
$RCA\omega < V_{LIMIT}$

ii) $i_{peak} = \frac{4CA}{T} < I_{LIMIT}$
$\frac{4CAR}{T} < V_{LIMIT}$
Furthermore, since the triangle is a function whose derivative is not defined at the switching points, the op-amp will rail alternatingly at the negative supply value (when the switch is from up to down) and the positive supply value (when the switch is from down to up), once each per period.

iii) The derivative of a square wave consists of impulses. The opamp limits on voltage and current prevent the circuit from performing the intended function accurately.

c) The non-idealness will cause an extra term that is proportional to the input to be added to the derivative of the input.

$$v_2(t) = -RC\frac{dv_1(t)}{dt} - \frac{R}{R_L}v_1(t).$$

ANS:: (a) $v_2(t) = -RC\frac{dv_1(t)}{dt}$, (c) $v_2(t) = -RC\frac{dv_1(t)}{dt} - \frac{R}{R_L}v_1(t)$.

Problem 15.21 a) Using the "ideal operational amplifier" assumption, i.e., infinite gain, infinite input resistance, and zero output resistance, determine the relationship between $v_O(t)$ and $v_I(t)$ in Figure 15.75.

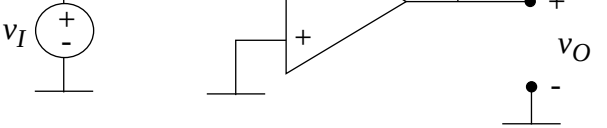


Figure 15.75:

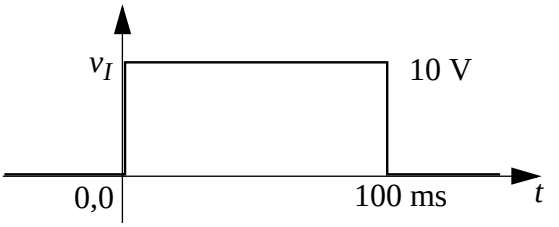


Figure 15.76:

b) If the signal $v_I(t)$ is the rectangular pulse in Figure 15.76, sketch $v_O(t)$ for $t > 0$, assuming that $v_O(0) = 0$.

Solution:

a) $v^+ = v^- = 0$

$i = \frac{v_I}{R} = -C\frac{dv_O}{dt}$

$v_O = -10 \int v_I dt$

b) See Figure 15.77.

ANS:: (a) $v_O = -10 \int v_I dt$

Problem 15.22 An operational amplifier is connected as shown in Figure 15.78.

The voltage v_I is 2 volts for $0 < t < 1$ ms, and 0 otherwise. Assuming that $v_O = 0$ for $t < 0$, sketch v_O for $t > 0$.

Solution:

First, draw the full impedance model of the voltage-source, as shown in Figure Figure15.79.

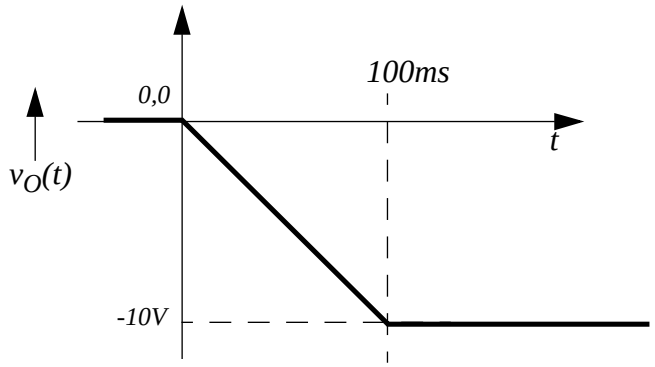


Figure 15.77:

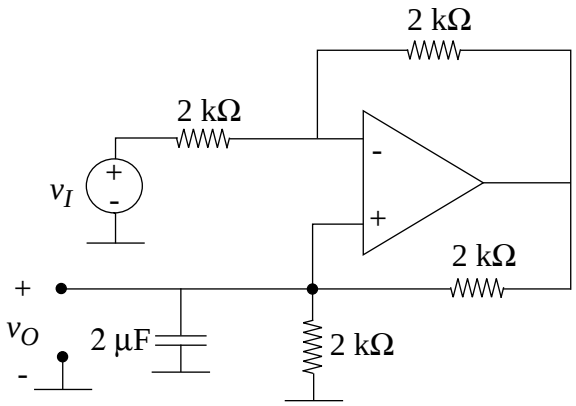


Figure 15.78:

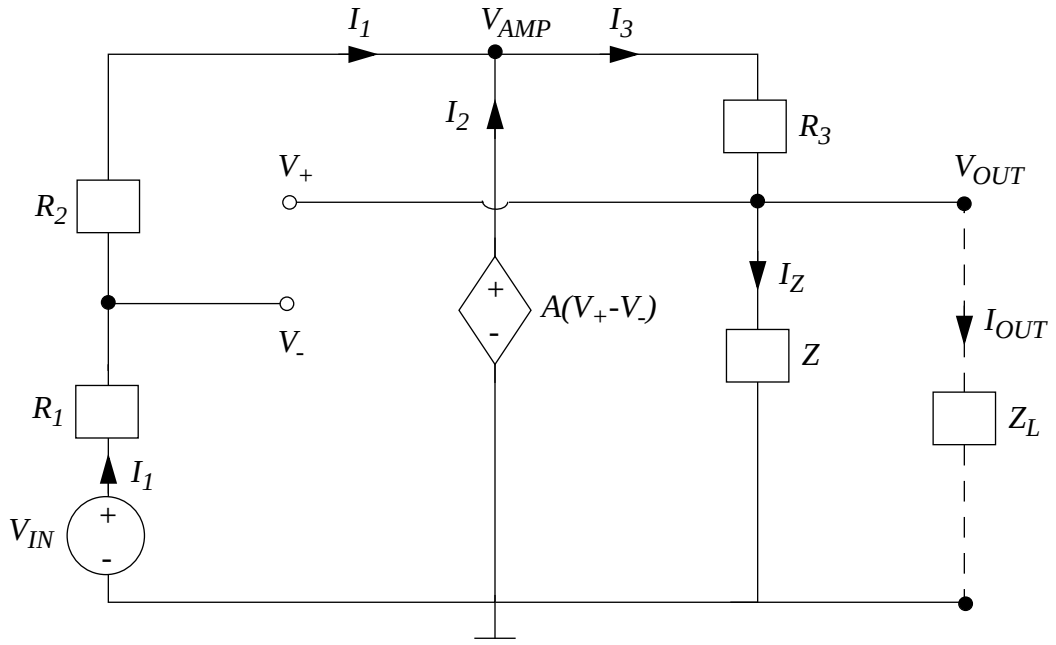


Figure 15.79:

Let Z_L be an arbitrary output load impedance, and Z be the impedance of the resistor and capacitor in parallel, which is $\frac{R_4}{R_4Cs+1}$.

From here, we can get the following three node equations:

$$\frac{v_I - v^-}{R_1} = \frac{v^- - v_{AMP}}{R_2},$$

$$\frac{v_{AMP} - v_O}{R_3} = \frac{v_O}{Z} + \frac{v_O}{Z_L},$$

$$v_{AMP} = A(v_O - v^-).$$

Simplifying these three, we can get the following relation:

$$\frac{v_O}{v_I} = \frac{-R_2 Z Z_L}{R_1 R_3 Z_L + R_1 R_3 Z - R_2 Z Z_L}.$$

Substituting in for Z and simplifying more...

$$\frac{v_O}{v_I} = \frac{-R_2 R_4 Z_L}{R_1 R_3 Z_L (R_4 Cs + 1) + R_1 R_3 R_4 - R_2 R_4 Z_L}.$$

Then, even though the notation of the problem would indicate otherwise (filled output nodes), we assume that Z_L is infinitely large. We substitute in the given values of $R_1, R_2, R_3, R_4,$ and C, to get that

$$v_O(s) = \frac{-250}{s} v_I(s).$$

Taking the inverse Laplace transform of this, we get:

$$v_O(t) = -250 \int v_I(t) dt.$$

The corresponding graph is shown in Figure Figure15.80.

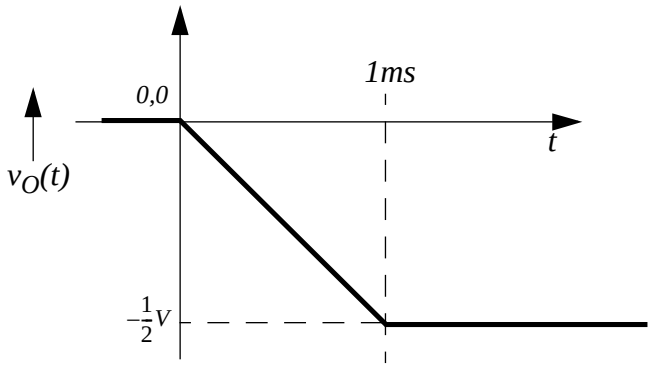


Figure 15.80:

Problem 15.23 Consider the following two circuits in Figure 15.81.

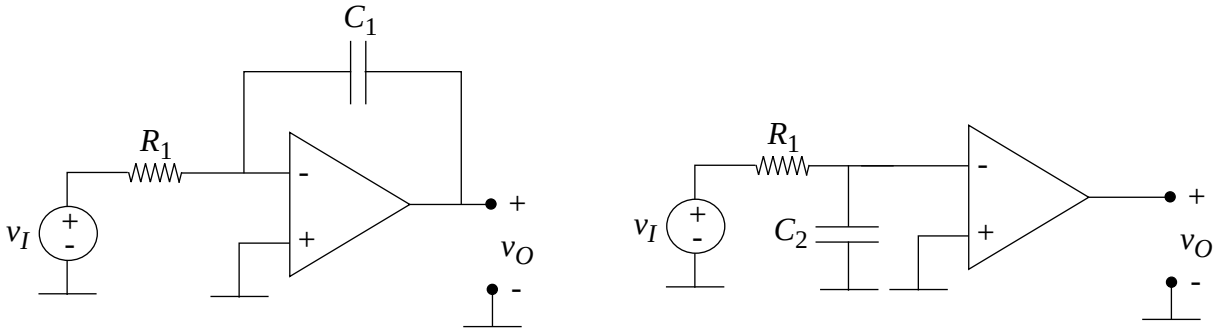


Figure 15.81:

Use the Op Amp model to find the transfer function v_O/v_I for the two circuits.

Assume only *moderate* gain (say 100) for the Op Amp so you cannot assume $v^+ = v^-$. How large does C_2 have to be compared to C_1 in order for the two circuits to behave the same? The increase in the effective size of C_1 because of the gain of the amplifier is called the "Miller Effect", and is used in Op Amp design.

Solution:

Both amplifiers have output $v_O = -Av^-$. The node equation for the first one is as follows:

$$\frac{v_I - v^-}{R_1} = \frac{v^- - v_O}{\frac{1}{C_1 s}}.$$

These two equations can be combined to yield the following result:

$$\frac{v_O}{v_I} = \frac{-A}{R_1 C_1 s(A+1)+1}.$$

The second amplifier has a voltage-divider at the input:

$$\frac{v^-}{v_I} = \frac{\frac{1}{C_2 s}}{R_1 + \frac{1}{C_2 s}}.$$

This, combined with the amplifier gain model, results in the following transfer function:

$$\frac{v_O}{v_I} = \frac{-A}{R_1 C_2 s + 1}.$$

Comparing these two, we get the following relation:

$$R_1 C_2 s = R_1 C_1 s(A+1).$$

This can be simplified to:

ANS:: $C_2 = C_1(A+1)$.

Problem 15.24 Assuming an ideal Op Amp: (large gain, $v^+ \simeq v^-$, r_{in} infinite, r_{out} zero, but including amplifier saturation effects.)

a) Plot a curve of i_{IN} versus v_{IN} between -20 and +20 volts for the circuit in Figure 15.82, assuming $R_2 = R_3$. Dimension your plot.

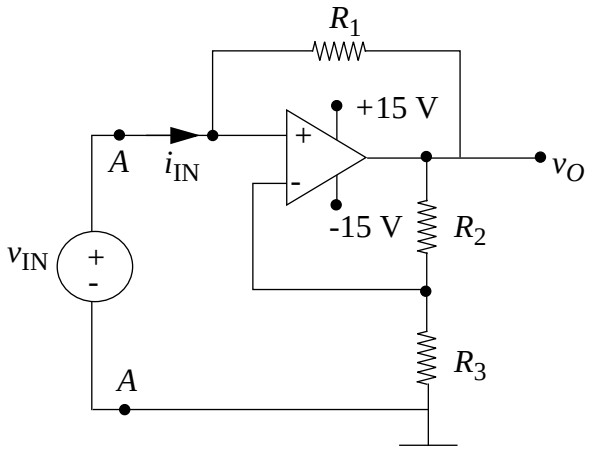


Figure 15.82:

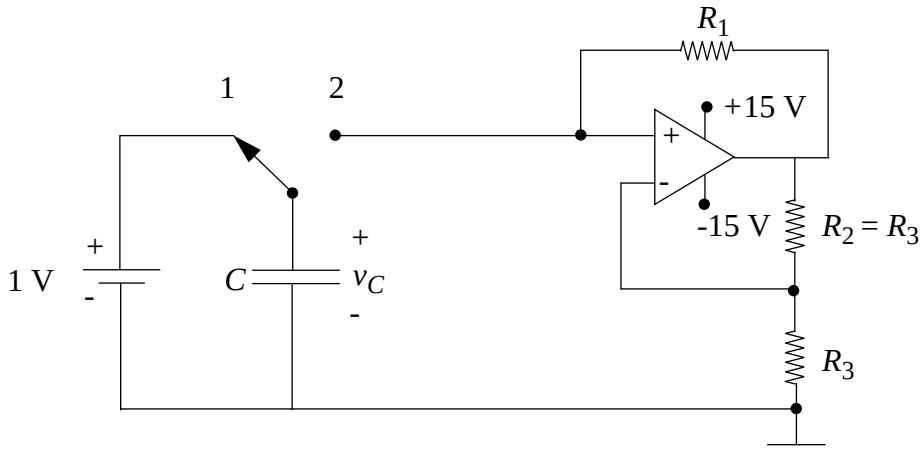


Figure 15.83:

b) A capacitor is initially charged to 1 volt (switch in position (1)) in Figure 15.83, then connected to the circuit at $t = 0$ (switch in position (2)). Sketch and dimension the waveform $v_C(t)$ for t greater than zero.

Solution:

a) First, draw the input as shown in Figure 15.84.

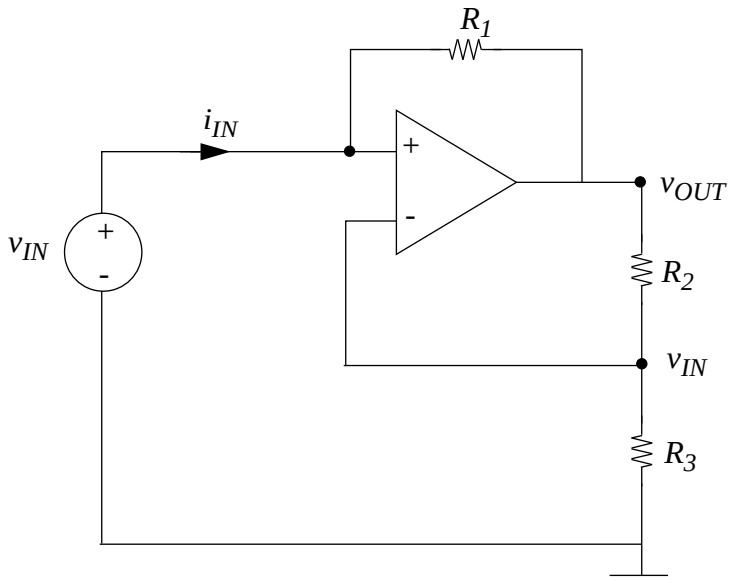


Figure 15.84:

The current is derived as follows:

$$i_{IN} = \frac{v_{IN} - v_{OUT}}{R_1}.$$

If the op-amp is not railed, then by a simple voltage-divider rule, $v_{OUT} = 2v_{IN}$. If the op-amp is railed, then either $v_{OUT} = 15V$, or $v_{OUT} = -15V$. The current is therefore characterized as follows:

$$i_{IN} = \frac{v_I N + 15}{R_1} for v_{IN} < -7.5V, i_{IN}$$

$$= -\frac{v_{IN}}{R_1}, for -7.5V < v_{IN} < 7.5V, and i_{IN} = \frac{v_{IN} - 15}{R_1} for v_{IN} > 7.5V$$

See Figure 15.85 for the relevant $v - i$ plot.

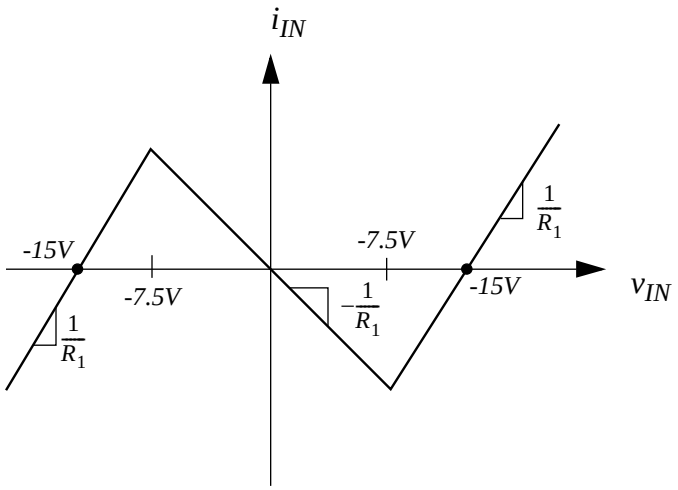


Figure 15.85:

b) While the voltage across the capacitor is between -7.5V and 7.5V, the circuit will act as a simple RC circuit, but with a negative resistance. Therefore, the voltage across the circuit will increase exponentially with a time constant of $-CR_1$. When the voltage hits 7.5V, the device will start acting like an ordinary resistor, which attempts to discharge the capacitor. This immediately drops the voltage below 7.5V, which then increases it again. Therefore, once the voltage hits 7.5V, it will never change.

See Figure 15.86 for the plot of voltage as a function of time.

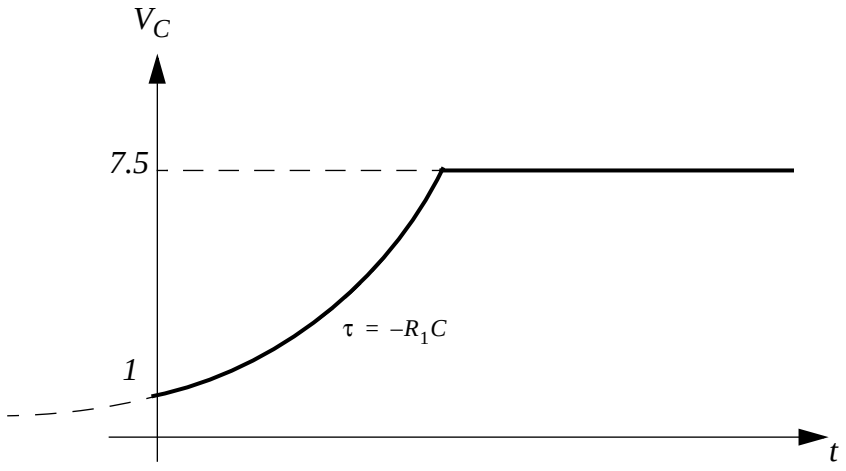


Figure 15.86:

ANS:: (a) $i_{IN} = \frac{v_I N+15}{R_1} for v_{IN} < -7.5V, i_{IN} = -\frac{v_{IN}}{R_1}, for -7.5V < v_{IN} <$

$7.5V, and i_{IN} = \frac{v_I N - 15}{R_1} for v_{IN} > 7.5V.$

Problem 15.25 An operational amplifier is connected as shown in Figure 15.87.

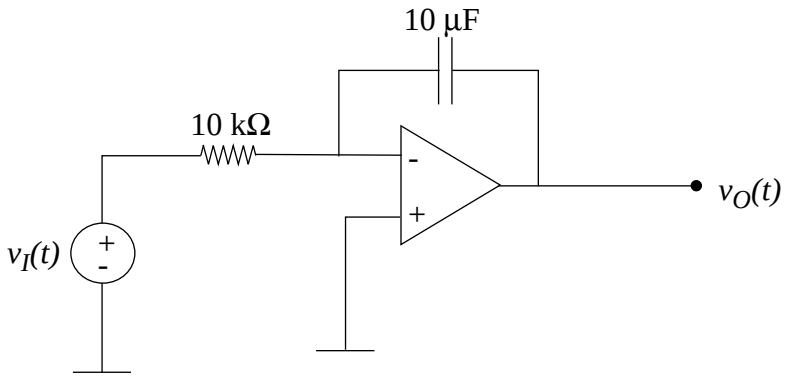


Figure 15.87:

a) Assuming that the amplifier has infinite gain and infinite input resistance and zero output resistance, determine the relationship between $v_O(t)$ and $v_I(t)$.

b) The signal $v_I(t)$ is a rectangular pulse as Figure 15.88.

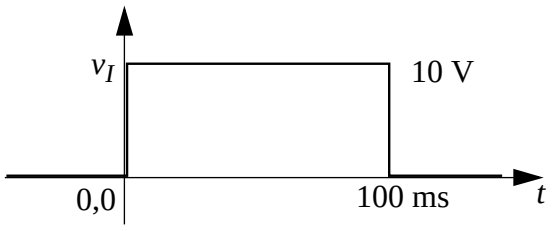


Figure 15.88:

Assuming that $v_O(0) = 0$, draw $v_O(t)$, for $t > 0$.

c) The operational amplifier is now connected as in Figure 15.89.

The voltage $v_O(t)$ is held at zero (by some means not shown) for $t < 0$. The switch is initially in the up position, connecting the $10k\Omega$ resistor to a fixed voltage V_F. At time $t = 100ms$, the switch is thrown to the down position. The observed voltage $v_O(t)$ is shown in Figure 15.90.

Determine the relationship between V_F and τ, the time required for $v_O(t)$ to return to zero volts.

Solution:

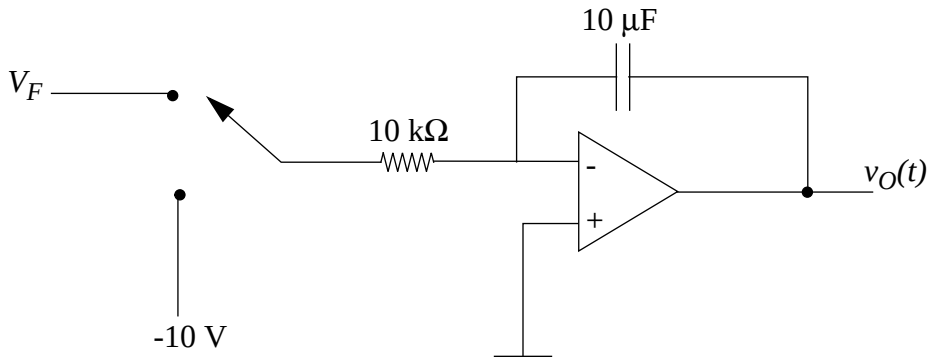


Figure 15.89:

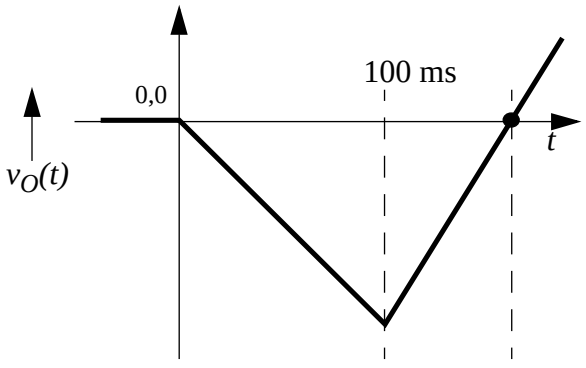


Figure 15.90:

a) $v^- = v^+ = 0$

$i(t) = \frac{v_I(t)}{R} = -C\frac{dv_O(t)}{dt}$

$v_O(t) = \frac{-1}{RC}\int v_I(t)dt$

$v_O(t) = -10\int v_I(t)dt$

b) See Figure 15.91.

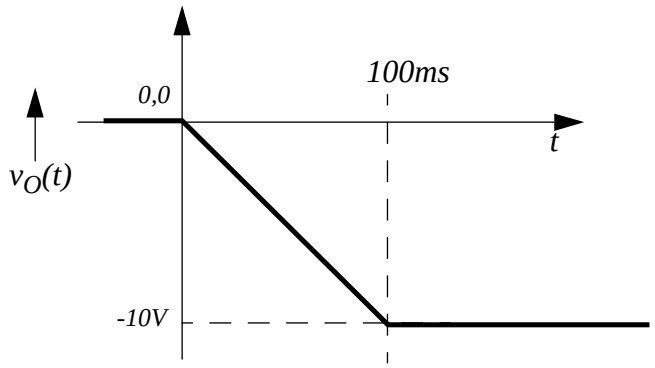


Figure 15.91:

c) $v_{MIN} = -10 \times V_F \times 100ms$

$-10 \times -10 \times \tau = V_F$

$\tau = \frac{V_F}{100}$

ANS:: (c) $\tau = \frac{V_F}{100}$

Problem 15.26 We wish to show that the circuit shown in Figure 15.92 behaves in a manner very similar to an RLC circuit.

a) Write the node equations for v_2 and v_3.

b) Simplify these equations by using the Op Amp assumption, i.e., $v^- \simeq v^+$. This allows you to neglect v_3 terms compared to v_4 terms, and $\frac{dv_3}{dt}$ terms compared to $\frac{dv_2}{dt}$ and $\frac{dv_4}{dt}$ terms, provided C_1 and C_2 are comparable. (You must later check on this last assumption.)

c) Find the characteristic equation. Compare with the RLC case.

d) For the numerical values given below, is the circuit under, over, or critically damped? What is the Q of the circuit, in *literal* form?

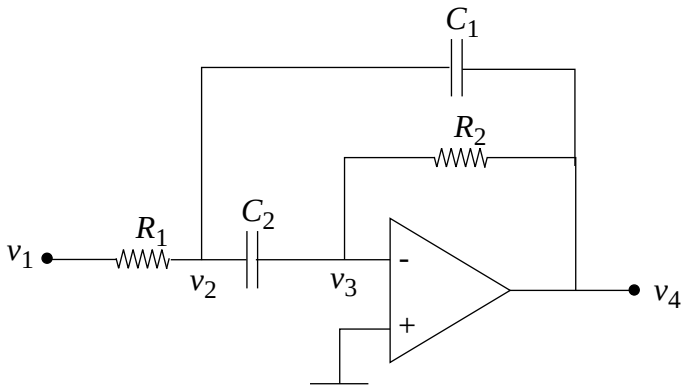


Figure 15.92:

$C_1 = C_2 = .01\mu F$
$R_1 = 10\Omega$
$R_2 = 1k\Omega$

Solution:

First, draw the voltage-source impedance model of the op-amp, since it will come in useful in part b. See Figure 15.93.

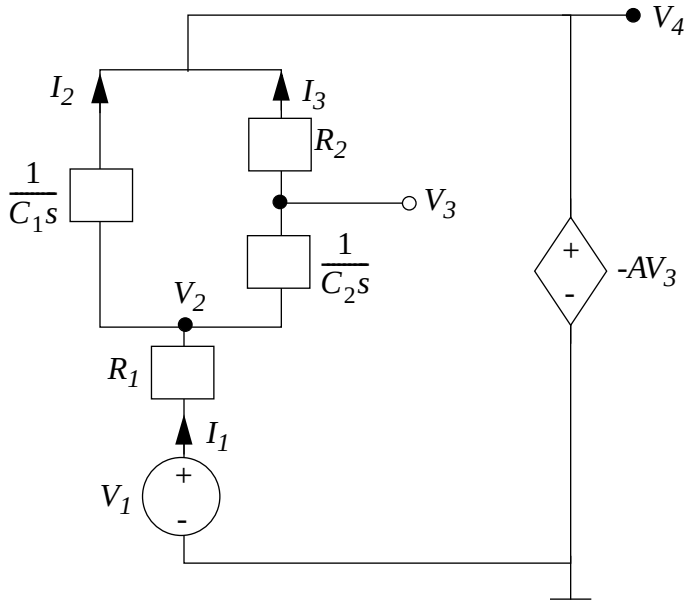


Figure 15.93:

a)

$$\frac{v_1 - v_2}{R_1} = \frac{v_3 - v_4}{R_2} + \frac{v_2' - v_3'}{\frac{1}{C_2}}, \frac{v_2' - v_3'}{\frac{1}{C_2}} = \frac{v_3 - v_4}{R_2}.$$

b) The third necessary condition is $v_4 = -Av_3$. With these three equations, we can derive the following result:

$$-\frac{1}{A}v_4 - v_4 - \frac{1}{A}v_4' R_2 C_2 - R_1(C_1 C_2) - \frac{1}{A}v_4' - R_1(C_1 + C_2)v_4' +$$
$$\frac{1}{A}R_1 C_2 R_2(C_1 + C_2)v_4'' = R_2 C_2 v_1' - \frac{1}{A}v_4'' R_1 C_2 + v_4'' R_1 C_1.$$

Here is where the condition of capacitor size similarity comes in. Ordinarily, one would cancel out all the terms involving $\frac{1}{A}$, since A is infinite in an ideal op-amp. However, in a real op-amp, A is only about 10^6, and it is quite possible for C_1 and $\frac{1}{A}C_2$ to be of comparable size, which devalidates the principle behind the cancellation. Therefore, we must give the condition that the capacitors are of "comparable size", meaning that the ratio of their magnitudes is far less than A.

Given that, we may cancel several terms to get the following result:

$$v_1' R_2 C_2 = -v_4'' R_1 R_2 C_1 C_2 - v_4 - v_4' R_1 C_1 - v_4' R_1 C_2.$$

c) We now let v_1 and v_4 be of the form e^{st}.

We can solve for the ratio $\frac{v_4}{v_1}$, getting the following, which corresponds to the transfer function of an RLC circuit.

$$\frac{v_4}{v_1} = \frac{-R_2 C_2 s}{R_1 C_1 R_2 C_2 s^2 + R_1(C_1 + C_2)s + 1}.$$

d) The damping can be found using the discriminant. For the denominator of the form $As^2 + Bs + C$, the discriminant is $B^2 - 4AC$. In our case, we plug in the numbers and get a negative term, meaning that the circuit is overdamped.

In order to find Q, we recall that for a general transfer function whose denominator is of the form $As^2 + Bs + C, Q = \sqrt{\frac{AC}{B^2}}$. This implies that for our case,

$$Q = \sqrt{\frac{(C_1 + R_2 C_2}{(C_1 + C_2)^2 R_1}}.$$

The circuit is overdamped.

ANS:: (a) $\frac{v_1-v_2}{R_1} = \frac{v_2-v_4}{\frac{1}{C_2 s}} + \frac{v_2-v_3}{\frac{1}{C_2 s}}$, $\frac{v_2-v_3}{\frac{1}{C_2 s}} = \frac{v_3-v_4}{R_2}$. (b) $v_1 R_2 C_2 s = -v_4 R_1 R_2 C_1 C_2 s^2 - v_4 - v_4 R_1 C_1 s - v_4 R_1 C_2 s$. (c) $\frac{v_4}{v_1} = \frac{-R_2 C_2 s}{R_1 C_1 R_2 C_2 s^2 + R_1 (C_1 + C_2) s + 1}$ (d) $Q = \sqrt{\frac{(C_1+R_2 C_2}{(C_1+C_2)^2 R_1}}$, and the circuit is overdamped.

Problem 15.27 What is the differential equation relating to v_O to v_I in the network in Figure 15.94? Assume the Op Amps are ideal.

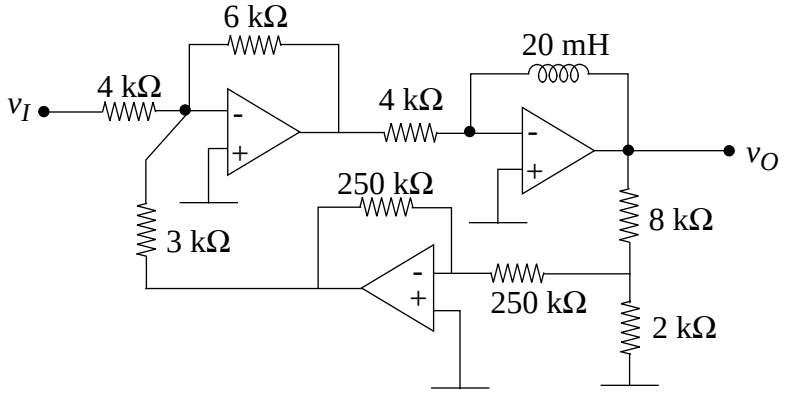


Figure 15.94:

Solution: Label the output of the bottom amplifier before the $3k\Omega$ resistor as node v_X. By superposition, the first op-amp is an inverting amplifier which calculates the sum $-\frac{3}{2}v_I - 2v_X$. The second op-amp is also a differentiator, with gain $-\frac{.02}{4000} = -\frac{1}{200000}$ on the derivative of the input. We now know that $v_O = \frac{1}{200000}(1.5v_I' + 2v_X')$.

The input to the next op-amp is almost an ideal voltage divider, since most of the current going through the $8k\Omega$ resistor is channeled to ground, so the input to the op-amp can be approximated by $.2v_O$. The third op-amp is merely an inverter, so we can calculate that $v_X = -.2v_O$.

We now have:

$$v_O = \frac{1}{200000}(1.5v_I' - .4v_O').$$

This can be simplified to:

$$v_O - 2 * 10^{-6} v_O' = 7.5 * 10^{-6} v_I'.$$

ANS:: $v_O - 2 * 10^{-6} \frac{dv_O}{dt} = 7.5 * 10^{-6} \frac{dv_I}{dt}$.

Problem 15.28 The circuit in Figure 15.95 behaves in a manner very similar to an RLC circuit.

a) Write the node equations.

b) Assume $v_A = V_a e^{st}, v_B = V_b e^{st}$, and find the characteristic equation.

c) Find α and ω_o in terms of C_1, C_2, G_1, G_2.

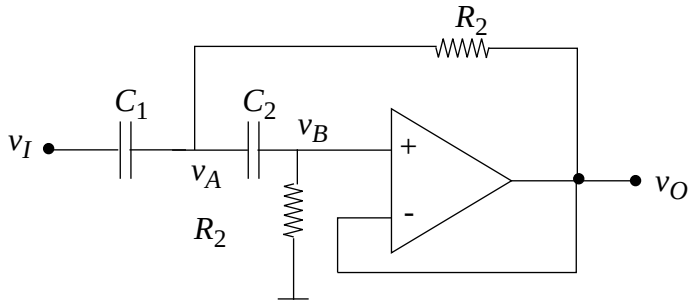


Figure 15.95:

Solution:

This is done most easily by using the impedance model. See Figure 15.96 for the impedance model of this circuit.

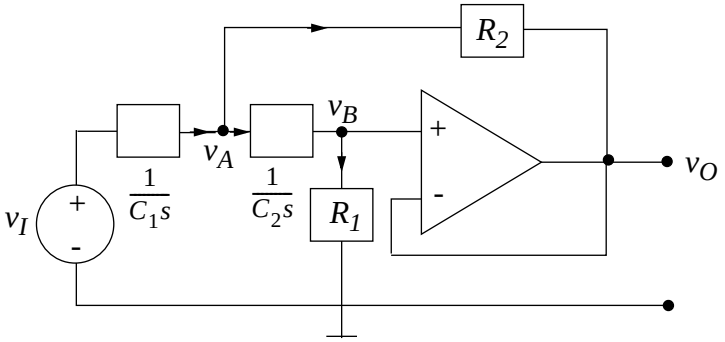


Figure 15.96:

a) If we let G_1 and G_2 be the conductances (the reciprocals of the resistances) corresponding to the two resistors, we get the following two node equations.

$$(v_I - v_A)C_1 s = (v_A - v_B)C_2 s + (v_A - v_O)G_2, v_B G_1 = (v_A - v_B)C_2 s.$$

b) If the op-amp is ideal, then $v_O = v_B$ due to the negative feedback. Simplifying the three equations that we have, we get that:

$$\frac{v_B}{v_1} = \frac{C_1 C_2 R_1 R_2 s^2}{C_1 C_2 R_1 R_2 s^2 + R_2 C_2 s + 1}.$$

c) For a transfer function with denominator $As^2 + Bs + C$, α is defined to be one-half the bandwidth, which is $\frac{B}{2A}$, and the resonance frequency ω_o is $\sqrt{\frac{C}{A}}$. For our case, we get the following values.

$$\alpha = \frac{G_1}{2C_2}, \omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}.$$

ANS:: (a) $(v_I - v_A)C_1 s = (v_A - v_B)C_2 s + (v_A - v_O)G_2, v_B G_1 = (v_A - v_B)C_2 s$, (b) $\frac{v_B}{v_1} = \frac{C_1 C_2 R_1 R_2 s^2}{C_1 C_2 R_1 R_2 s^2 + R_2 C_2 s + 1}$, (c) $\alpha = \frac{G_1}{2C_2}, \omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}$.

Problem 15.29 a) Find $H_1(S) = V_1/V_s$ in Figure 15.97. Plot and dimension $\log|H_1|$ and $\angle H_1$ vs. $\log\omega$.

R_1 = 10 kΩ R_2 = 1 kΩ

C_1 = 1 μF C_2 = 0.01 μF

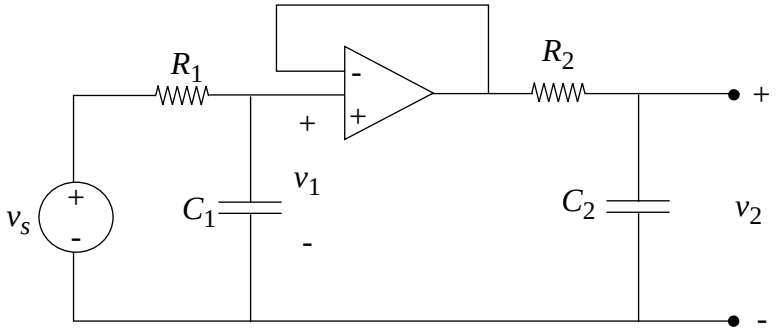


Figure 15.97:

b) Find $H_2(S) = V_2/V_1$. Plot and dimension $\log|H_2|$ and $\angle H_2$ vs. $\log\omega$.

c) Find $H_t(S) = V_2/V_s = H_1(S)H_2(S)$. Plot and dimension $\log|H_t|$ and $\angle H_t$ vs. $\log\omega$. Compare with the plots you obtained in parts a) and b).

Solution:

a) See Figure soln-fig:18-29-a.

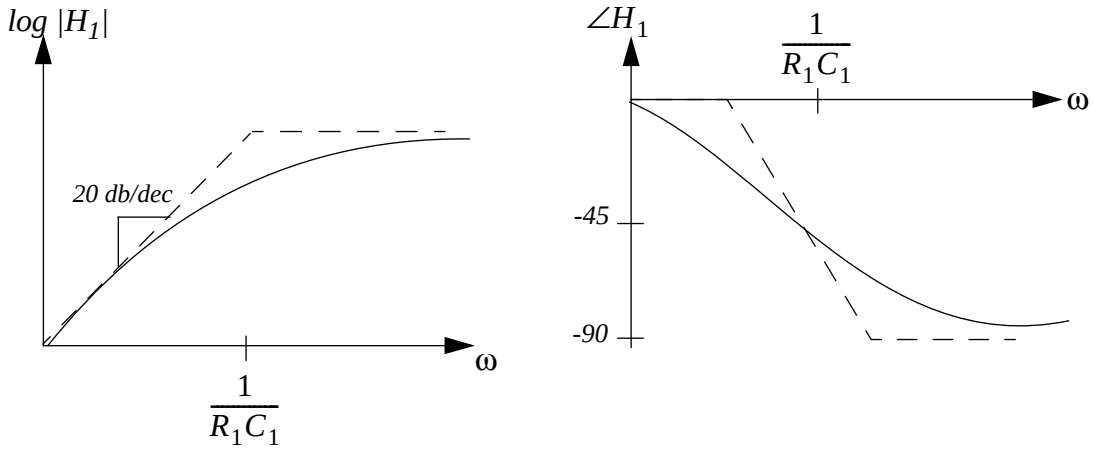


Figure 15.98:

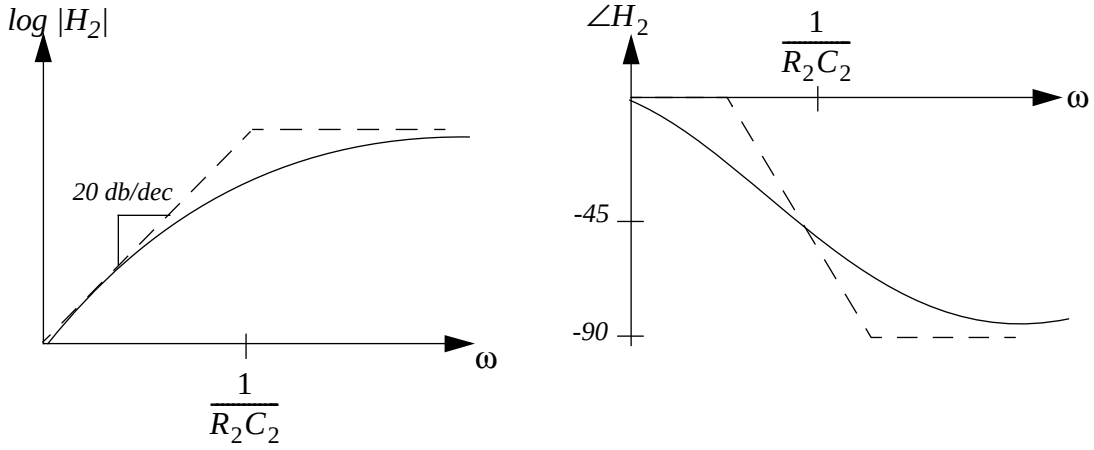


Figure 15.99:

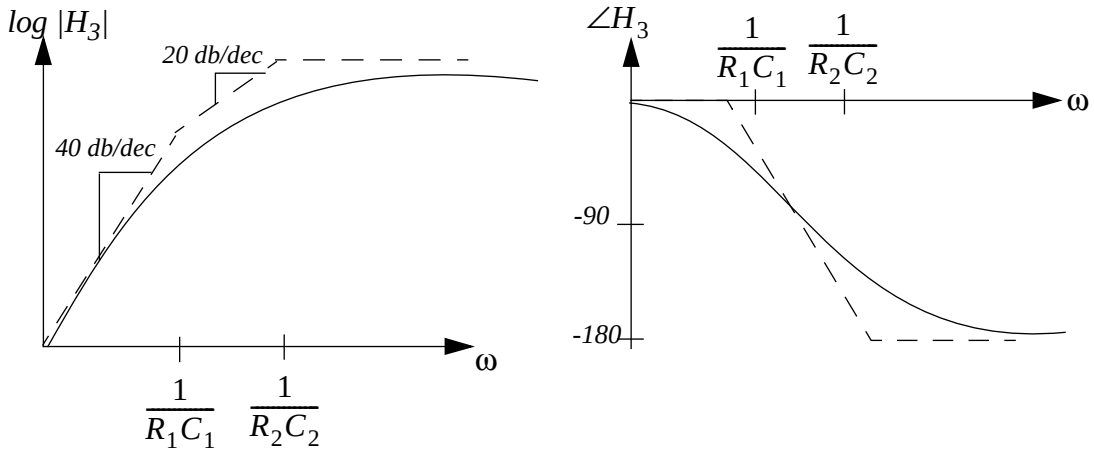


Figure 15.100:

b) See Figure soln-fig:18-29-b.

c) See Figure soln-fig:18-29-c.

Problem 15.30 a) Find the transfer function for the network in Figure 15.101.

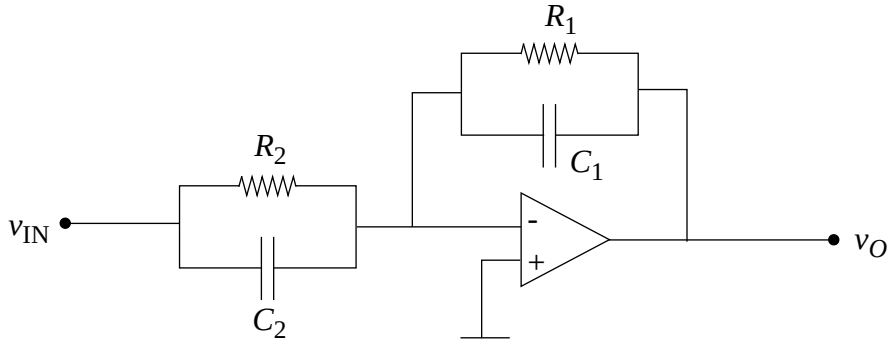


Figure 15.101:

b) Synthesize the function $\frac{V_o}{V_{in}} = -(s+4)/(s+6)$ using the above circuit. That is, find values of R_1, R_2, C_1, and C_2 which satisfy V_o/V_{in}. You may use capacitors of $1\mu F$.

Solution:

a) $\frac{V_o}{V_{in}} = \frac{-Z_F}{Z_{IN}}$

$Z_{IN} = R_2 || \frac{1}{sC_2}$

$Z_F = R_1 || \frac{1}{sC_2}$

$$\frac{V_o}{V_{in}} = \frac{-(sR_1R_2C_2 + R_1)}{sR_1R_2C_1 + R_2}$$

b) Given the previous derivation, we see that we must let C_1 and C_2 be the same, since the magnitude of s must be the same. We use $1\mu F$ capacitors, because we can.

Plugging this in and simplifying, we get the following:

$$-\frac{s + \frac{10^6}{R_2}}{s + \frac{10^6}{R_1}} = -\frac{s+4}{s+6}.$$

This implies that $R_2 = 250k\Omega, R_1 = 167k\Omega$. In order to synthesize these, we can use a $220k\Omega$ in series with a $33k\Omega$, or if more precision is needed, $220k\Omega$ in series with the parallel combination of a $33k\Omega$ and a $330k\Omega$. R_2 can be made from a $220k\Omega$ in parallel with a $680k\Omega$, which turns out to be remarkably precise.

$$C_1 = 1\mu F, C_2 = 1\mu F,$$

$$R_1 = 220k\Omega || 680k\Omega,$$

$$R_2 = 220k\Omega + (33k\Omega || 330k\Omega).$$

ANS:: (a) $\frac{V_o}{V_{in}} = \frac{-(sR_1R_2C_2+R_1)}{sR_1R_2C_1+R_2}$, (b) $C_1 = 1\mu F, C_2 = 1\mu F, R_1 = 220k\Omega||680k\Omega, R_2 = 220k\Omega + (33k\Omega||330k\Omega)$.

Problem 15.31 The circuit shown in Figure 15.102 is a capacitance multiplier. It may be incorporated into circuits which might otherwise require unrealistically large physical capacitors. You may assume that the operational amplifier has ideal characteristics.

a) Find the impedance Z looking into terminal A-A' for the circuit.

b) Show that the model on the right corresponds to an impedance equivalent to the result obtained in part a).

c) For $R_1 = R_2 = 10M\Omega, R_3 = 1k\Omega$, what is C_{eq} in terms of C?

Solution:

See Figure 15.103.

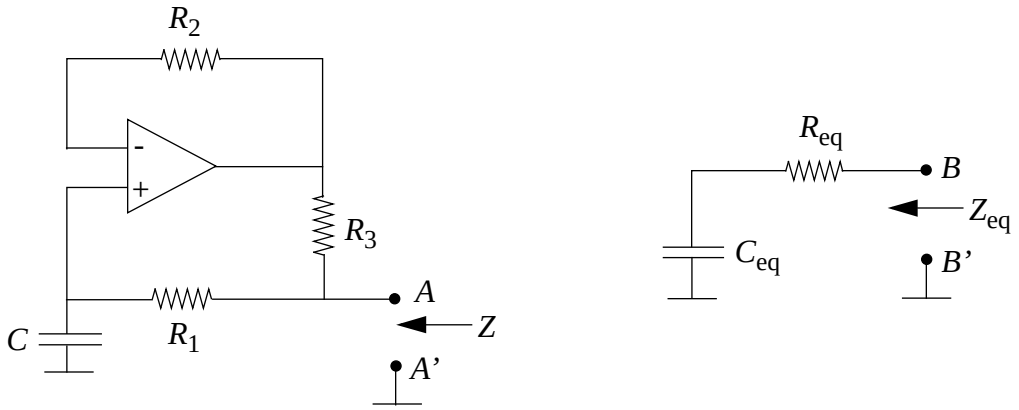


Figure 15.102:

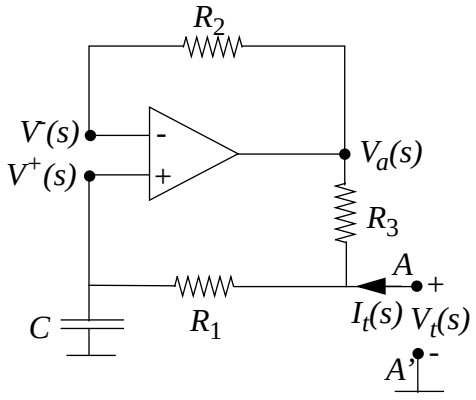


Figure 15.103:

a) $V^+ = V^-$

$i^+ = 0$, therefore $V_a = V^-$

Analyze the current I_t from test voltage with complex amplitude V_t.

$V^+ = \frac{\frac{1}{sC}}{R_1+\frac{1}{sC}} V_t$

$I_t = \frac{V_t - V_a}{R_3} + \frac{V_t - V_a}{R_1}$

$Z_{eq} = \frac{R_3}{R_1+R_3}(\frac{1}{sC} + R_1)$

b) $Z_{eq} = \frac{1}{sC_{eq}} + R_{eq}$

c) $R_{eq} = \frac{R_1 R_3}{R_3+R_1}$

$C_{eq} = C \times \frac{R_3+R_1}{R_3}$

$C_{eq} = C \times 10001$

Problem 15.32 Show that the Op Amp circuit in Figure 15.104 has the same form of transfer function as the circuit in Problem 14.1 (shown on the left hand side of Figure 15.104). Find expressions for the resonant frequency and the Q.

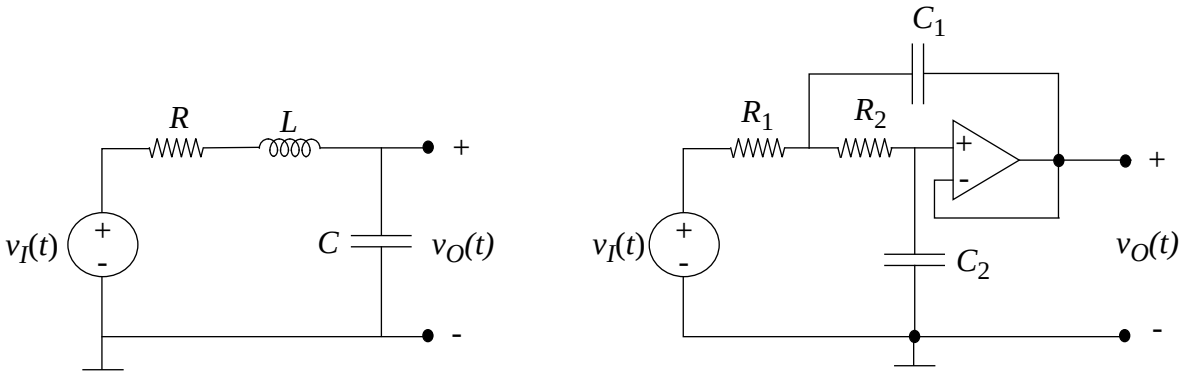


Figure 15.104:

Solution:

This is actually the same as Problem 15.28 but with the resistors and the capacitors switched. We recall the equation derived in Problem 15.28, part B:

$$v_1 C_1 C_2 s^2 = v_0 C_1 C_2 s^2 + v_0 G_1 C_2 s + v_0 G_1 G_2.$$

We replace the admittances as necessary:

$$C_1 s \Rightarrow G_1, C_2 s \Rightarrow G_2, G_1 \Rightarrow C_1 s, G_2 \Rightarrow C_2 s.$$

From that, we get the following transfer function:

$$\frac{v_O}{v_I} = \frac{G_1 G_2}{C_1 C_2 s^2 + G_2 C_2 s + G_1 G_2}.$$

This is equivalent to pulling the voltage across a capacitor in a series RLC circuit. The resonance frequency of a transfer function with denominator of the form $As^2 + Bs + C$ is $\sqrt{\frac{C}{A}}$, and Q is $\sqrt{\frac{AC}{B^2}}$. We substitute, getting the following values:

ANS:: $\omega_o = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}, Q = \sqrt{\frac{C_2 R_2}{C_1 R_1}}$.

Problem 15.33 The circuit in Figure 15.105 is a switched capacitor filter. The switches S_1 and S_2 are driven by nonoverlapping clocks as in Problem 15.15. Both S_1 switches are closed for time $1/2f_c$ with S_2 open, and S_2 closed for $1/2f_c$ with S_1 open. $V_{in} = A\cos\omega t, \quad \omega << 2\pi f_0$.

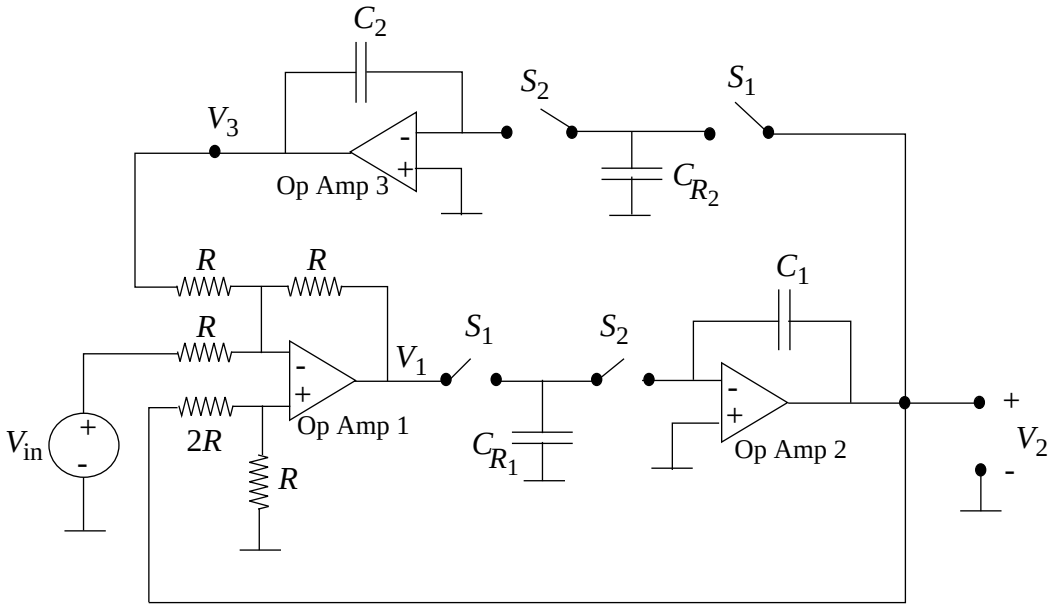


Figure 15.105:

a) Find (in the sinusoidal steady state) the transfer functions V_3/V_2 and V_2/V_1. Refer to Problem 15.15 to see how to handle the switches. Note that there are no switches across C_1 and C_2.

b) Now find a simple equation to describe the operation of Op Amp 1, i.e., find an expression for V_1 in terms of V_2, V_{in}, and V_3. Note that in all of our impedance calculations, we have been implicitly assuming that the relation among V's for such a circuit is the same as the relation among the time variables $v(t)$.

c) Now substitute from a) into b) to find the overall transfer function V_2/V_{in}. Find expressions for the resonant frequency ω_0 and the bandwidth $\Delta\omega$ in terms of the circuit constants. The easiest way to do this is to get the transfer function into the form

$$V_o = \frac{K_s V_{in}}{s^2 + 2\alpha s + \omega_0^2} \tag{15.1}$$

and work by analogy to the parallel RLC case. How does the resonant frequency ω_0 depend on the clock frequency f_c?

Solution:

First, let the effective resistances of the switched capacitors be R_1 and R_2.

a) The second and third op-amps are both integrators, and have the following transfer characteristics:

$$\frac{V_2}{V_1} = \frac{-1}{R_1 C_1 s}, \frac{V_3}{V_2} = \frac{-1}{R_2 C_2 s}.$$

b) The first op-amp is similar to the one detailed in Problem 15.8, except has only two inputs instead of three. Therefore, it has the following transfer characteristic.
$V_1 = \frac{V_2 R}{2R+R}\left(1 + \frac{R}{R} + \frac{R}{R}\right) - R\left(\frac{V_3}{R} + \frac{V_{IN}}{R}\right)$.
This simplifies to:

$$V_1 = V_2 - V_3 - V_{IN}.$$

c) We substitute into the previous equation, getting:

$$V_2 R_1 C_1 s = V_2 - \frac{V_2}{R_2 C_2 s} - V_{IN}.$$

This can be transformed into:

$$\frac{V_2}{V_{IN}} = \frac{R_2 C_2 s}{R_1 R_2 C_1 C_2 s^2 - R_2 C_2 s + 1}.$$

From here, we can get the resonant frequency ω_0 and the bandwidth $\Delta = omega$, since for any transfer function with denominator $As^2 + Bs + C$, the resonant frequency is $\sqrt{\frac{C}{A}}$ and the bandwidth is $\frac{B}{A}$.

$$\frac{V_2}{V_{IN}} = \frac{R_2 C_2 s}{R_1 R_2 C_1 C_2 s^2 - R_2 C_2 s + 1}, \Delta\omega = \frac{1}{R_1 C_1}, \omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}.$$

ANS:: (a) $\frac{V_2}{V_1} = \frac{-1}{R_1 C_1 s}, \frac{V_3}{V_2} = \frac{-1}{R_2 C_2 s}$, (b) $V_1 = V_2 - V_3 - V_{IN}$, c) $\frac{V_2}{V_{IN}} = \frac{R_2 C_2 s}{R_1 R_2 C_1 C_2 s^2 - R_2 C_2 s + 1}, \Delta\omega = \frac{1}{R_1 C_1}, \omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$.

Problem 15.34 The circuit shown in Figure 15.106 behaves like an RLC circuit.

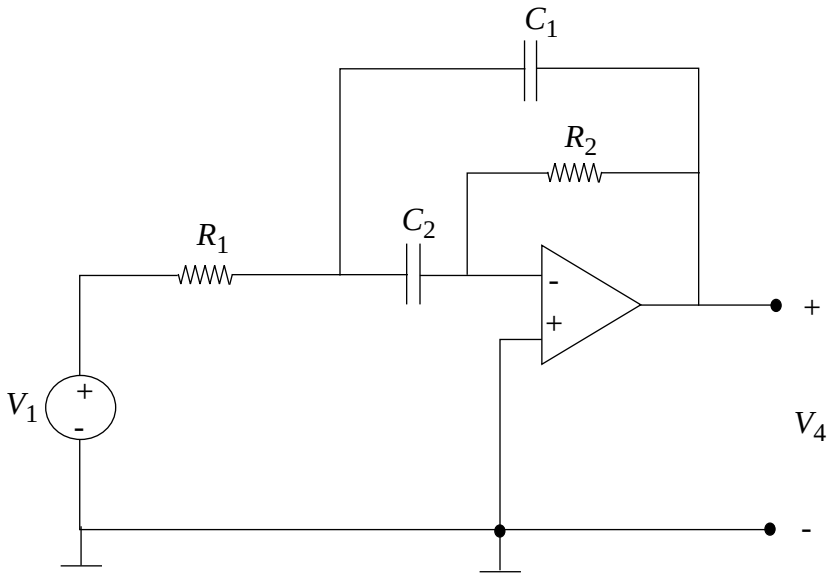


Figure 15.106:

a) Find the transfer function V_4/V_1. (You may assume that the Op Amp is ideal, i.e. $V^+ = V^-$ to simplify your calculations.)

b) Sketch the magnitude of the transfer function $|V_4/V_1|$ versus frequency. Indicate the frequency at which the peak occurs, the magnitude of the transfer function at the peak, and the Q of the resonance. Use the following numerical values:

$C_1 = C_2 = 0.01\mu F \quad R_1 = 10\Omega \quad R_2 = 1k\Omega$

c) This circuit is known as an RC active filter. Is it a low-pass, high-pass, or hand-pass filter? What is the expression for bandwidth in terms at $R_1, C_1,$ etc.? That is, $B = \omega_2 - \omega_1$ where ω_1 and ω_2 are the half power frequencies?

Solution:

This is a continuation of Problem 15.26.

a) From Problem 15.26, part C, we get the transfer function:

$$\frac{v_4}{v_1} = \frac{-R_2 C_2 s}{R_1 C_1 R_2 C_2 s^2 + R_1 (C_1 + C_2) s + 1}$$

b) See Figure soln-fig:18-34-same-as-38.

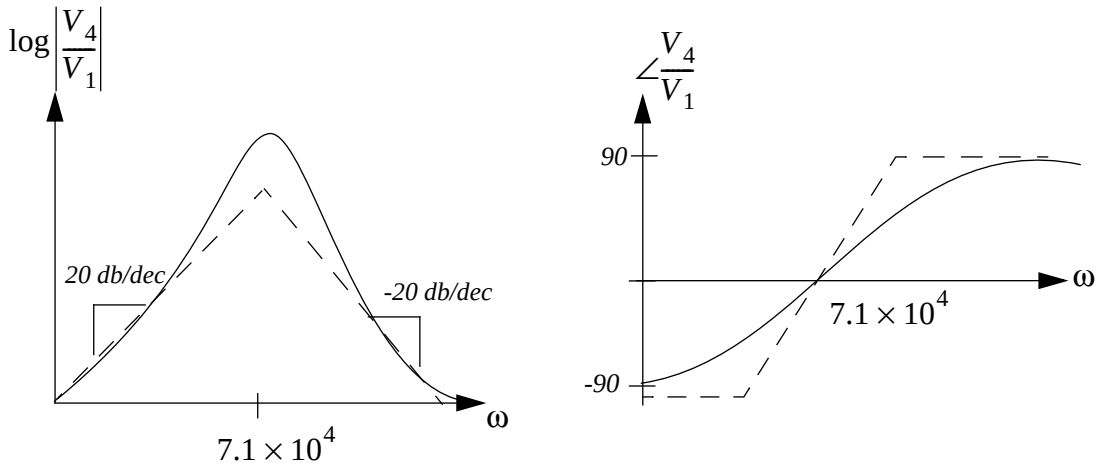


Figure 15.107:

c) Since the numerator contains a linear term in s and the denominator a quadratic, this is a band-pass filter. The bandwidth for any function with the denominator $As^2 + Bs + C$ is $\frac{B}{A}$, so in this case we get a bandwidth of:

$$\frac{C_1 + C_2}{R_1 C_1 C_2}.$$

ANS:: (a) $\frac{v_4}{v_1} = \frac{-R_2 C_2 s}{R_1 C_1 R_2 C_2 s^2 + R_1 (C_1 + C_2) s + 1}$, (b) $\frac{C_1 + C_2}{R_1 C_1 C_2}$.

Problem 15.35 a) Find an expression for the complex amplitude ratio V_o/V_i for the active filter circuit in Figure 15.108, given that $R_2 = 10R_1$. Sketch the Bode plot, $|V_o/V_i|$ versus ω and V_o/V_i versus ω.

b) An equivalent filter can be made with the circuit shown in Figure 15.109. Find the value of C_2 needed to make a filter equivalent to that in part a), assuming that R_1 and R_2 are the same here as for part a). How does the value of C_x here compare to that of C in the filter of part a)?

Solution:

a) $\frac{V_o}{V_i} = \frac{-Z_F}{Z_{IN}} = \frac{-R_2 || \frac{1}{sC}}{R_1}$

$\frac{V_o}{V_i} = \frac{R_2}{sCR_2R_1 + R_1}$

Given that $R_2 = 10R_1$, we substitute in, getting:

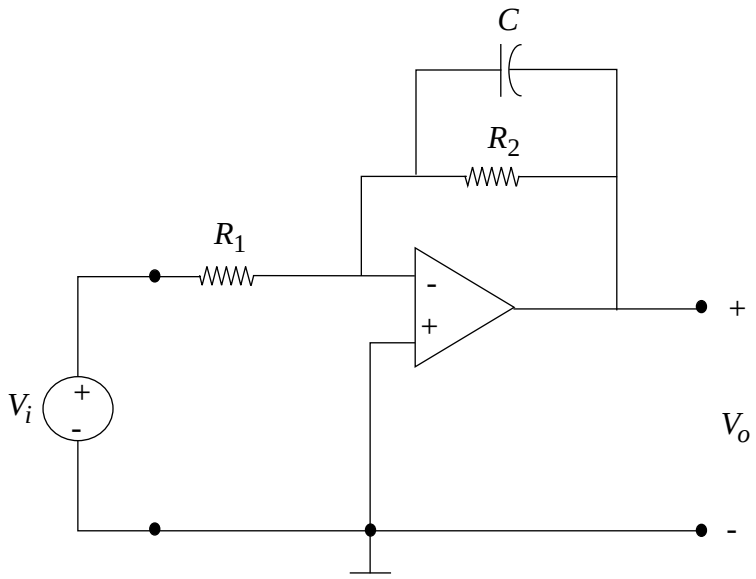


Figure 15.108:

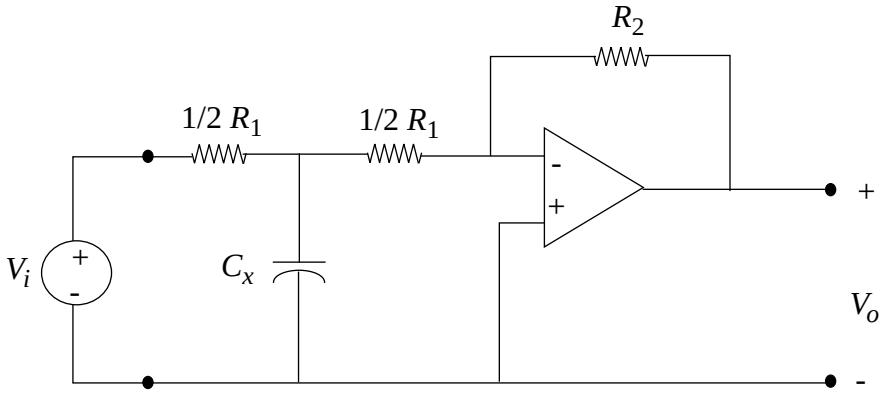


Figure 15.109:

$$\frac{V_O}{V_I} = \frac{-10}{10R_1Cs + 1}.$$

See Figure soln-fig:18-35 for the Bode plot.

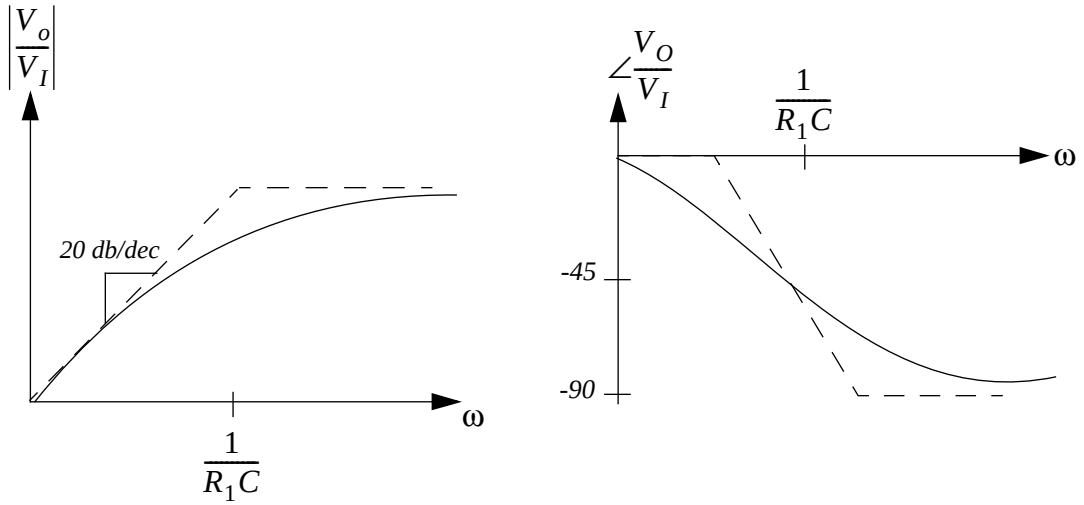


Figure 15.110:

b) First, find the Thevenin equivalent of the input. The open-circuit voltage is given by a voltage divider rule:

$$V_{TH} = V_I \frac{\frac{1}{C_x s}}{\frac{1}{2}R_1 + \frac{1}{C_x s}}.$$

This can be simplified to:

$$V_{TH} = V_I \frac{2}{R_1 C_x s + 2}.$$

The Thevenin impedance is found by shorting out the voltage source:

$$Z_{TH} = \frac{1}{2}R_1 + (\frac{1}{2}R_1 || \frac{1}{C_x s}).$$

This simplifies to:

$$Z_{TH} = \frac{R_1^2 C_x s + 4R_1}{2R_1 C_x s + 4}.$$

This is now a standard inverting amplifier configuration:

$$V_O = V_{TH}\frac{-R_2}{Z_{TH}}.$$

Substituting in, we get:

$$\frac{V_O}{V_I} = \frac{-4R_2}{R_1^2 C_x s + 4R_1} = \frac{-40}{R_1 C_x s + 4}.$$

Comparing this result to that derived in part A, we get that:

$$C_x = 40C.$$

ANS:: (a) $\frac{V_O}{V_I} = \frac{-10}{10R_1Cs+1}$., (b) $C_x = 40C$.

Problem 15.36 The circuit shown in Figure 15.111 behaves in a way very similar to an RLC circuit.

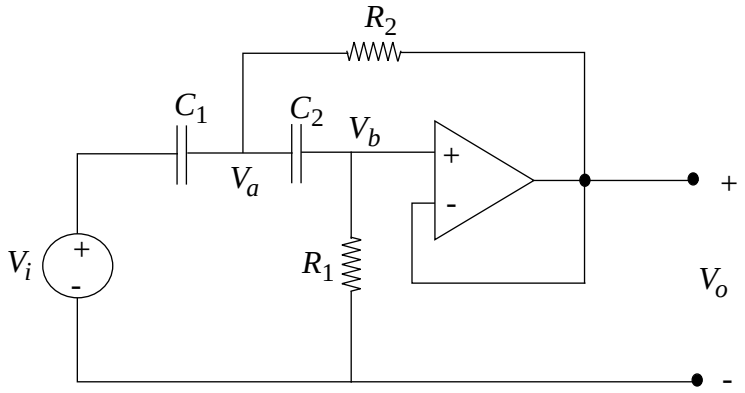


Figure 15.111:

a) Write the sinusoidal steady state node equations for the complex amplitudes V_a and V_b.

b) Solve for V_o/V_i using the results in a), and noting that $V_o = V_b$.

c) Assuming the circuit is underdamped, sketch the magnitude of the transfer function $|V_o/V_i|$ versus frequency. Indicate the frequency at which the peak occurs, the magnitude of the transfer function at the peak, and the Q of the resonance.

Solution:

a) $\frac{V_i - V_a}{\frac{1}{sC_1}} + \frac{V_b - V_a}{\frac{1}{sC_2}} + \frac{V_o - V_a}{R_2} = 0$

$\frac{V_a - V_b}{\frac{1}{sC_2}} - \frac{V_b}{R_1} = 0$

b) Doing a bit of algebra, one gets that:

$$\frac{V_O}{V_I} = \frac{R_1 R_2 C_1 C_2 s^2}{R_1 R_2 C_1 C_2 s^2 + R_2(C_1 + C_2)s + 1}.$$

c) See Figure soln-fig:18-36.

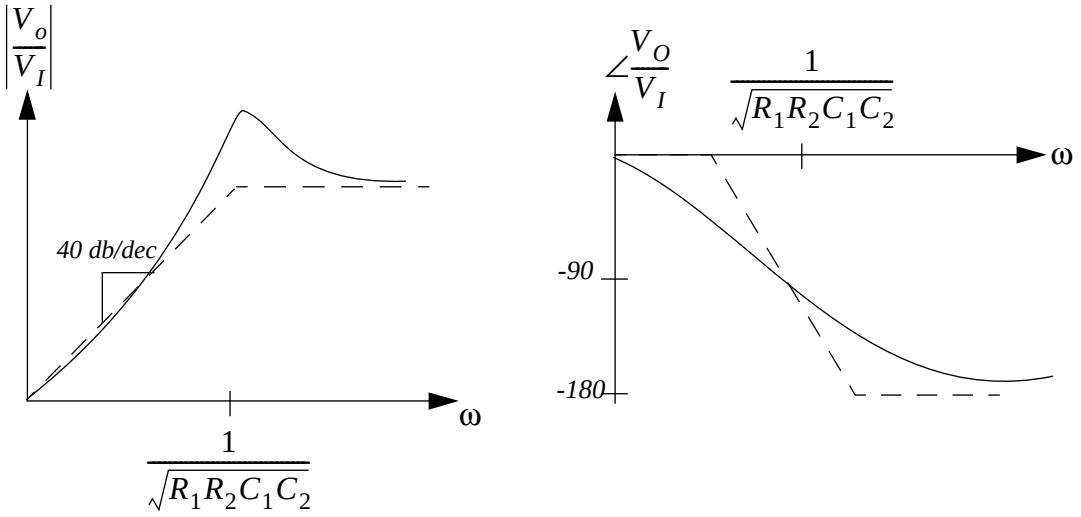


Figure 15.112:

The frequency at which the peak occurs is the resonance frequency, ω_o, and can be determined from the transfer function whose denominator is $As^2 + Bs + C$ by finding $\sqrt{\frac{C}{A}}$, which turns out to be $\sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$. To find the magnitude at this frequency, substitute in for s, remembering that $s = j\omega$, and after a bit of simplification, getting:

$$\frac{V_O}{V_I}|_{\omega_o} = \sqrt{\frac{R_1}{R_2}}\frac{\sqrt{C_1 C_2}}{C_1 + C_2}.$$

The value of Q can be determined by finding $\sqrt{\frac{AC}{B^2}}$, and it turns out to be the square of the magnitude of the peak.

$$\omega_o = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}, \frac{V_O}{V_I}|_{\omega_o} = \sqrt{\frac{R_1}{R_2}}\frac{\sqrt{C_1 C_2}}{C_1 + C_2}, Q = \frac{C_1 C_2 R_1}{(C_1 + C_2)^2 R_2}.$$

ANS:: (b) $\frac{V_O}{V_I} = \frac{R_1 R_2 C_1 C_2 s^2}{R_1 R_2 C_1 C_2 s^2 + R_2(C_1+C_2)s+1}$., (c) $\omega_o = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}, \frac{V_O}{V_I}|_{\omega_o} = \sqrt{\frac{R_1}{R_2}}\frac{\sqrt{C_1 C_2}}{C_1+C_2}, Q = \frac{C_1 C_2 R_1}{(C_1+C_2)^2 R_2}$.

Problem 15.37 Plot the frequency response (magnitude and phase) of the active filter shown in Figure 15.113. Assume the Op Amp is ideal.

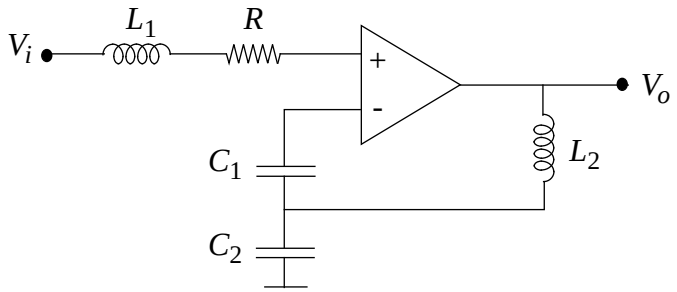


Figure 15.113:

Solution: First, redraw the impedance model of the op-amps shown in Figure 15.114. L_1, R, and C_1 can be omitted since no current ever flows through them. This is a standard non-inverting op-amp configuration. The voltage at node V_X is equal to V_i since the op-amp is assumed to be ideal, and there is negative feedback. A simple voltage-divider relationship ensues.

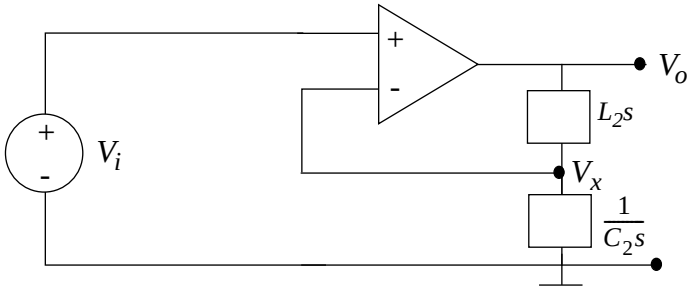


Figure 15.114:

$$V_i = V_o \frac{L_2 s}{L_2 s + \frac{1}{C_2 s}}.$$

This can be solved for V_o and simplified:

ANS:: $V_o = V_i \frac{C_2 L_2 s^2 + 1}{C_2 L_2 s^2}$.

See Figure soln-fig:18-37-2 for the frequency response.

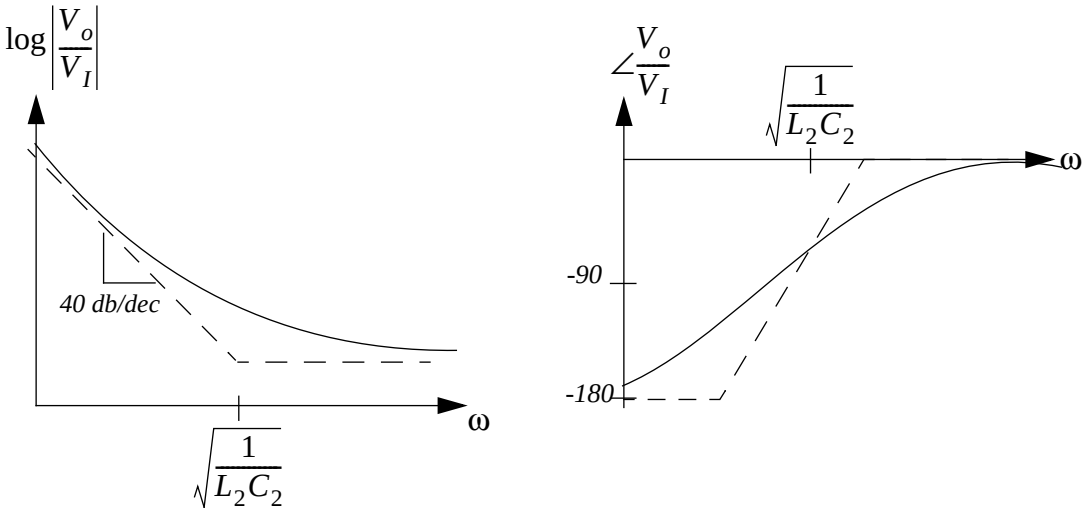


Figure 15.115:

Problem 15.38 The circuit shown in Figure 15.116 has a resonance very similar to an RLC circuit.

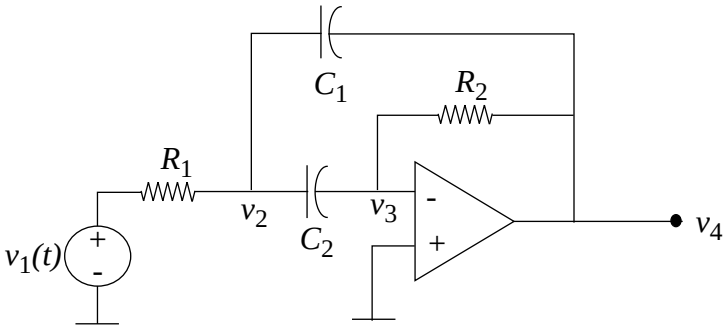


Figure 15.116:

a) Write the sinusoidal steady-state equations for V_2 and V_3.

b) Solve for V_4/V_1 using the results in a), and noting that $V_3 = -V_4/A$, where the Op Amp gain A can be assumed to be very large.

c) Assuming now that $C_1 = C_2 = 0.1\mu F$, $R_1 = 10\Omega$, $R_2 = 1k\Omega$, sketch the magnitude of the transfer function $|V_4/V_1|$ versus frequency. Indicate the frequency at which the peak occurs, the magnitude of the transfer function at the peak, and the Q of the resonance.

Solution:

a) This has been already done in Problem 15.26.

$$\frac{v_1 - v_2}{R_1} = \frac{v_2 - v_4}{\frac{1}{C_2 s}} + \frac{v_2 - v_3}{\frac{1}{C_2 s}}, \frac{v_2 - v_3}{\frac{1}{C_2 s}} = \frac{v_3 - v_4}{R_2}.$$

b) This was also done in Problem 15.26. This intermediate result was derived.

$$(1 + R_1 C_2 s + R_1 C_1 s)(-\frac{1}{A} v_4 - v_4 - \frac{1}{A} v_4 R_2 C_2 s) =$$

$$(v_1 - \frac{1}{A} v_4 R_1 C_2 s + v_4 R_1 C_1 s)(R_2 C_2 s).$$

If we assume that the capacitors are of comparable magnitude, then we may cancel several terms to get the following result:

$$\frac{v_4}{v_1} = \frac{-R_2 C_2 s}{R_1 C_1 R_2 C_2 s^2 + R_1 (C_1 + C_2) s + 1}$$

c) Substituting in the values given, we get a transfer characteristic of:

$$\frac{v_4}{v_1} = \frac{-10^{-4} s}{10^{-10} s^2 + 2 * 10^{-6} s + 1}.$$

For any transfer function whose denominator is of the form $As^2 + Bs + C$, the frequency of the peak ω_o is given by $\sqrt{\frac{C}{A}}$, the magnitude at the peak may be found by substitution, and the factor Q can be found by finding $sqrt\frac{AC}{B^2}$. For our function, we get:

$$\omega_o = 10^5, \frac{v_4}{v_1}|_{\omega_o} = 50, Q = 250.$$

See Figure 15.117 for the Bode plot.

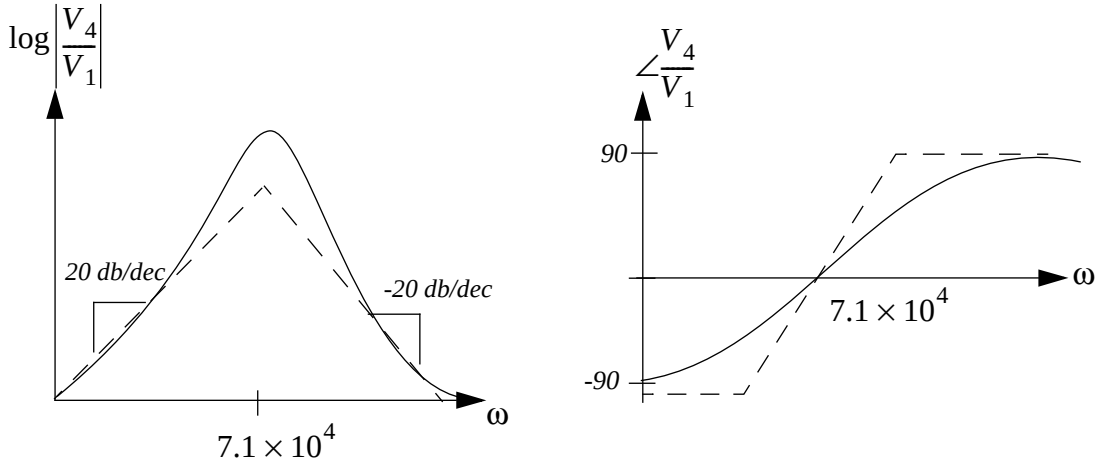


Figure 15.117:

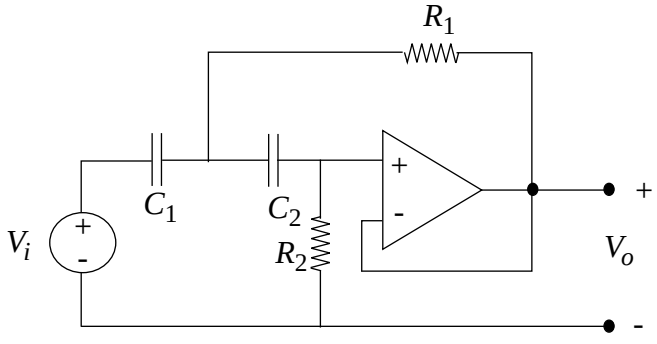


Figure 15.118:

ANS:: (a) $\frac{v_1-v_2}{R_1} = \frac{v_2-v_4}{\frac{1}{C_2 s}} + \frac{v_2-v_3}{\frac{1}{C_2 s}}$, $\frac{v_2-v_3}{\frac{1}{C_2 s}} = \frac{v_3-v_4}{R_2}$., (b) $\frac{v_4}{v_1} = \frac{-R_2 C_2 s}{R_1 C_1 R_2 C_2 s^2 + R_1(C_1+C_2)s+1}$, (c) $\omega_o = 10^5$, $\frac{v_4}{v_1}|_{\omega_o} = 50, Q = 250$.

Problem 15.39 For the circuit in the figure in Figure 15.118

a) Find a set of equations which, if solved, would give V_o/V_i.

b) Assuming that these equations, when solved, yield

$$V_o/V_i = \frac{(j\omega C_1)(j\omega C_2)}{G_1 G_2 + j\omega(C_1+C_2)G_2 + (j\omega)^2 C_1 C_2} \tag{15.2}$$

Find the expression for the undamped resonant frequency (ω_0) of the circuit.

c) Find an expression for the low-frequency asymptote of V_o/V_i. (Zero is not an acceptable answer.)

d) Find an expression for the high-frequency asymptote of V_o/V_i. (Zero is not an acceptable answer.)

e) Assuming $Q = 1/2$, sketch the magnitude and phase of V_o/V_i versus ω. Specify coordinates, and dimension key features.

Solution:

a) This was already done in Problem 15.36. The equation derived there will be used here, except with resistors R_1 and R_2 switched.

$$\frac{V_O}{V_I} = \frac{R_1 R_2 C_1 C_2 s^2}{R_1 R_2 C_1 C_2 s^2 + R_1(C_1+C_2)s + 1}.$$

b) The assumption is valid. The resonance frequency of any transfer function with denominator of the form $A(j\omega)^2 + Bj\omega + C$ is given by $\sqrt{\frac{C}{A}}$. In this case, it is:

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}.$$

c) Since this is a high-pass filter, the asymptote in a linear plot is indeed zero, but in a logarithmic plot, it is a line with a non-zero slope. Since the filter is second-order, the slope will be 2.

We also know that the low-frequency and high-frequency asymptotes cross at the resonance value, and the high frequency asymptote is a horizontal line with value 1, we can find the line, since it goes through the point $(\omega_o, 1)$ and has slope 2. The line is:

$$\left|\frac{V_o}{V_i}\right| = 2(\omega - \omega_o) + 1.$$

d) The high-pass filter will reach a constant value, and since the $(j\omega)^2$ coefficient of the numerator and the denominator are the same, this constant is one.

$$\left|\frac{V_o}{V_i}\right| = 1.$$

e) See Figure soln-fig:18-39.

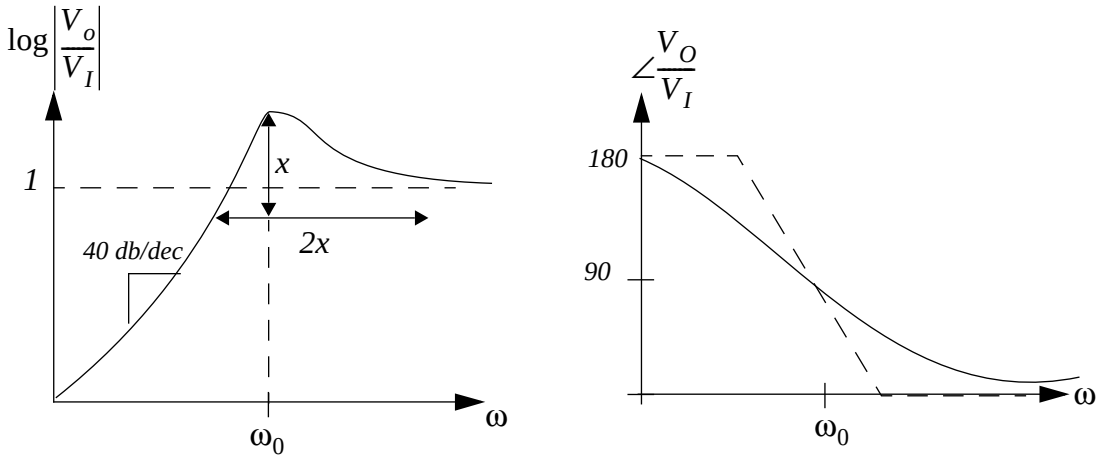


Figure 15.119:

ANS:: (a)$\frac{V_O}{V_I} = \frac{R_1R_2C_1C_2s^2}{R_1R_2C_1C_2s^2+R_1(C_1+C_2)s+1}$, (b) $\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}}$, (c) $\left|\frac{V_o}{V_i}\right| = 2(\omega - \omega_o) + 1$, (d) $\left|\frac{V_o}{V_i}\right| = 1$.

Problem 15.40 Tech Hi-Fi advertises a car stereo system that can deliver 10 watts average power into a 4Ω-speaker. Given your demonstrated proficiency in electronics, you decide to build one using an (hefty) Op Amp. To save yourself the problems associated with designing the receiver you plan to use a small transistor AM-FM radio as the signal source.

You try the circuit shown in Figure 15.120.

In the following parts, you may assume that the hefty Op Amp has very high open-loop gain, zero output resistance, infinite input resistance, and other good features.

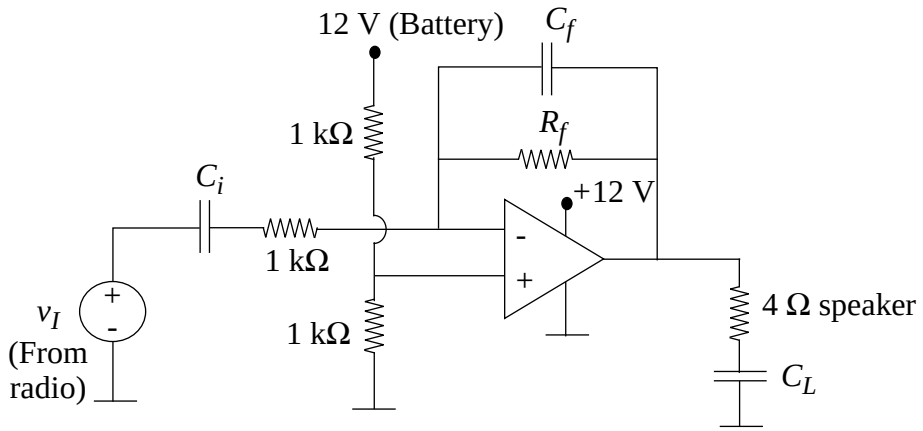


Figure 15.120:

a) What is the operating point value of the voltage at the output of the operational amplifier?

b) Why is capacitor C_L included?

c) Assume that the maximum signal from your radio is 1 volt peak to peak. What is the maximum value of R_f that insures the operational amplifier will remain in the linear region?

d) What is the maximum average power that can be delivered to the 4Ω speaker with v_I is a constant amplitude sinusoid?

e) In spite of your answer to parts b) and c), assume that you choose $R_f = 10k\Omega$ and that capacitor C_L is very large. In order to reduce low frequency noise, you decide that you should make the lower half-power frequency 100 radians per second. What value of C_i should be selected? You also want to filter high frequency noise by making the upper half-power frequency 10^5 radians per second. What value of C_f should be selected?

Solution:

a) 6 volts

b) C_L is included because all items have a load capacitance associated with them.

c) The output voltage of the opamp must be between 0 and 12 volts. Therefore, the maximum value of R_f is:

12 kΩ.

d) Maximum output signal is 12 volts peak-to-peak. This equals $\frac{6}{\sqrt{2}}$ volts RMS.

Power $= \frac{V_{RMS}^2}{R}$

$$3\sqrt{2}voltsRMS, 4.5watts.$$

e) The gain of the amplifier can be calculated using the impedance model shown in Figure 15.121 to be:

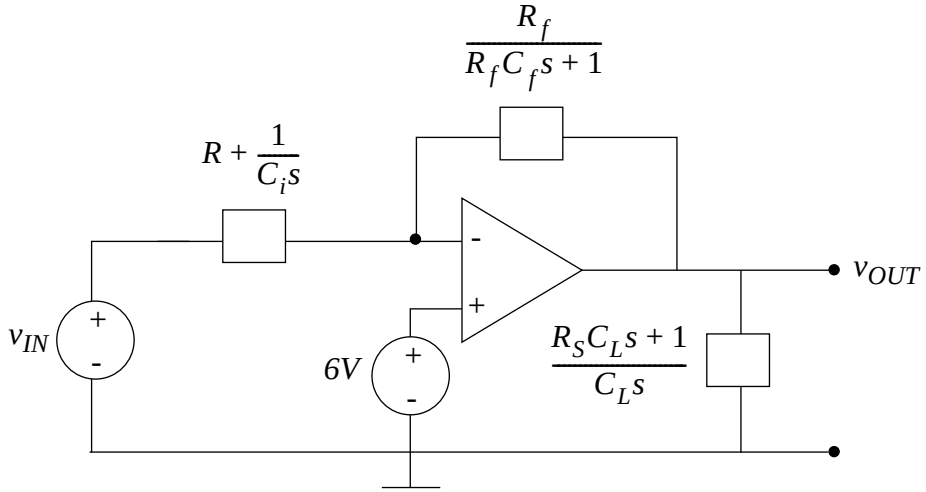


Figure 15.121:

$$\frac{v_O UT}{v_I N} = \frac{-10^3 C_i s}{10^7 C_i C_f s^2 + 10^3 C_i s + 10^4 C_f s + 1}.$$

We must set the magnitude of this gain to be $\sqrt{\frac{1}{2}}$ times the magnitude at resonance, which is 1. Plugging in $s = j\omega$ and simplifying, we come up with the following:

$$\omega = \frac{1}{10^4 C_f}, \frac{1}{10^3 C_i}.$$

Plugging in the desired half-power frequencies, we get the following:

$$C_f = 10^{-9}F, C_i = 10^-5F.$$

ANS:: (a) 6 volts, (b) C_L is included because all items have a load capacitance associated with them, (c) 12 kΩ, (d) $3\sqrt{2}voltsRMS, 4.5watts$, (e) $C_f = 10^{-9}F, C_i = 10^-5F.$

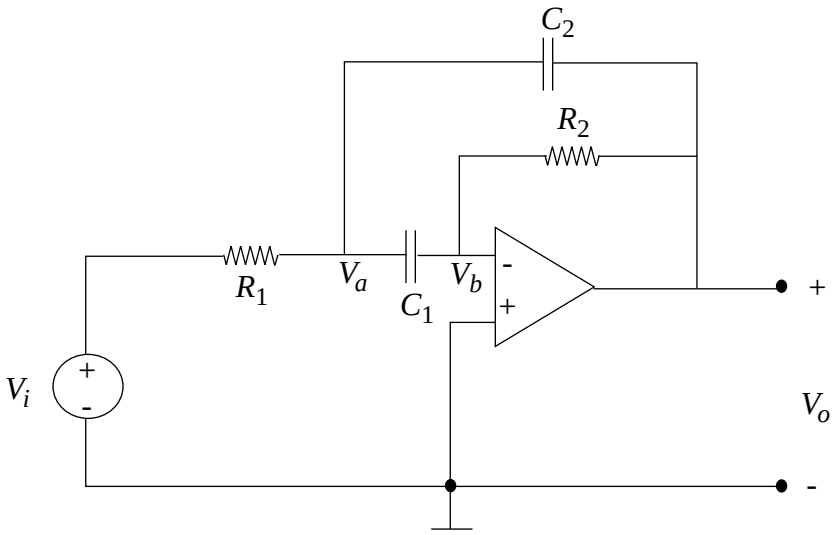


Figure 15.122:

Problem 15.41 a) Using the ideal Op Amp assumptions, write the node equations for the complex voltage for the circuit in Figure 15.122. Solve for V_o.

b) Assume V_o is of the form

$$V_o = \frac{sKV_i}{s^2 + 2\alpha s + \omega_0^2} \tag{15.3}$$

If a short pulse is now applied to this circuit, the output voltage after the pulse is

$$v_O(t) = 3e^{-100t}\sin(1000t + 20^o) \tag{15.4}$$

For $K = 400(sec^{-1})$ find the response $v_O(t)$ in the steady state to a 1 volt cosine wave at the resonant frequency:

$$v_I(t) = 1\cos\omega_0 t \tag{15.5}$$

(Provide *numbers* for ω_0 etc.)

c) Repeat b), for a one volt cosine wave at the lower 0.707 frequency ω_1.

Solution:

a) This was already done in Problem 15.38, except with capacitors C_1 and C_2 switched. Interestingly, the switch does not change our answer at all.

$$\frac{V_O}{V_I} = \frac{-R_2 C_1 s}{R_1 R_2 C_1 (C_1 + C_2) s^2 + R_1 C_2 s + 1}.$$

b) The transfer function is the response of a system to an impulse, so we can find the frequency-domain equivalent of the response, and from there match up the constants.

$$v_O(t) = 3e^{-100t} sin(1000t + L).$$

L is a non-relevant offset, since it will just change the amplitude, which we will be given anyway. We can rewrite the time-domain equation as:

$$v_O(t) = 3e^{-100t} \frac{1}{2j} (e^{1000jt} - e^{-1000jt}).$$

From this we can ascertain that the natural frequencies are $s = 100 \pm 1000j$.

We now find a quadratic equation with those roots:

$$s^2 + 200s + 10^4 + 10^6.$$

From this we can determine $\alpha = 100$ and $\omega_o = sqrt10^4 + 10^6$, or about 1005.

Our transfer function is as follows:

$$\frac{v_O}{v_I} = \frac{400s}{s^2 + 200s + 1010000}.$$

The steady-state response to a cosine can be found by plugging in $s = 1005j$, and finding the magnitude and phase of the resulting cosine output.

The constant and quadratic terms cancel out due to resonance, so we can simply find the gain by dividing 400 by 200. There is also no phase shift at resonance, so our output is also a cosine.

$$v_O(t) = 2cos(1005t).$$

c) The lower half-power frequency can be found by subtracting the half-bandwidth α from the resonance frequency. This turns out to be approximately 905 radians/sec. The magnitude and phase can be found in a similar manner as the last time. The magnitude ends up being about 1.3758, and the phase shift about 47.5 degrees.

$$v_O(t) = 1.3758cos(1005t - 47.5\ degrees).$$

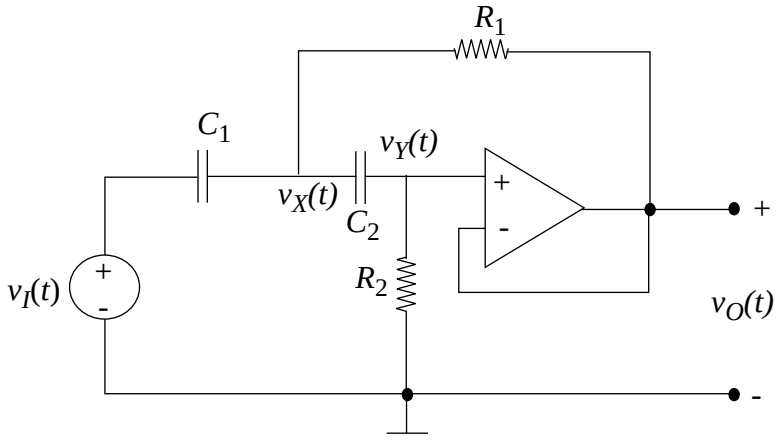


Figure 15.123:

ANS:: (a) $\frac{V_O}{V_I} = \frac{-R_2C_1s}{R_1R_2C_1(C_1+C_2)s^2+R_1C_2s+1}$, (b) $v_O(t) = 2cos(1005t)$., (c) $v_O(t) = 1.3758cos(1005t - 47.5\ degrees)$.

Problem 15.42 a) For the circuit in Figure 15.123 write the node equations needed to find $V_o(s)$ in terms of $V_i(s)$. Your answer *must* be arranged with the source terms on the left, the unknown variables on the right, and must use *conductances* $g(= 1/R)$.

b) Solving these equations, you should obtain for $C_1 = C_2$,

$$V_o(s) = \frac{s^2V_i}{s^2 + s\frac{2}{R_2C} + \frac{1}{R_1R_2C^2}} \tag{15.6}$$

For $R_1 = 1k\Omega$, find the values of R_2 and C which give a Q of 10 and a resonant frequency defined as the frequency where the s^2 term and the s^0 term cancel in the denominator of the above expression) of $\omega_o = 1000$ radians/second.

Solution:

a) From Problem 15.28:

$$(v_I - v_X)C_1s = (v_X - v_Y)C_2s + (v_X - v_O)G_1,$$

$$v_YG_2 = (v_X - v_Y)C_2s.$$

These can be rewritten in the desired form as follows:

$$v_1 C_1 s + v_O G_1 = v_X C_1 s + v_X C_2 s + v_X G_1 - v_Y C_2 s.$$

$$0 = -v_X C_2 s + v_Y G_2 + v_Y C_2 s.$$

b) For any transfer function whose denominator is $As^2 + Bs + C$, the resonant frequency is defined as $\sqrt{\frac{C}{A}}$ and the Q factor is $\sqrt{\frac{AC}{B^2}}$.

We get the following two equations:

$$\omega_0^2 = \frac{1}{1000 R_2 C^2},$$

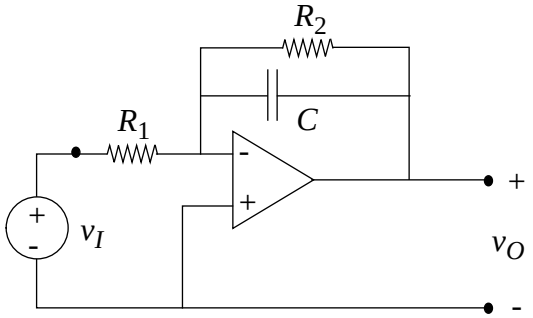
$$Q^2 = \frac{\frac{4}{R_2^2 C^2}}{\frac{1}{1000 R_2 C^2}}.$$

This implies that $R_2 = 400\Omega$ and $C = 1.5811x10^{-6}F$.

The resistor can be synthesized quite nicely by putting a 330Ω resistor in series with a 68Ω resistor, while the capacitor can be made from a $1.5x10^{-6}F$ capacitor in parallel with a $6.8x10^{-8}F$ capacitor with pretty reasonable margin of error.

ANS:: (b) $R_2 = 330\Omega + 68\Omega, C = 1.5x10^{-6}||6.8 * 10^{-8}$.

Problem 15.43 For the network shown in Figure 15.124:



Find V_o/V_i

Figure 15.124:

a) Determine an expression for the indicated transfer function.

b) Sketch the magnitude and angle of the indicated quantity as a function of frequency. You may use either linear or log-log coordinates, but it is recommended that you learn to use both kinds of axes.

Solution:

a) $\frac{V_o}{V_1} = \frac{-R_2}{j\omega R_1 R_2 C + R_1}$

b) See Figure 15.125

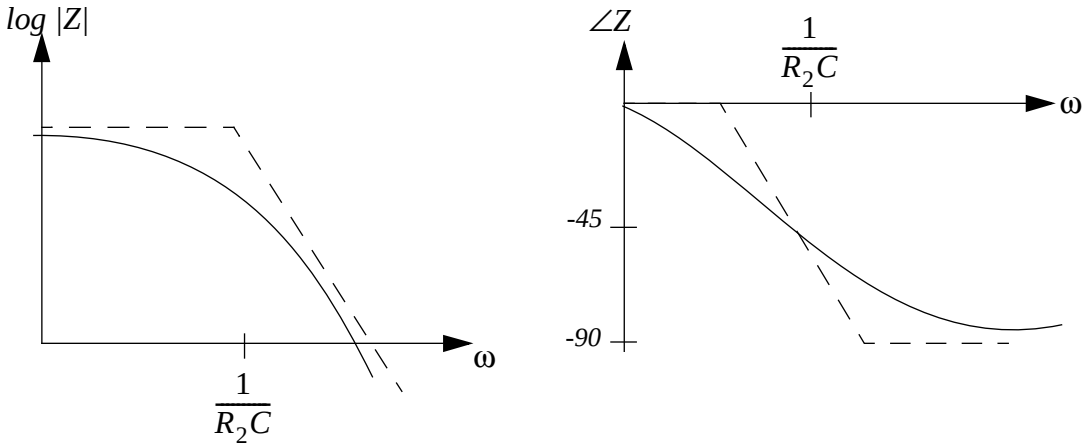


Figure 15.125:

ANS:: (a) $\frac{V_o}{v_i} = \frac{-R_2}{j\omega R_1 R_2 C + R_1}$

Chapter 16

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